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Semiconductor IC

Data Book 1990

CCD Camera & Peripheral

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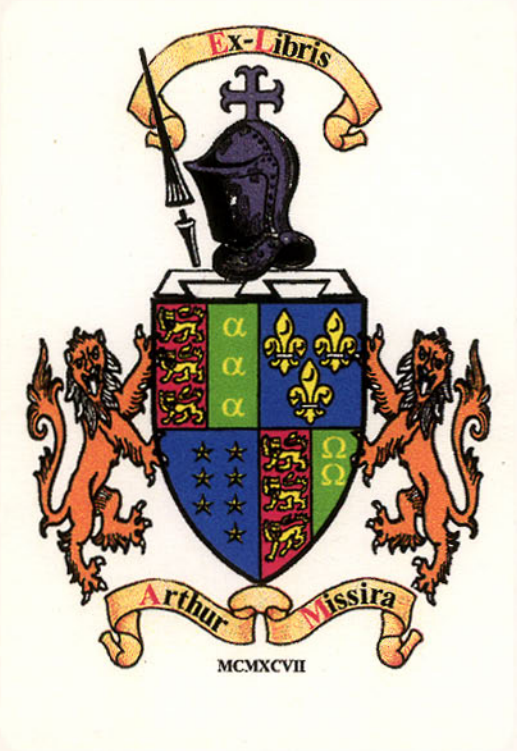
CCD Camera & Peripheral 1990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PREFACE

This is the 1990 version of the Sony semiconductor IC data book. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this data book, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

The contents of this data book although accurate and complete at the time of publication, are subject to change in order to incorporate improvements on the products.

Circuits shown are typical examples illustrating the operation of the devices. They are not meant to convey any patents or other rights. **Sony** cannot assume responsibility for any problems arising out of the use of these circuits.

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1. List of Model Names

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2. Index by Usage

1) CCD Camera (Black/White)

Type	Application	Function				Page
		Optical size (inch)	TV System	Picture elements (H×V)	Remarks	
ICX018CL	CCD Image Sensor for B/W	2/3	EIA	510×492		33
ICX021CL		2/3	CCIR	500×582		47
ICX022AL-3	CCD Image Sensor for B/W	2/3	EIA	768×493		61
ICX024AL-3	CCD Image Sensor for B/W	2/3	CCIR	756×581		75
ICX026BL	CCD Image Sensor for B/W	1/2	EIA	510×492	600mil shrink package	89
ICX027BL	CCD Image Sensor for B/W	1/2	CCIR	500×582	600mil shrink package	102
ICX038AL	CCD Image Sensor for B/W	1/2	EIA	768×494	600mil shrink package	115
ICX039AL	CCD Image Sensor for B/W	1/2	CCIR	752×582	600mil shrink package	131

2) CCD Camera (Color)

Type	Application	Function				Page
		Optical size (inch)	TV System	Picture elements (H×V)	Remarks	
ICX018CK	CCD Image Sensor for color	2/3	NTSC	510×492		149
ICX021CK		2/3	PAL	500×582		
IU018CK-AB	CCD Image Sensor for color unit	2/3	NTSC	510×492	Optical low-pass filter IR cut filter	161
IU021CK-AB		2/3	PAL	500×582	Optical low-pass filter IR cut filter	
ICX022AK-3	CCD Image Sensor for color	2/3	NTSC	768×493		164
ICX024AK-3	CCD Image Sensor for color	2/3	PAL	756×581		179
IU022AK-30A IU022AK-40A	CCD Image Sensor for color unit	2/3	NTSC	768×493	Optical low-pass filter IR cut filter	194
IU024AK-30A IU024AK-40A		2/3	PAL	756×581	Optical low-pass filter IR cut filter	
ICX022AN-3	CCD Image Sensor for color	2/3	NTSC	768×493		197
ICX024AN-3	CCD Image Sensor for color	2/3	PAL	756×581		214
ICX026BK	CCD Image Sensor for color	1/2	NTSC	510×492	600mil shrink package	231
ICX027BK	CCD Image Sensor for color	1/2	PAL	500×582	600mil shrink package	246
ICX038AK	CCD Image Sensor for color	1/2	NTSC	768×494	600mil shrink package	261
ICX039AK	CCD Image Sensor for color	1/2	PAL	752×582	600mil shrink package	278

3) CCD Imager System

Type	Application	Function	Page
IS018CL	CCD imager system kit for B/W camera	ICX018CL and three peripheral hybrid ICs, for EIA	297
IS021CL		ICX018CL and three peripheral hybrid ICs, for CCIR	
IS026BK	CCD imager system kit for color camera	ICX018CL and five peripheral hybrid ICs, for NTSC	301
IS027BK		ICX018CL and five peripheral hybrid ICs, for PAL	

4) IC for Scanning System of Video Camera

Type	Application	Function	Page
CXD1030M	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL	313
CXD1158M	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL sub carrier output × 3	322
CXD1159Q	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL window pulse output	332
CXD1217M	Sync signal generator	Compatible with the respective systems, NTSC, PALM, PAL and SECAM color framing by the respective systems, NTSC, PALM, PAL and SECAM	341
CX23047B	Timing pulse generator for scanning system	CCD drive timing pulse generation, signal processing pulse generation, for ICX018CK/CL, ICX021CK/CL	353
CXD1035BQ-Z	Timing pulse generator for scanning system	CCD drive timing pulse generation, signal processing pulse generation, for ICX022AK/AL, ICX024AK/AL	364
CXD1141M	Variable electric shutter timing generator	Variable electronic shutter timing generation (1/60 to 1/10000 sec.) for ICX022AK/AL, ICX024AK/AL	376
CXD1156Q/R	Timing Generator for CCD driving Camera	CCD drive timing pulse generation, Variable electronic shutter timing generation (1/60 to 1/10000 sec,) for ICX026BK/BL, ICX027BK/BL	380
CXD1251Q	Blemish compensation timing generator	Blemish compensation timing generator, for ICX026BK/BL, ICX027BK/BL	393
CXD1255Q	Timing Generator for CCD driving Camera	CCD drive timing pulse generation, signal processing pulse generation, for ICX038AK/ICX039AK variable electronic shutter timing generation (1/60~1/10000 sec)	398
CXB0026AM	CCD clock driver	CCD imager driver × 2, compatible with high frequency operation	412
CX20180	Vertical clock drive	CCD imager driver × 4, lead-out generation inverter, negative voltage generation inverter	415
CXA1065M	Vertical clock drive	CCD imager driver × 4, lead-out generation inverter, negative voltage generation inverter	426
CXD1250M	Vertical clock drive	CCD imager driver × 4, lead-out generation inverter	441

5) Signal Processing IC for Video Camera

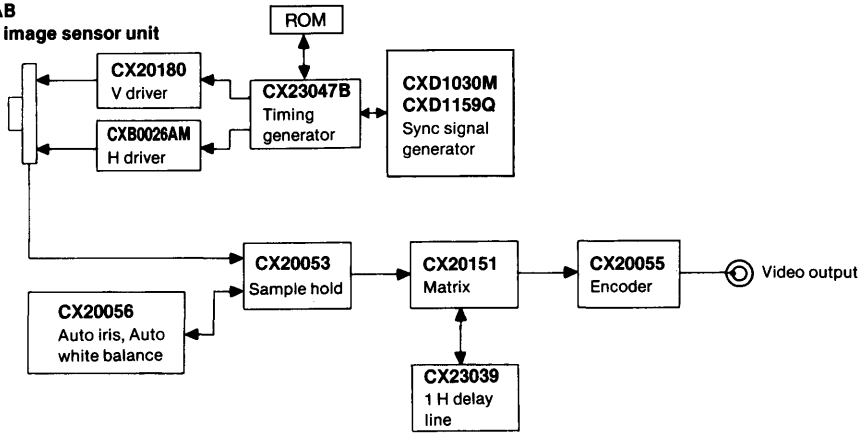
Type	Application	Function	Page
CXA1310AQ	Monochrome camera	Single Chip Processing for CCD Monochrome camera	451
CX20053	Sample hold	CDS, color separation, color mix correction, γ correction, blanking, white clip, pedestal setting	465
CX20055	Encoder	Aperture correction, blank cleaning, white clip, chroma mod, fader, finder, switcher, 75Ω driver	484
CX20056	Auto iris, auto white balance	Iris drive, RB line seq. signal separation, auto white balance, low light alarm	503
CX20151	Matrix	Color differential, signal forming, luminance signal forming, multiplexer	521
CX23039	1H delay line×4	1H delay line × 4, S/H, delay line driver	546
CXA1337Q-Z/R	Sample hold	CDS,AGC, Color separation, chroma suppress	559
CXA1338Q-Z/R	Signal processing	From color compensation (Mg, G, Cy, Ye) interleave coding, R, G, B sythetic and Y signal processing	577
CXA1339Q-Z/R	Matrix	Matrix, white balance, γ correction, negative/positive inversion	598
CXA1072Q-Z/R	Encoder	Aperture, auto-corrier balance, negative-positive reverse, fader, chroma suppression, BLK cleaning	616
CXL1503M CXL1505M	For matrix 1H delay line Signal Processing	1H CMOS-CCD delay line × 4	640
CXL1504M	Luminous signal 1H delay line	1H CMOS-CCD delay line	648
CXA1270N	Vertical outline compensation	Signal generation during, Vertical Outline Compensation	656
CX20095A CX20186	Video output	6dB amp, video driver, bilateral video driver	664

6) CCD Delay Line

Type	Application	Function	Page
CXL1009P	Video disk	CMOS-CCD delay line for time base corrector, 300mil shirink-DIP	673
CXL1008P/M	VCR	NTSC skew compensate	682
CXL5001P/M	General purpose	NTSC 1H CMOS-CCD delay line	694
CXL5002P/M	General purpose	NTSC 1/2H CMOS-CCD delay line	701
CXL5003P/M	General purpose	PAL 1H CMOS-CCD delay line	707
CXL5005P/M	General purpose	NTSC 1H CMOS-CCD delay line, with PLL	714

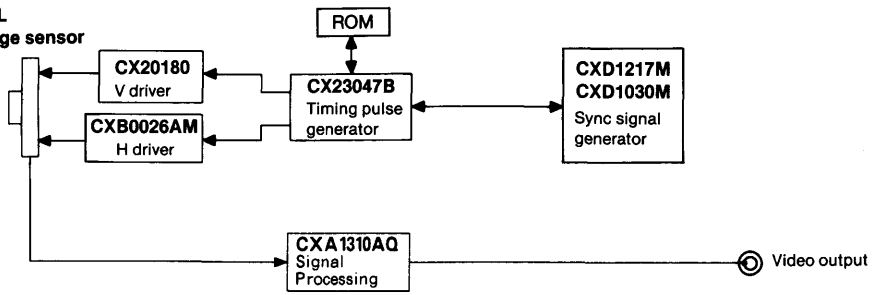
■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 2/3″ LENS SYSTEM

ICX018CK
ICX021CK
CCD color image sensor
IU018CK-AB
IU021CK-AB
CCD color image sensor unit



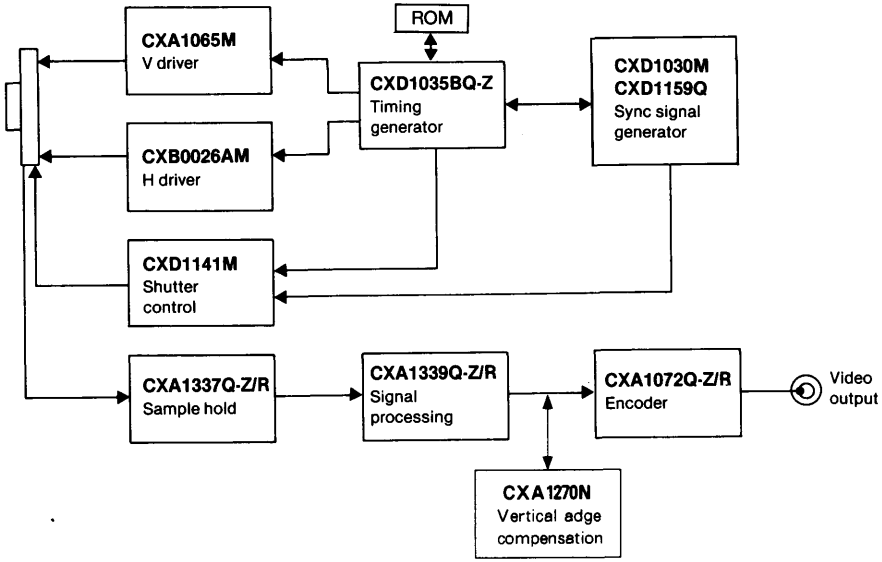
■ CCD B/W CAMERA BLOCK DIAGRAM FOR 2/3″ LENS SYSTEM

ICX018CL
ICX021CL
CCD image sensor



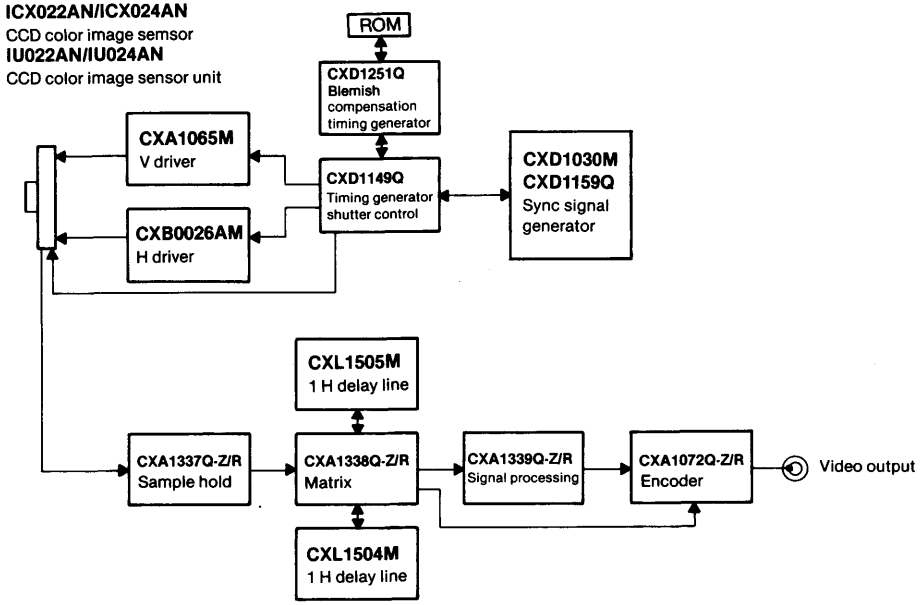
■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 2/3″ LENS SYSTEM

ICX022AK/ICX024AK
CCD color image sensor
IU022AK/IU024AK
CCD color image sensor unit



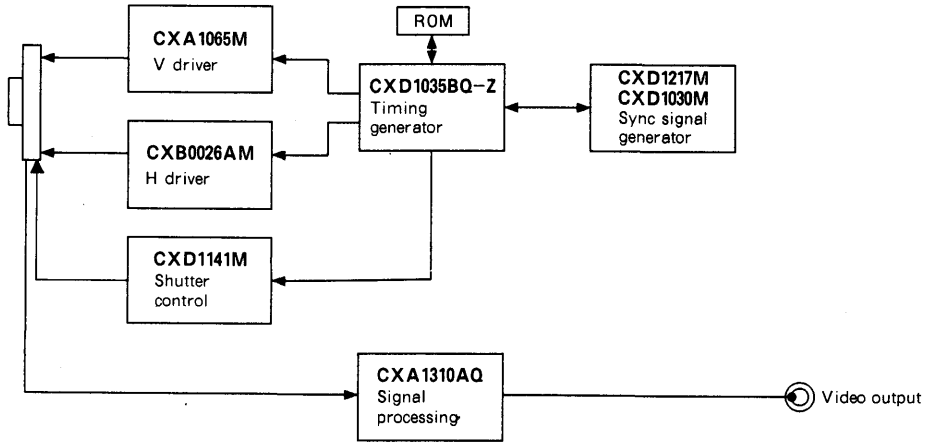
■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 2/3″ LENS SYSTEM

ICX022AN/ICX024AN
CCD color image semsor
IU022AN/IU024AN
CCD color image sensor unit



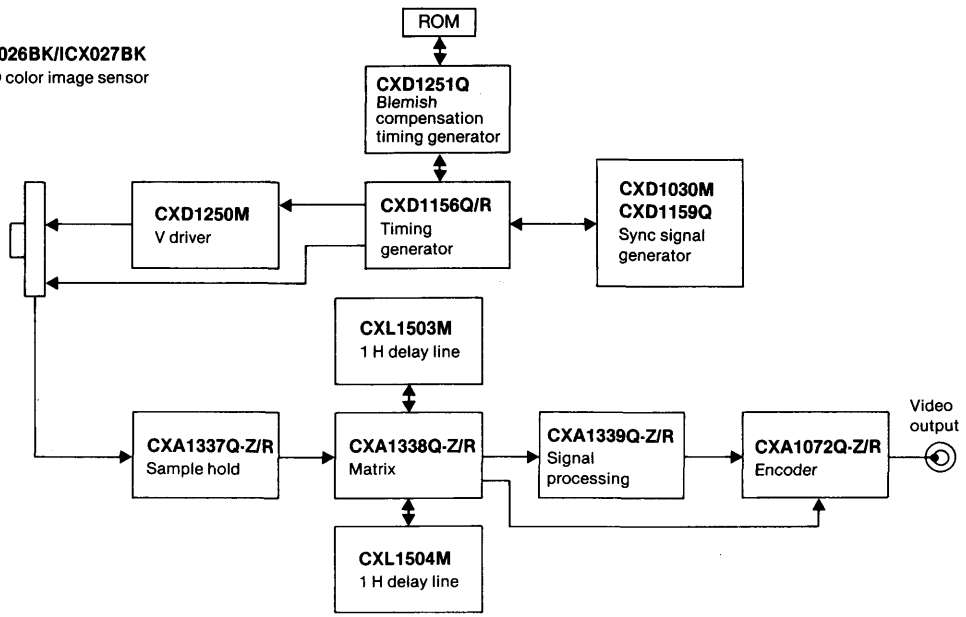
■ CCD B/W CAMERA BLOCK DIAGRAM FOR 2/3" LENS SYSTEM

ICX022AL–3
ICX024AL–3
CCD image sensor



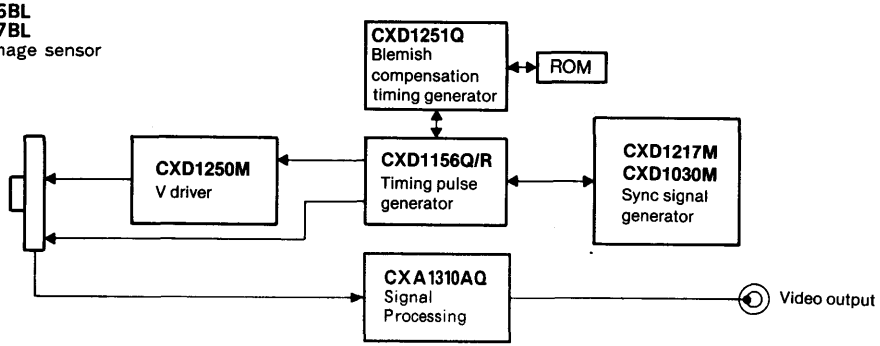
■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 1/2" LENS SYSTEM

ICX026BK/ICX027BK
CCD color image sensor



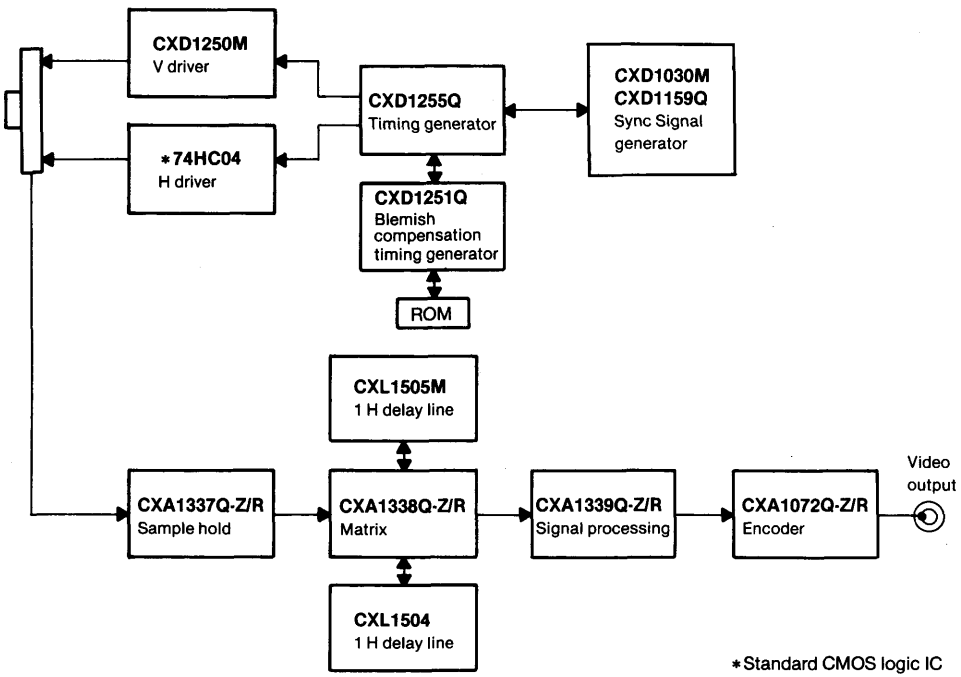
■ CCD B/W CAMERA BLOCK DIAGRAM FOR 1/2″ LENS SYSTEM

ICX026BL
ICX027BL
CCD image sensor



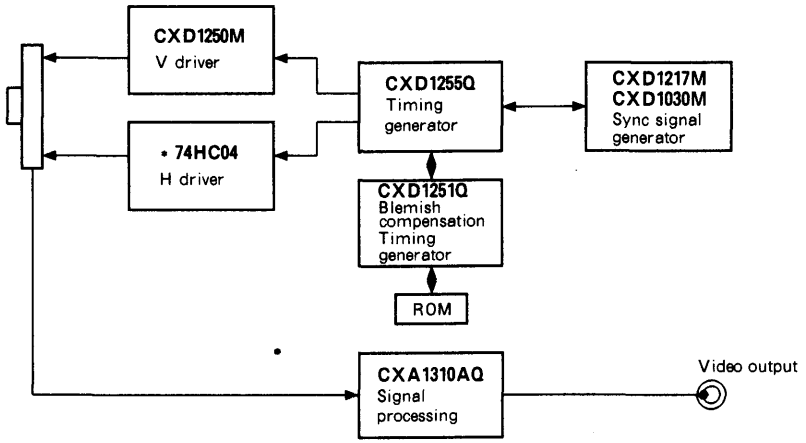
■ CCD COLOR CAMERA BLOCK DIAGRAM FOR 1/2″ LENS SYSTEM

ICX038AK
ICX039AK
CCD image sensor



■ CCD B/W CAMERA BLOCK DIAGRAM FOR 1/2" LENS SYSTEM

ICX038AL
ICX039AL
CCD image sensor



* Standard CMOS logic IC

3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

a) Conventional nomenclature system

[Example] CX 20 011 A

- Improvement mark
  "A" is affixed when specifications are partially improved.
- Product number
  Identifies individual product.
- Category number
  Indicates the product category in one or two digits.
  Bipolar IC: 0, 1, 8, 10, 20, 22
  MOS IC: 5, 7, 23, 79
- Sony IC mark

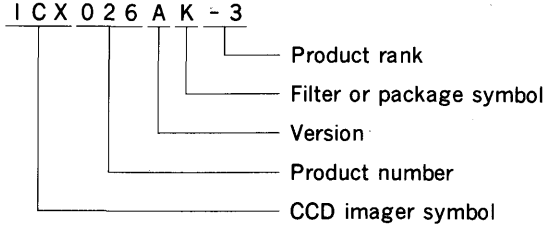
b) New nomenclature

[Example] CX A 1001 A P

- Package mark
  P: Plastic Dual In-line Package
  D: Ceramic Dual In-line Package
  M: Small Outline L-Leaded Package
  L: Single In-line Package
  Q: Quad Flat L-Leaded Package
  S: Shrink Dual In-line Package
  N: Very Small Outline Package (SSOP)
  R: Very Small Quad Flat Package
- Improvement mark
  "A" is affixed when specifications are improved.
- Product number
  Identifies the individual product.
- Product category mark
  A: Bipolar IC
  B: Bipolar digital IC
  D: MOS logic IC
  K: Memory, Mask ROM
  P, Q: Microcomputer, Microprocessor
  L: CCD signal processor
- Sony IC mark

2) Nomenclature of CCD Imager

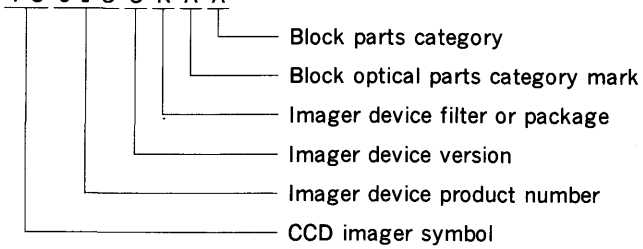
(Example) ICX026AK-3



3) Nomenclature of CCD Imager Block

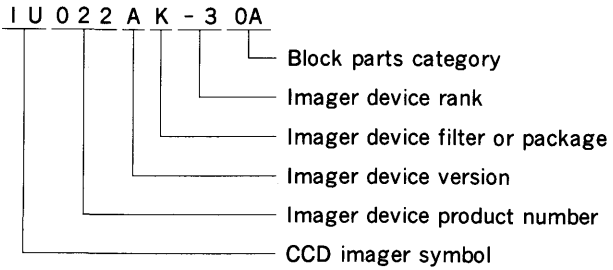
a) Conventional nomenclature system

(Example) IU018CKAA



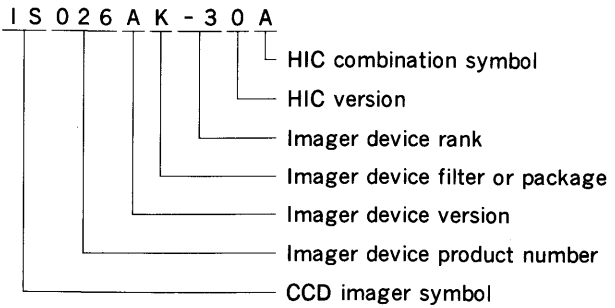
b) New Nomenclature

(Example) IU022AK-30A



4) Nomenclature of CCD Imager System

(Example) IS026AK-30A



4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

Maximum rating must never be reached for any TWO items at the SAME time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit, the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

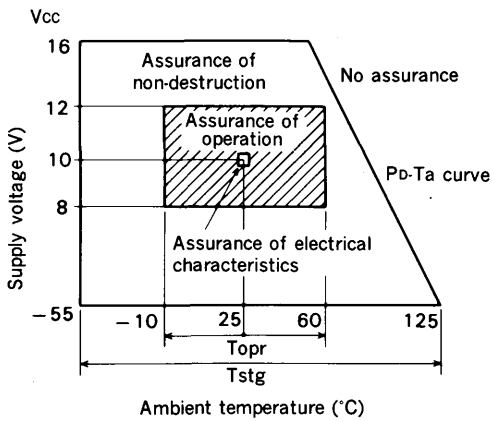
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

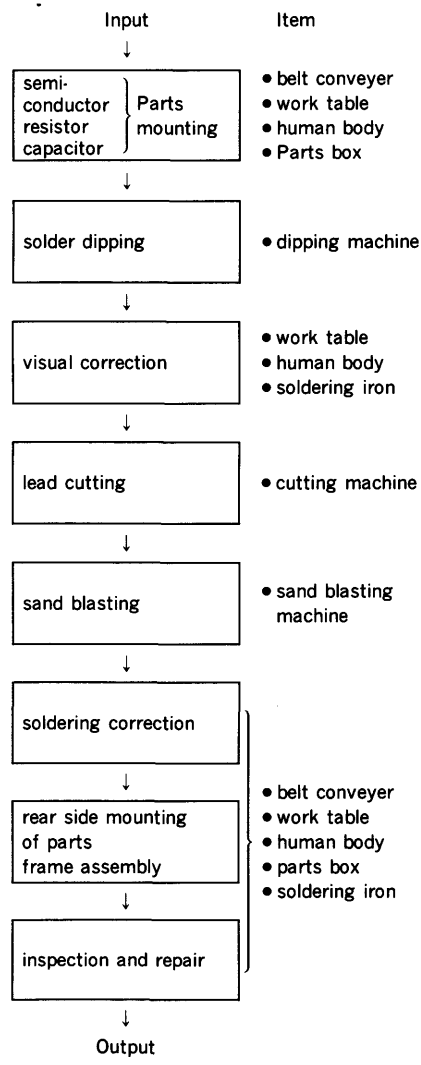
Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

①Equalize potentials of terminals when transporting or storing.

②Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③Prepare an environment that does not generate static electricity.

One method is keeping relative humidity in the work room to about 50%.

Operator

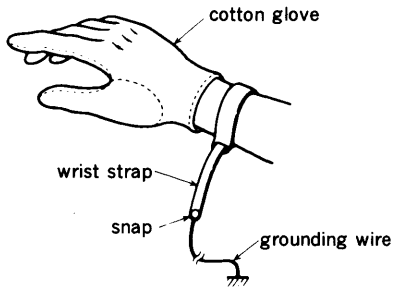
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling and semiconductor device.

example of grounding band

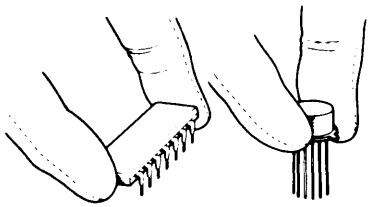


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



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Equipment and tools

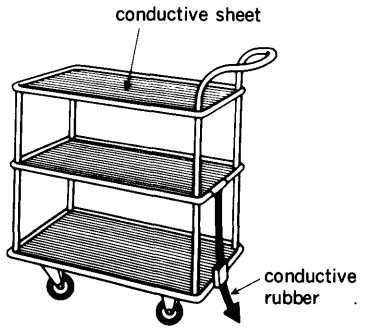
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

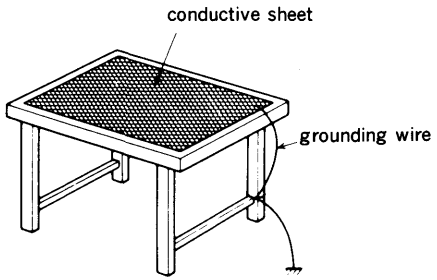
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

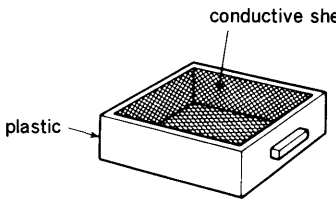
grounding of work table



(3) Semiconductor device case

Use a metal case, or an antistatic plastic case (lined with conductive sheet).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or on a wood or on a metal carrier.

(5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

(6) Other points of caution

Take note of the kind of brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

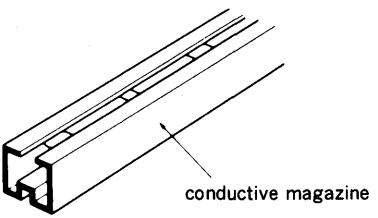
Transporting, storing and packaging methods

(1) Magazine

Use metal, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.

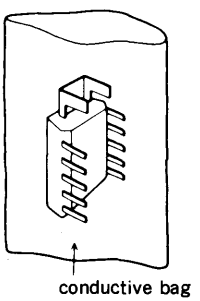
magazine



(2) Bag

Use a conductive bag to store ICs. If the use of vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.

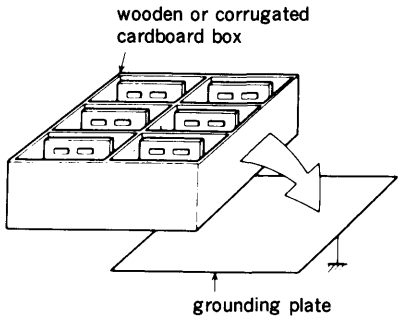
bag



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



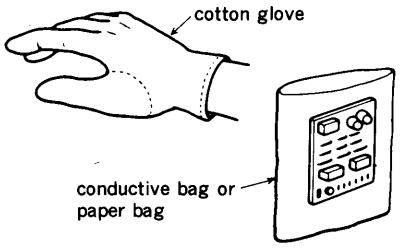
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than 10MΩ (DC 500V) after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

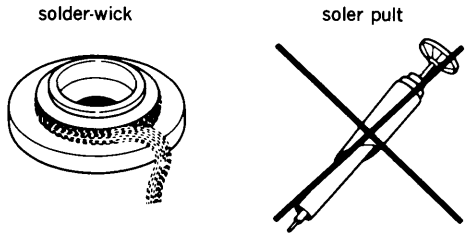
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

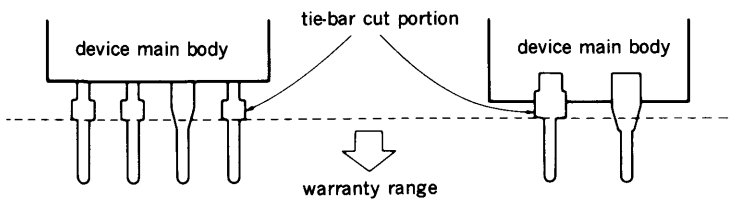
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{0}$ seconds in a solder bath of 350°C±10°C, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be 260°C±5°C. To solder by soldering iron temperature should be 350°C±10°C.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at 260°C±5°C. The distance between the device main body and solder bath is 1.6 mm.

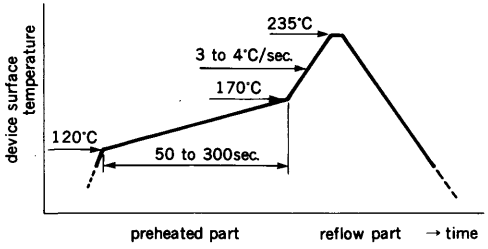
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

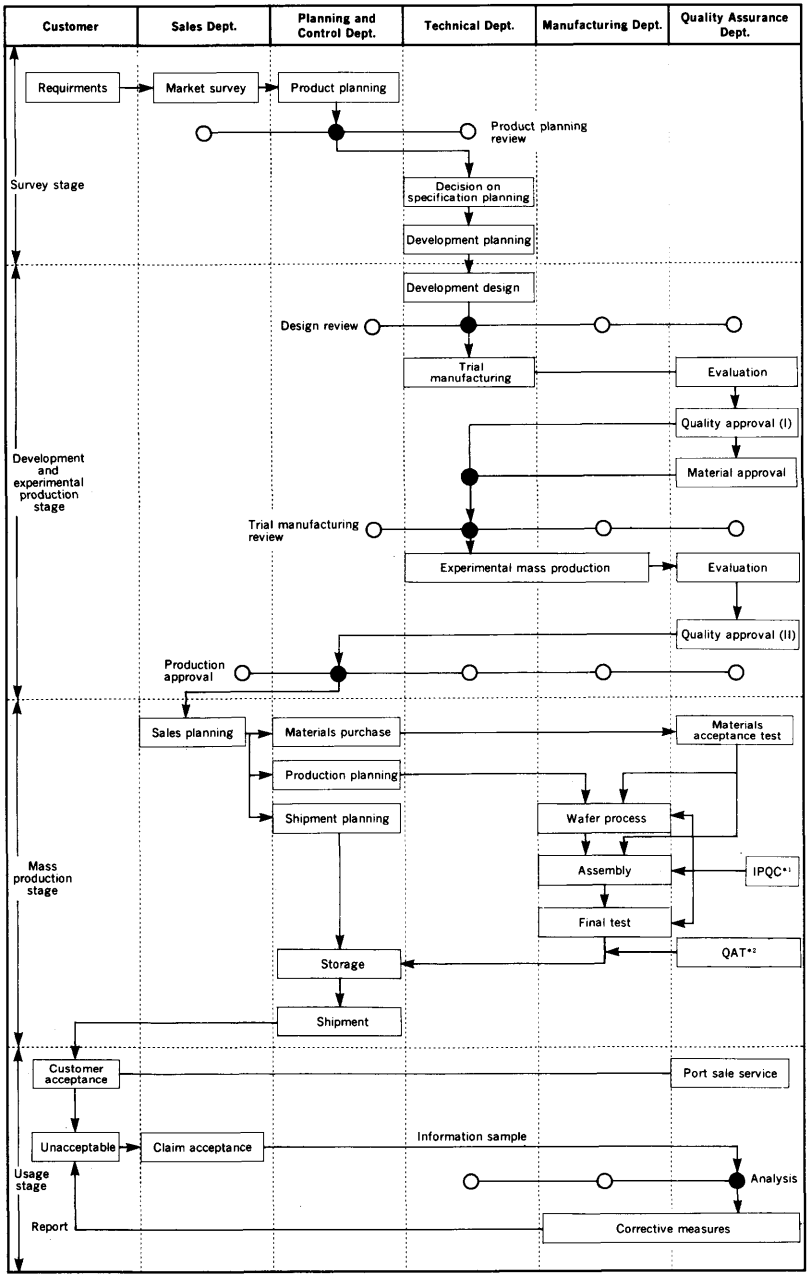
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing, orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.

Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item		Testing time	LTPD
Electrical Characteristics Test		In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation	up to 1000 h	10%
	high temperature and high humidity with bias	up to 1000 h	10%
	pressure cooker	up to 200 h	10%
Environmental Test	soldering heat resistance	10s	15%
	heat cycle	100 cycles	15%
Mechanical Test	solderability	Japan Industrial Standard (JIS)	15%
	length strength		15%
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.		

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

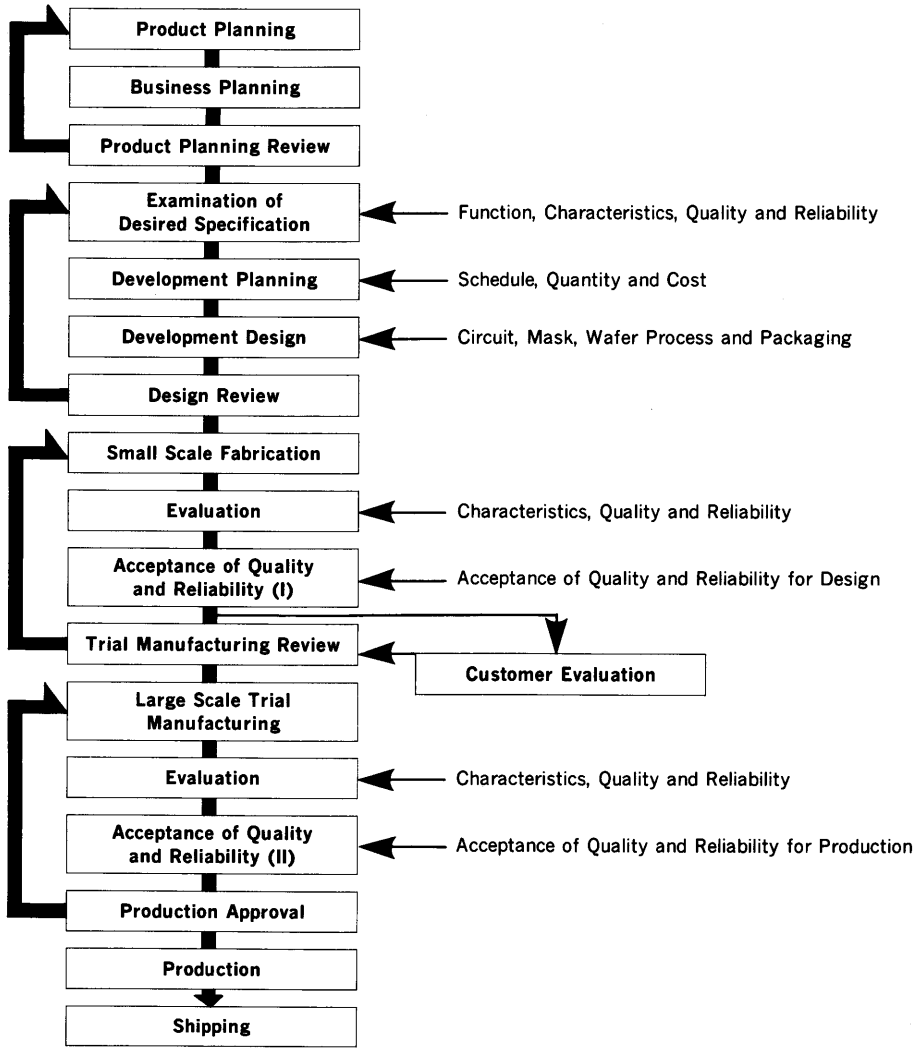
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta=−65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta=−65°C to+150°C		100c	10%
Heat shock	Ta=−65°C to+150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)	based on JIS			10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

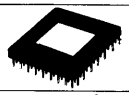
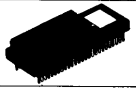
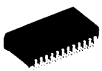
LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

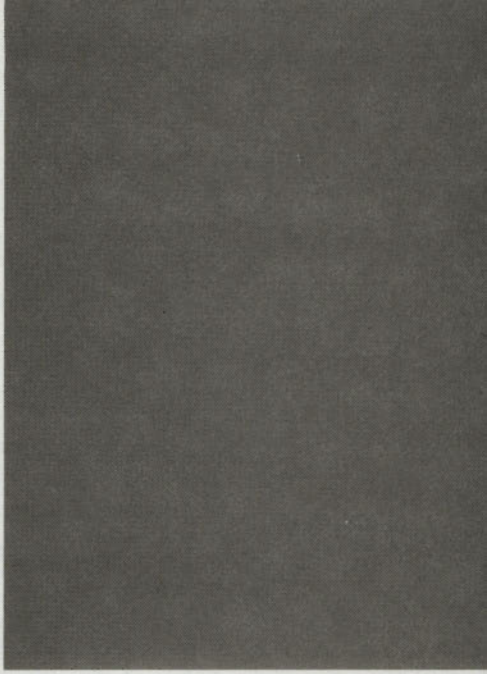
Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



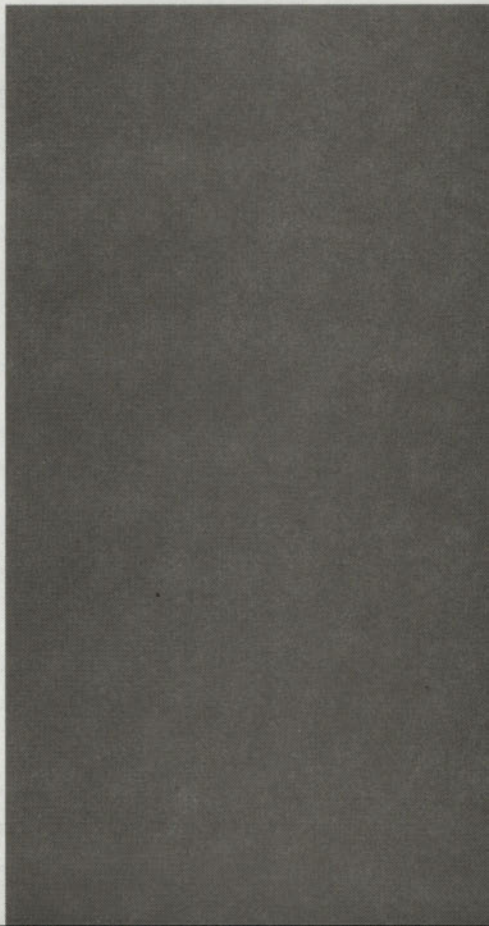
Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	Zig-Zag IN-LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK Zig-Zag IN-LINE PACKAGE		P	1.778mm (70MIL) Zig Zag inline	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE		P	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
	Standard chip carrier	Q F J (PLCC)	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		Q F N (LCC)	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package side

*P……Plastic, C……Ceramic



CCD Camera (Black/White)



1) CCD Camera (Black/White)

Type	Application	Function				Page
		Optical size (inch)	TV System	Picture elements (H×V)	Remarks	
ICX018CL	CCD Image Sensor for B/W	2/3	EIA	510×492		33
ICX021CL		2/3	CCIR	500×582		47
ICX022AL-3	CCD Image Sensor for B/W	2/3	EIA	768×493		61
ICX024AL-3	CCD Image Sensor for B/W	2/3	CCIR	756×581		75
ICX026BL	CCD Image Sensor for B/W	1/2	EIA	510×492	600mil shrink package	89
ICX027BL	CCD Image Sensor for B/W	1/2	CCIR	500×582	600mil shrink package	102
ICX038AL	CCD Image Sensor for B/W	1/2	EIA	768×494	600mil shrink package	115
ICX039AL	CCD Image Sensor for B/W	1/2	CCIR	752×582	600mil shrink package	131

Solid-State Image Device for EIA B/W TV System

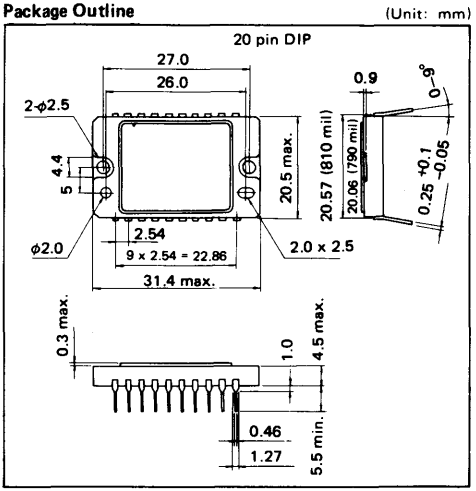
Description

ICX18CL is an interline transfer CCD solid-state imaging device developed for one-chip B/W cameras.

Features

- Number of effective picture elements
  510 (H) x 492 (V)
- Number of optical black elements
  Horizontal (H) direction
  2 picture elements in front
  20 picture elements in back
  Vertical (V) direction
  12 picture elements in front
- High sensitivity
- Low smear
- Anti-blooming
- Low lag, no burning
- Resistance to electro-magnetic field and micro-phonic noise
- Precise image geometry
- γ characteristic: 1

Package Outline (Unit: mm)



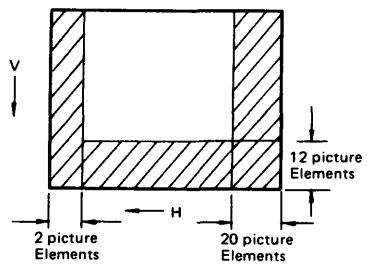


Fig. 1 Layout of Optical Black Elements

Device Organization

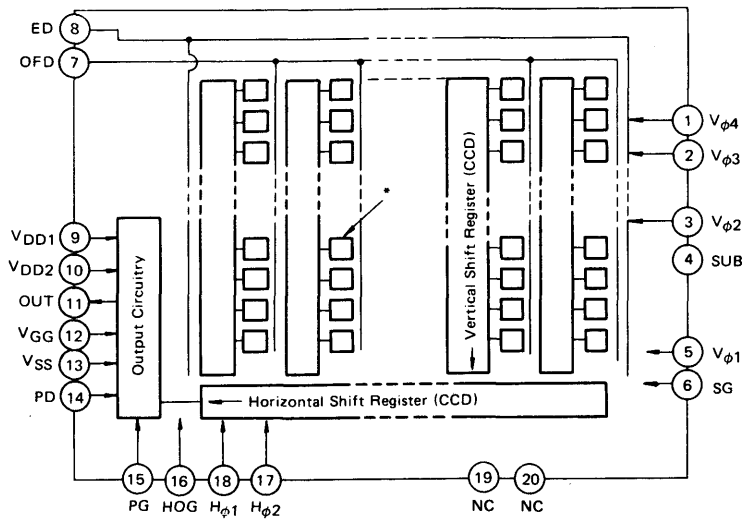
- Interline transfer CCD image sensor
- Unit cell size 17 μm (H) x 13 μm (V)
- Number of dummy bits 8 bits horizontal, 1 bit vertical (even field only)
- Chip size 10.0 mm (H) x 9.3 mm (V)
- Thin polysilicon gate MOS diode sensor using the multi-layer interference effect
- On-chip, high-sensitivity output amplifier
- P-sub, P-well structure

50185A-TO

Absolute Maximum Ratings

• Supply voltages V_{DD1}, V_{DD2}, and V_{PD}	−0.3 to +30V	(SUB = 0V)
• Horizontal and vertical clock pins — SUB	−20 to +20V	
• Between horizontal clocks, between vertical clocks	22V	
• Horizontal and vertical clock pins — Sensor gate	18V	
• Pins other than those listed above	−0.3 to +20V	
• Storage temperature	−30 to +80°C	
• Operating temperature	−10 to +55°C	

Block Diagram



* **Note)** —□— : Photosensor

Pin Configuration (Top View)

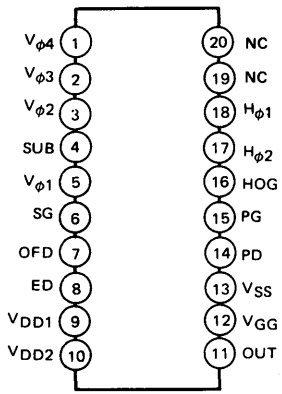


Fig. 2

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V_{\phi4}$	Vertical register transfer clock input	11	OUT	Signal output *
2	$V_{\phi3}$	Vertical register transfer clock input	12	V_{GG}	Output amplifier gate bias *
3	$V_{\phi2}$	Vertical register transfer clock input	13	V_{SS}	Output amplifier source bias *
4	SUB	Substrate	14	PD	Output reset drain *
5	$V_{\phi1}$	Vertical register transfer clock input	15	PG	Output reset clock *
6	SG	Sensor gate bias	16	HOG	Horizontal register read out control bias *
7	OFD	Anti-blooming bias *	17	$H_{\phi2}$	Horizontal register transfer clock input
8	ED	Edge drain bias *	18	$H_{\phi1}$	Horizontal register transfer clock input
9	V_{DD1}	Power supply *	19	NC	
10	V_{DD2}	Power supply *	20	NC	

* Never supply negative voltage to pins.

DC Bias Conditions

(Some of the characteristics shown below are determined by the recommended circuit in Fig. 4. Refer to Note 1 through 8.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Substrate bias	V_{SUB}		0		V	V_{SUB} = GND
Output circuit supply voltages	V_{DD1}	19	20	21	V	$V_{DD1} = V_{DD2}$
	V_{DD2}	19	20	21	V	
	V_{PD}	17	18.1	19.2	V	Note 1
	V_{SS}	Grounded with 2.2kΩ resistor				Note 2
	V_{GG}	7	9	11	V	Note 1
Anti-blooming bias	V_{OFD}	11	12	13	V	Note 3
Edge drain bias	V_{ED}	V_{OFD}				
HOG bias	V_{HOG}	0.8	1.0	1.2	V	
Sensor gate bias	V_{SG}	8.5	9.5	10.5	V	Note 3

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
DC supply current	I_{DD}		3.2	4	mA	Note 4
Input current 1	Iin1			1	μA	Note 5
Input current 2	Iin2			10	μA	Note 6

Clocl Voltage Conditions

(Some of the characteristics shown below are determined by the recommended circuit in Fig. 4. Refer to Note 1 through 8.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Read out pulse	V_{VT}	11.0	13.0	14.0	V	Note 3
Vertical transfer clocks						
Low level	V_{VL}	-5.5	-5.0	-4.5	V	Note 3
Amplitude	$V_{\phi V}$	6.8	7.5		V	
Horizontal transfer clocks						
Low level	V_{HL}	-4.4	-4.0	-3.6	V	
High level	V_{HH}	0.8	1.0	4.4	V	Note 7
Amplitude	$V_{\phi H}$	4.75	5.0	8.8	V	Note 7
Output reset clocks						
Low level	V_{PGL}	1.0	1.3	1.7	V	Note 8
High level	V_{PGH}	8.9	9.3	10.5	V	
Amplitude	$V_{\phi PG}$	7.2	8.0	8.8	V	

Clock Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical transfer clock vs. GND	$C_{\phi V}$		6200		pF	
Between vertical transfer clocks	$C_{\phi VV}$		1800		pF	
Output reset clock	$C_{\phi PG}$		14		pF	

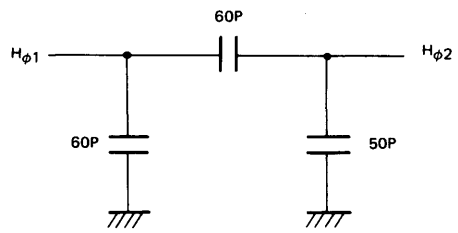


Fig. 3 Horizontal Transfer Clock Equivalent Circuit

Note)

1. V_{PD}, V_{GG}, and V_{HOG} should be produced from V_{DD1} and V_{DD2}. Resistance precision should be ±5%. See Figs. 4 and 5.
2. V_{SS} should be self-biased and should be connected to GND through a 2.2kΩ (±5%) resistor.
3. $V_{VHH} + 5.1 \leqq V_{SG} \leqq V_{VT} - 1.5$ $\quad V_{VT} \leqq V_{OFD} + 2$ (Unit: V)
   V_{VHH} is the maximum level of the waveforms containing couplings of vertical transfer clocks $V_{\phi1}$ to $V_{\phi4}$ excluding the period in which a three level VT is pulsed.
4. Total output amp current, when the load resistance is 2.2kΩ.
5. The current to the substrate when 20V is sequentially applied to Pins $V_{\phi1}$, $V_{\phi2}$, $V_{\phi3}$, $V_{\phi4}$, $H_{\phi1}$, and $H_{\phi2}$.
6. The current to the substrate when 20V is applied to SG, ED, OFD, PD, HOG, TP1, and TP2 independently. The terminals, which have not been measured, should be connected to the ground.

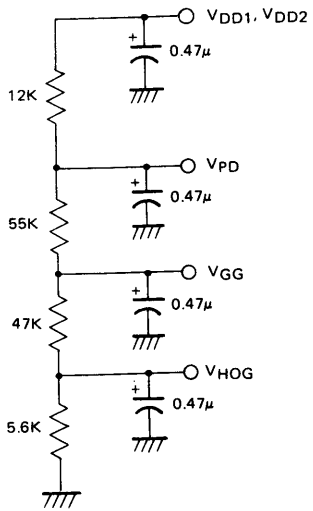
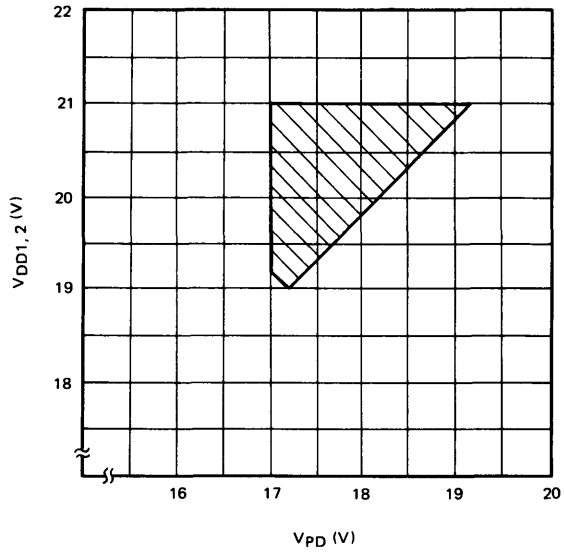


Fig. 4 Recommended Circuit for Bias Setting of V_{DD1}, V_{DD2}, V_{PD}, V_{GG}, and V_{HOG}



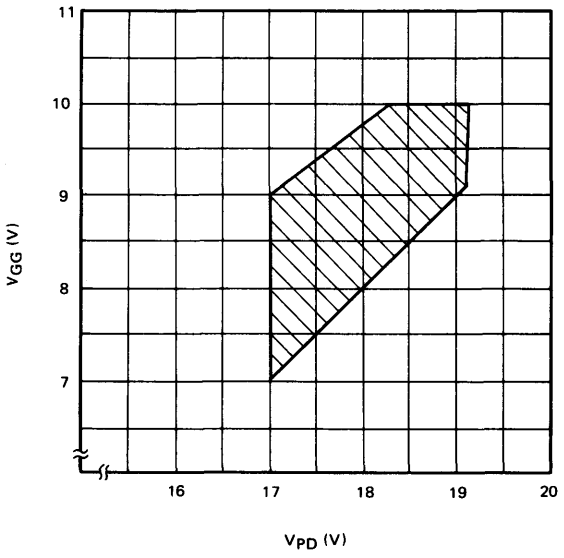


Fig. 5 Bias Setting Range of V_{DD1}, V_{DD2}, V_{PD}, and V_{GG}

The shaded section is the recommended operating range.

Note) 7 V_{HH}, $V_{\phi H}$, and V_{HL} are determined as follows.

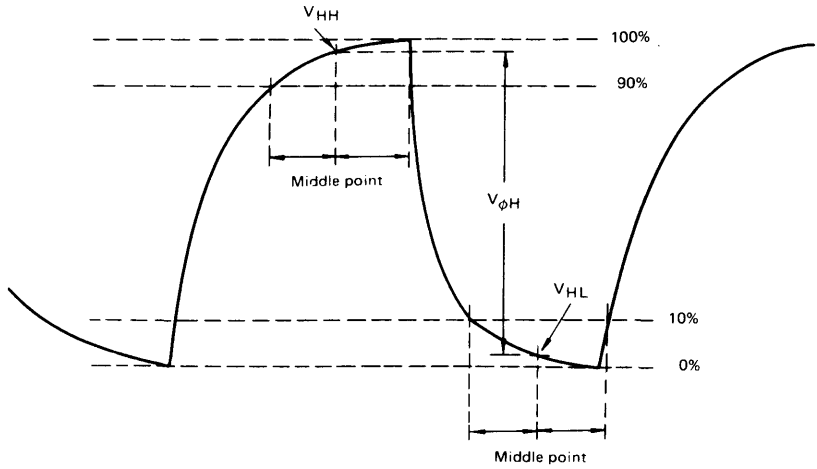


Fig. 6 Horizontal Transfer Clock Waveform

8 V_{PGL}, V_{PGH}, and $V_{\phi PG}$ are determined as follows.

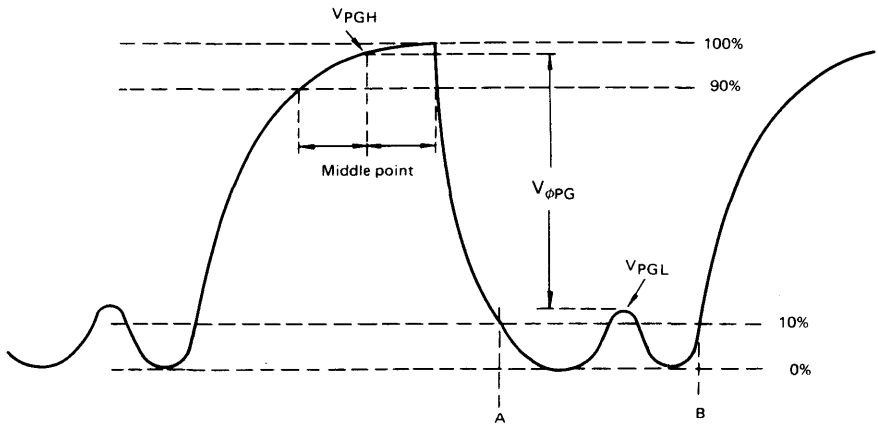


Fig. 7 Output Reset Clock Waveform.

V_{PGL} is defined by the maximum level between Points A and B. Be careful not to allow ringing on the low side to be less than 0V.

Drive Pulse Waveform Conditions

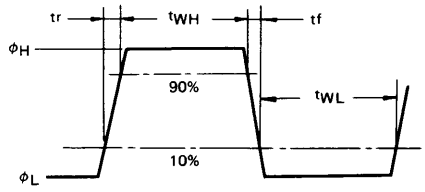


Fig. 8 Pulse Waveform

Symbol	tWH			tWL			tr			tf			Unit	Condition
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$H_{\phi1}$		42			42			10			10		ns	During scanning time
$H_{\phi2}$		42			42			10			10			
$H_{\phi1}$		6.8						0.01			0.01		μs	During parallel-serial conversion
$H_{\phi2}$		0						0			0			
PG	10	42			42			10			10		ns	Normally PG = $H_{\phi1}$
$V_{\phi1}/V_{\phi2}$		61.2			2.1			0.1			0.1	0.5	μs	During scanning time
$V_{\phi3}/V_{\phi4}$		3.6			59.6			0.1			0.1	0.5		
$V_{\phi1}/V_{\phi3}$		19						1			1			During read out from sensor

Operating Characteristics

Ta = 25°C See the Test Circuit.

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Condition
Sensitivity	S	110	160	220	mV	1	
Saturation Output Voltage	V_{sat}	400	530	850	mV	2	
Video Signal Shading	SV1		10	19	%	3	
Smear	SM		0.01	0.04	%	4	
Dark Signal	Vdt			13	mV	5	Ta = 55°C
Dark Signal Shading	ΔVdt			4	mV	6	Ta = 55°C

Test Method

○ Test conditions

1) The device drive conditions in the following measurements should be adjusted to the typical values of the DC and clock voltage conditions. (See Fig. 9.)
2) In measurements mentioned below, blemishes should be excluded. Unless specified, the optical black level should be the reference for the signal output, and the value measured at Point B in Fig. 9 should be used.

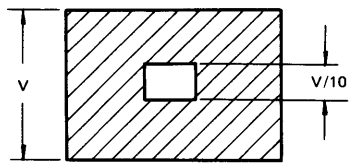
○ Definition of standard imaging condition

1) Standard imaging condition 1: Use Pattern box (Brightness 706 nt. 3200°K Halogen source) at F8 with FUJINON lens H6 x 12.5D (F1.4). CM-500S (1.0 mmt) should be used as an IR cut filter.
2) Standard imaging condition 2; Uniformity of a light source within 2%. The light-source color temperature should be 3200°K, and CM-500S (1.0 mmt) should be used as an IR cut filter. The quantity of light should be adjusted to the average value of output voltage Vs shown in each item.

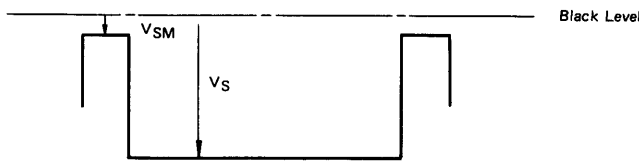
1. Set to the standard imaging condition 1 and measure output signal in the center of the screen.
2. Set to the standard imaging condition 2, adjust the intensity of light, check anti-blooming, then measure the minimum value of signal for the whole screen.
3. After setting up standard imaging condition 2, set the pattern box on the entire screen and measure the maximum and minimum output voltages of Channel (Vmax, Vmin) adjusting Vs to 300 mV.

$$SV_1 \equiv \frac{Vmax - Vmin}{Vs} \times 100(\%)$$

4. After setting up standard imaging condition 2, set the pattern box on a vertical 1/10 screen. Measure the average signal voltage Vs and maximum value V_{SM} during vertical blanking. (Vs = 300 mV, 1/10 V method)



$$SM \equiv \frac{V_{SM}}{V_S} \times 100\ (\%)$$



5. Average dark signal at ambient temperature of 55°C.
6. Measure maximum and minimum dark signal (Vdmax, Vdmin). Blemishes should be excluded. The temperature should be 55°C.

$$\Delta Vdt \equiv (Vdmax - Vdmin)$$

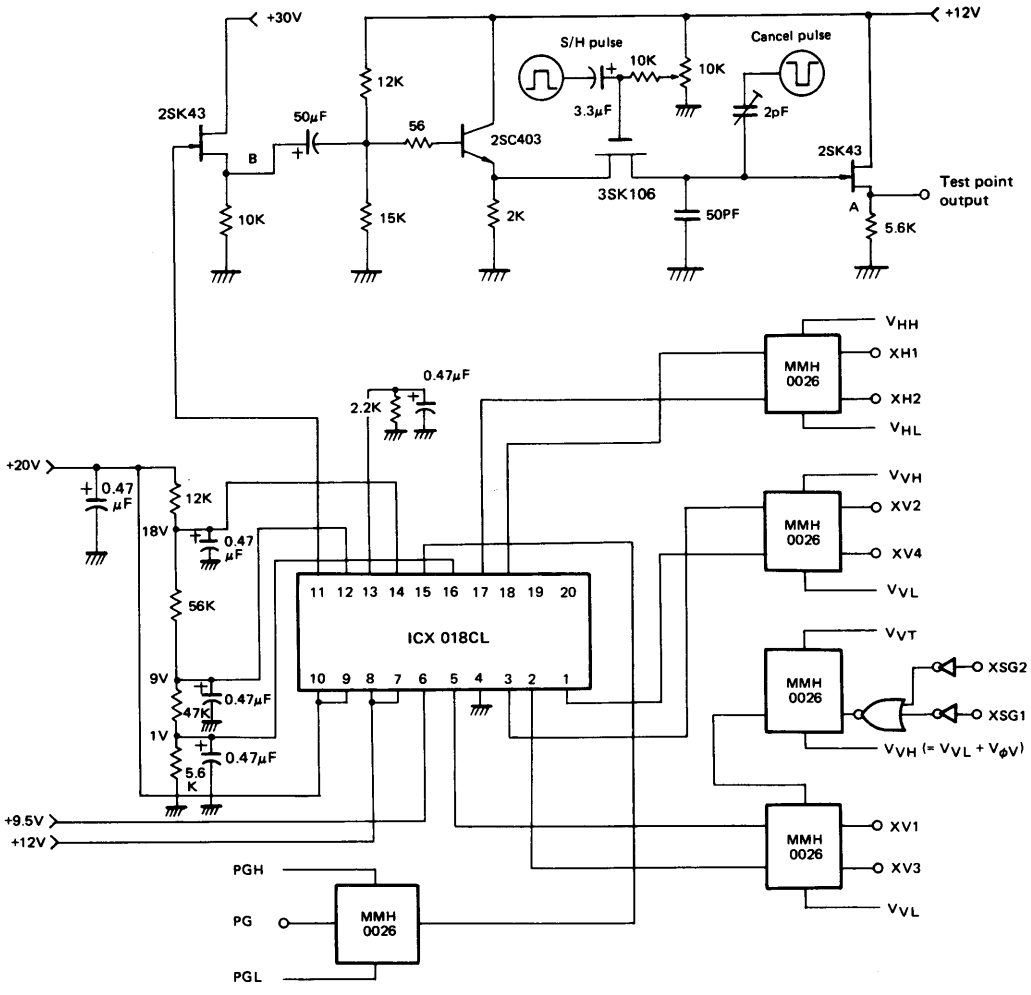
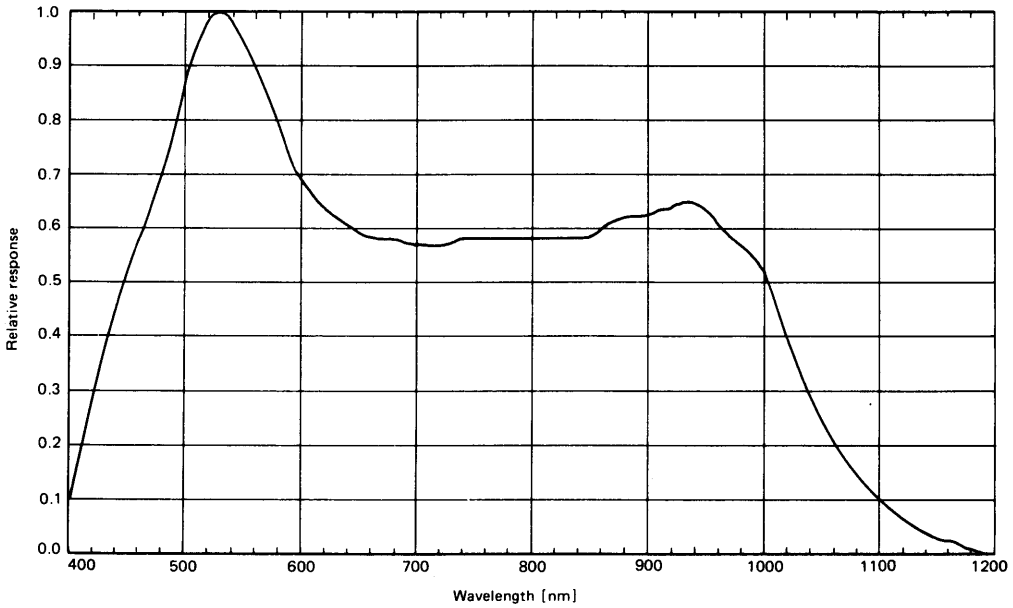


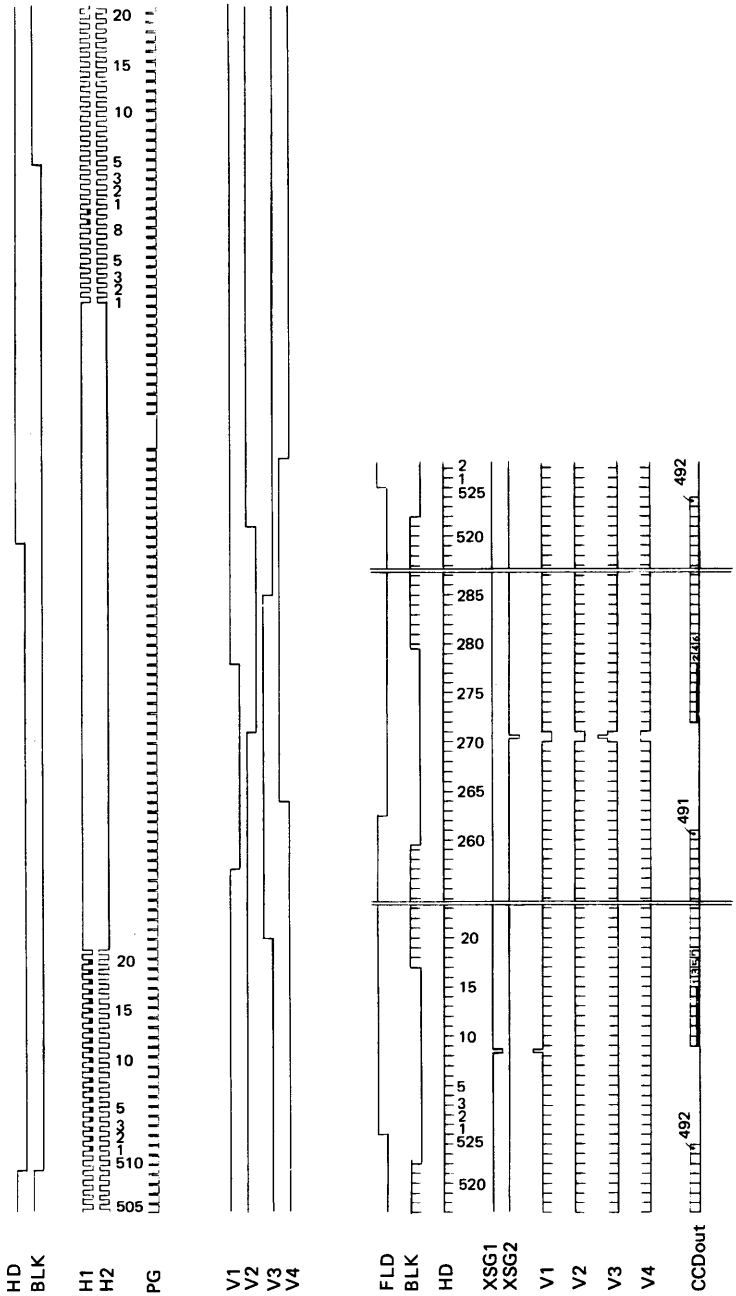
Fig. 9 Test Circuit

Note) XV1 denotes inverted level of V1. The others are the same.

Typical Spectral Response



Timing Chart (EIA)



Notes on Application

1) Electrostatic protection
It is crucial that static discharge be controlled and minimized. Handle most carefully.

2) Soldering
Make sure that the package temperature does not exceed 80°C. Solder dipping in a mounting furnace causes broken glass, filter delamination, and other defects. Use a grounded 30 W soldering iron and solder in less than 2 seconds for each pin. Cool sufficiently when reworking or remounting.

3) Glass surface dust
Do not touch glass plates. Be careful not to have objects contact glass surface. Clean with a cotton bud when the glass surface is stained. Do not use an organic solvent other than ethyl alcohol. Store in a special container to prevent dust and dirt. To prevent dew condensation, preheat or precool when moving to a room in which temperature difference is great.

4) ROM for blemish compensation
This device is shipped in a special container together with ROM. Be most careful about combination when remounting.

5) Care must be taken to avoid exposure to strong light for a long time.

Solid-State Image Device for CCIR B/W TV System

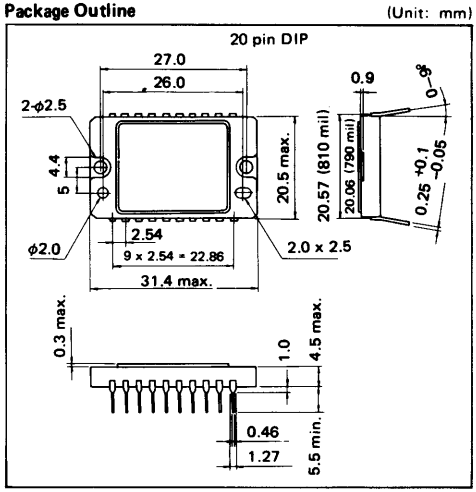
Description

ICX021CL is an interline transfer CCD solid-state imaging device developed for one-chip B/W cameras.

Features

- Number of effective picture elements
  500 (H) x 582 (V)
- Number of optical black elements
  Horizontal (H) direction
  2 picture elements in front
  30 picture elements in back
  Vertical (V) direction
  14 picture elements in front
- High sensitivity
- Low smear
- Anti-blooming
- Low lag, no burning
- Resistance to electro-magnetic field and micro-phonic noise
- Precise image geometry
- γ characteristic: 1

Package Outline (Unit: mm)



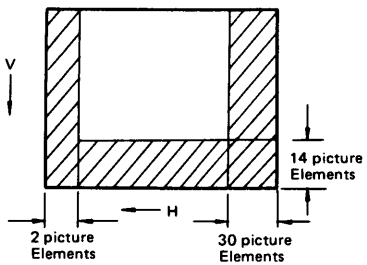


Fig. 1 Layout of Optical Black Elements

Device Organization

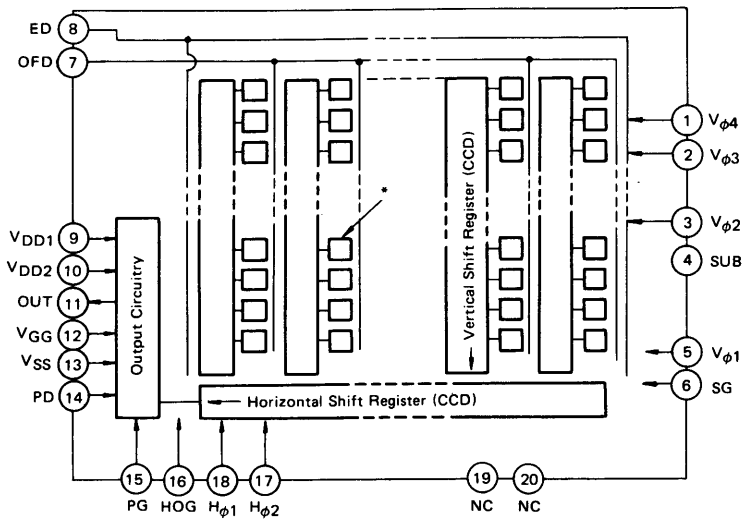
- Interline transfer CCD image sensor
- Unit cell size 17 μm (H) x 11 μm (V)
- Number of dummy bits 8 bits horizontal, 1 bit vertical (even field only)
- Chip size 10.0 mm (H) x 9.3 mm (V)
- Thin polysilicon gate MOS diode sensor using the multi-layer interference effect
- On-chip, high-sensitivity output amplifier
- P-sub, P-well structure

50184A-TO

Absolute Maximum Ratings

• Supply voltages V_{DD1}, V_{DD2}, and V_{PD}	−0.3 to +30V	
• Horizontal and vertical clock pins − SUB	−20 to +20V	
• Between horizontal clocks, between vertical clocks	22V	(SUB = 0V)
• Horizontal and vertical clock pins − Sensor gate	18V	
• Pins other than those listed above	−0.3 to +20V	
• Storage temperature	−30 to +80°C	
• Operating temperature	−10 to +55°C	

Block Diagram



* **Note)** □ : Photosensor

Pin Configuration (Top View)

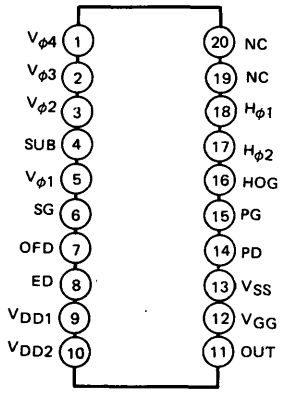


Fig. 2

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock input	11	OUT	Signal output *
2	Vφ3	Vertical register transfer clock input	12	V_{GG}	Output amplifier gate bias *
3	Vφ2	Vertical register transfer clock input	13	V_{SS}	Output amplifier source bias *
4	SUB	Substrate	14	PD	Output reset drain *
5	Vφ1	Vertical register transfer clock input	15	PG	Output reset clock *
6	SG	Sensor gate bias	16	HOG	Horizontal register read out control bias *
7	OFD	Anti-blooming bias *	17	Hφ2	Horizontal register transfer clock input
8	ED	Edge drain bias *	18	Hφ1	Horizontal register transfer clock input
9	V_{DD1}	Power supply *	19	NC	
10	V_{DD2}	Power supply *	20	NC	

* Never supply negative voltage to pins.

DC Bias Conditions

(Some of the characteristics shown below are determined by the recommended circuit in Fig. 4. Refer to Note 1 through 8.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Substrate bias	V_{SUB}		0		V	V_{SUB} = GND
Output circuit supply voltages	V_{DD1}	19	20	21	V	$V_{DD1} = V_{DD2}$
	V_{DD2}	19	20	21	V	
	V_{PD}	17	18.1	19.2	V	Note 1
	V_{SS}	Grounded with 2.2kΩ resistor				Note 2
	V_{GG}		9		V	Note 1
Anti-blooming bias	V_{OFD}	11	12	13	V	Note 3
Edge drain bias	V_{ED}	V_{OFD}				
HOG bias	V_{HOG}	0.8	1.0	1.2	V	
Sensor gate bias	V_{SG}	8.5	9.5	10.5	V	Note 3

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
DC supply current	I_{DD}		3.2	4	mA	Note 4
Input current 1	Iin1			1	μA	Note 5
Input current 2	Iin2			10	μA	Note 6

Clock Voltage Conditions

(Some of the characteristics shown below are determined by the recommended circuit in Fig. 4. Refer to Note 1 through 8.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Read out pulse	V_{VT}	11.0	13.0	14.0	V	Note 3
Vertical transfer clocks						
Low level	V_{VL}	-5.5	-5.0	-4.5	V	Note 3
Amplitude	$V_{\phi V}$	6.8	7.5		V	
Horizontal transfer clocks						
Low level	V_{HL}	-4.4	-4.0	-3.6	V	
High level	V_{HH}	0.8	1.0	4.4	V	Note 7
Amplitude	$V_{\phi H}$	4.75	5.0	8.8	V	Note 7
Output reset clock						
Low level	V_{PGL}	1.0	1.3	1.7	V	Note 8
High level	V_{PGH}	8.9	9.3	10.5	V	
Amplitude	$V_{\phi PG}$	7.2	8.0	8.8	V	

Clock Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical transfer clock vs. GND	$C_{\phi V}$		6200		pF	
Between vertical transfer clocks	$C_{\phi VV}$		1800		pF	
Output reset clock	$C_{\phi PG}$		14		pF	

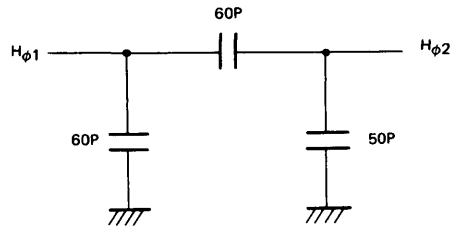


Fig. 3 Horizontal Transfer Clock Equivalent Circuit

Note) 1. V_{PD}, V_{GG}, and V_{HOG} should be produced from V_{DD1} and V_{DD2}. Resistance precision should be ±5%. See Figs. 4 and 5.

2. V_{SS} should be self-biased and should be connected to GND through a 2.2kΩ (±5%) resistor.

3. $V_{VHH} + 5.1 \leqq V_{SG} \leqq V_{VT} - 1.5$ $\quad V_{VT} \leqq V_{OFD} + 2$ (Unit: V)
   V_{VHH} is the maximum level of the waveforms containing couplings of vertical transfer clocks $V_{\phi 1}$ to $V_{\phi 4}$ excluding the period in which a three level VT is pulsed.

4. Total output amp current, when the load resistance is 2.2kΩ.

5. The current to the substrate when 20V is sequentially applied to Pins $V_{\phi 1}$, $V_{\phi 2}$, $V_{\phi 3}$, $V_{\phi 4}$, $H_{\phi 1}$, and $H_{\phi 2}$.

6. The current to the substrate when 20V is applied to SG, ED, OFD, PD, HOG, TP1, and TP2 independently. The pins which have not been measured should be connected to the ground.

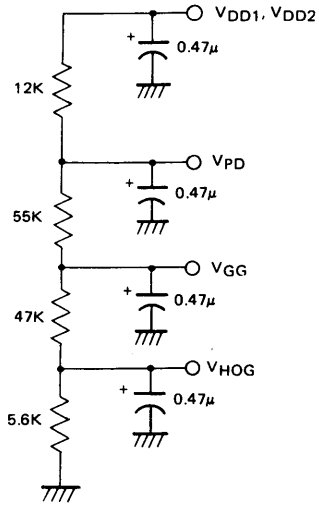
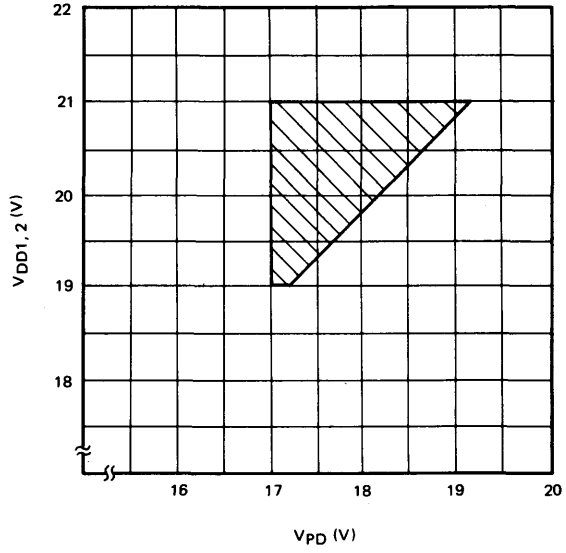


Fig. 4 Recommended Circuit for Bias Setting of V_{DD1}, V_{DD2}, V_{PD}, V_{GG}, and V_{HOG}



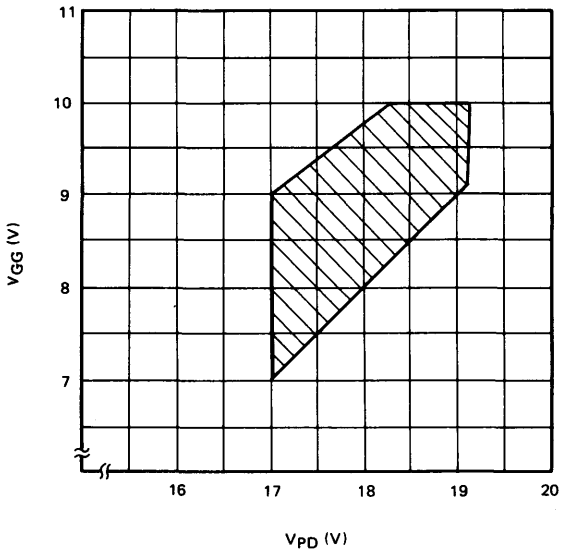


Fig. 5 Bias Setting Range of V_{DD1}, V_{DD2}, V_{PD}, and V_{GG}

The shaded section is the recommended operating range.

Note) 7 V_{HH}, $V_{\phi H}$, and V_{HL} are determined as follows.

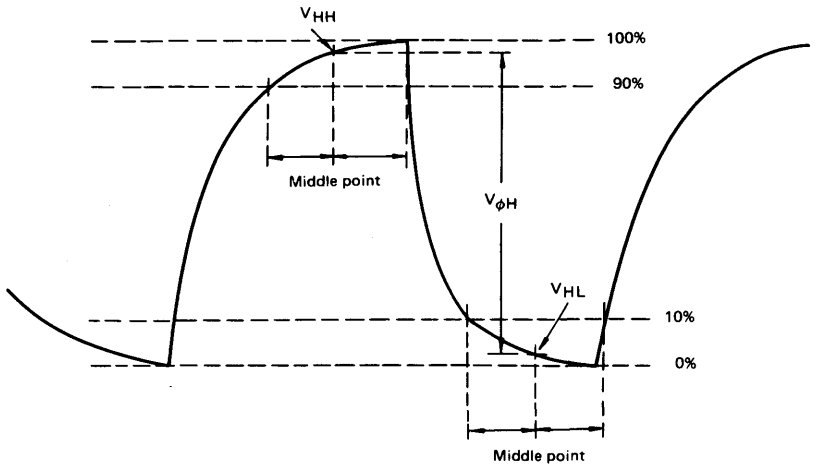


Fig. 6 Horizontal Transfer Clock Waveform

8 V_{PGL}, V_{PGH}, and $V_{\phi PG}$ are determined as follows.

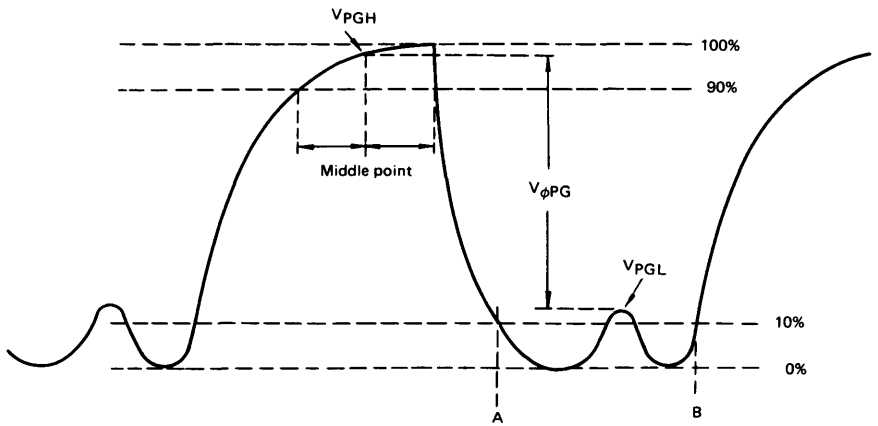


Fig. 7 Output Reset Clock Waveform.

V_{PGL} is defined by the maximum level between Points A and B. Be careful not to allow ringing on the low side to be less than 0V.

Drive Pulse Waveform Conditions

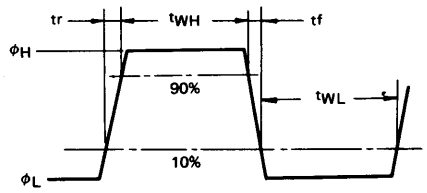


Fig. 8 Pulse Waveform

Symbol	tWH			tWL			tr			tf			Unit	Condition
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$H_{\phi1}$		43			43			10			10		ns	During scanning time
$H_{\phi2}$		43			43			10			10			
$H_{\phi1}$		6.87						0.01			0.01		μs	During parallel-serial conversion
$H_{\phi2}$		0						0			0			
PG	10	43			43			10			10		ns	Normally PG = $H_{\phi1}$
$V_{\phi1}/V_{\phi2}$		61.8			2.12			0.1			0.1	0.5	μs	During scanning time
$V_{\phi3}/V_{\phi4}$		3.64			60.2			0.1			0.1	0.5		
$V_{\phi1}/V_{\phi3}$		19.2						1			1			During read out from sensor

Operating Characteristics

Ta = 25°C See the Test Circuit.

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Condition
Sensitivity	S		130		mV	1	
Saturation Output Voltage	V_{sat}	360	440	850	mV	2	
Video Signal Shading	SV1		11	20	%	3	
Smear	SM		0.01	0.04	%	4	
Dark Signal	Vdt			13	mV	5	Ta = 55°C
Dark Signal Shading	ΔVdt			4	mV	6	Ta = 55°C

Test Method

○ Test conditions

1) The device drive conditions in the following measurements should be adjusted to the typical values of the DC and clock voltage conditions. (See Fig. 9.)
2) In measurements mentioned below, blemishes should be excluded. Unless specified, the optical black level should be the reference for the signal output, and the value measured at Point B in Fig. 9 should be used.

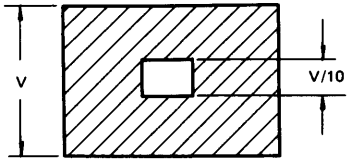
○ Definition of standard imaging condition

1) Standard imaging condition 1: Use pattern box (Brightness 706 nt. 3200°K Halogen source) at F8 with FUJINON lens H6 x 12.5D (F1.4). CM-500S (1.0mmt) should be used as an IR cut filter.
2) Standard imaging condition 2: Uniformity of a light source within 2%. The light-source color temperature should be 3200°K, and CM-500S (1.0 mmt) should be used as an IR cut filter. The quantity of light should be adjusted to the average value of output voltage Vs shown in each item.

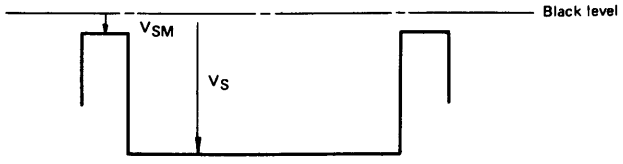
1. Set to the standard imaging condition 1 and measure output signal in the center of the screen.
2. Set to the standard imaging condition 2, adjust the intensity of light, check anti-blooming, then measure the minimum value of signal for the whole screen.
3. After setting up standard imaging condition 2, set the pattern box on the entire screen and measure the maximum and minimum output voltages of Channel (Vmax, Vmin) adjusting Vs to 300 mV.

$$SV_1 \equiv \frac{Vmax - Vmin}{Vs} \times 100(\%)$$

4. After setting up standard imaging condition 2, set the pattern box on a vertical 1/10 screen. Measure the average signal voltage Vs and maximum value V_{SM} during vertical blanking. (Vs = 300 mV, 1/10 V method)



$$SM \equiv \frac{V_{SM}}{V_S} \times 100\ (\%)$$



5. Average dark signal at ambient temperature of 55°C.
6. Measure maximum and minimum dark signal (Vdmax, Vdmin). Blemishes should be excluded. The temperature should be 55°C.

$$\Delta Vdt \equiv (Vdmax - Vdmin)$$

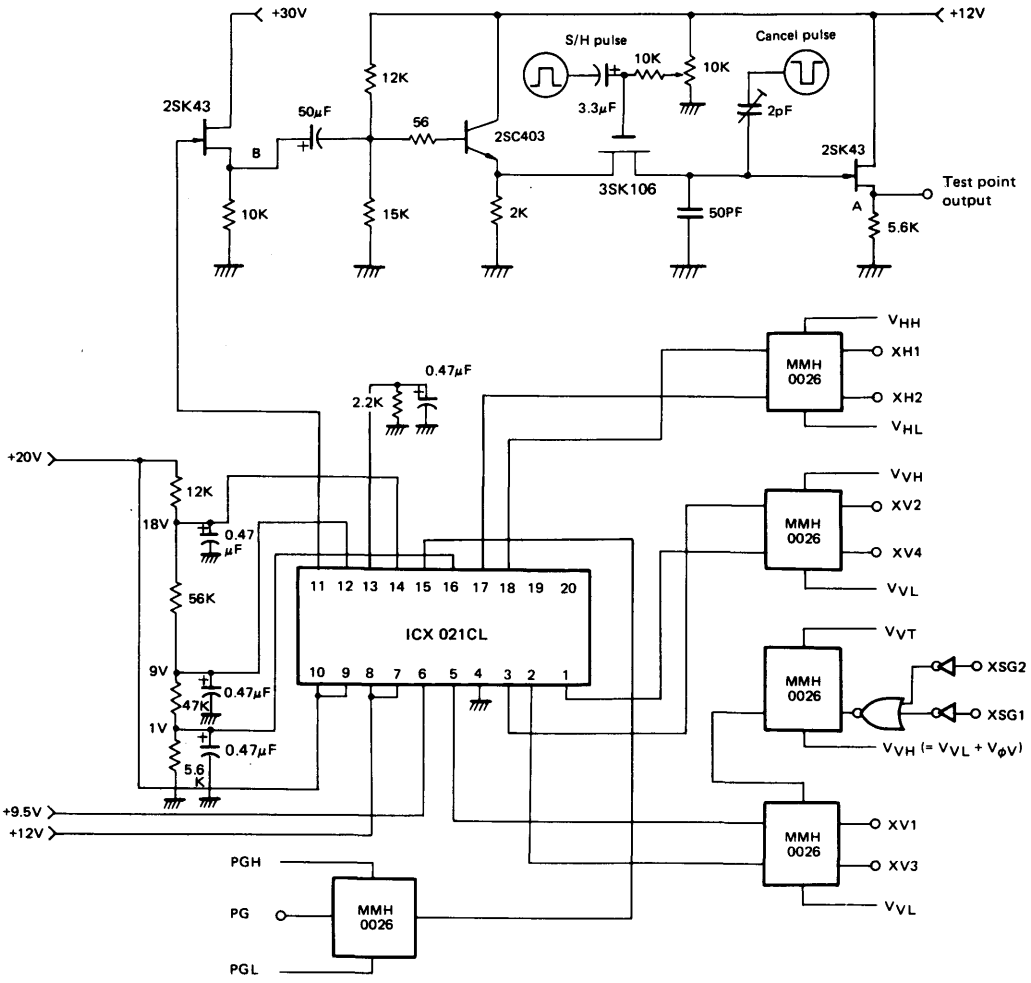
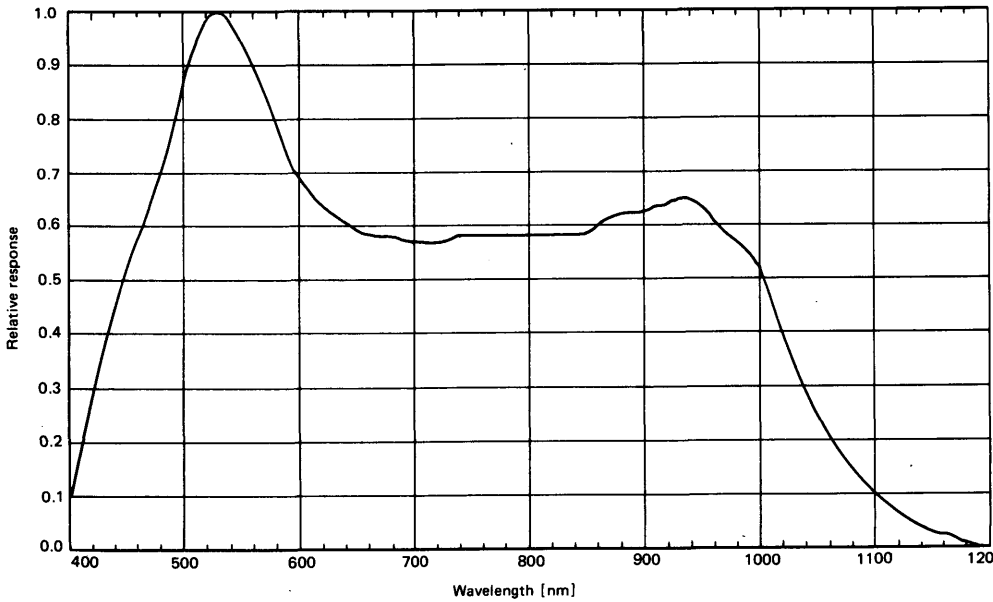


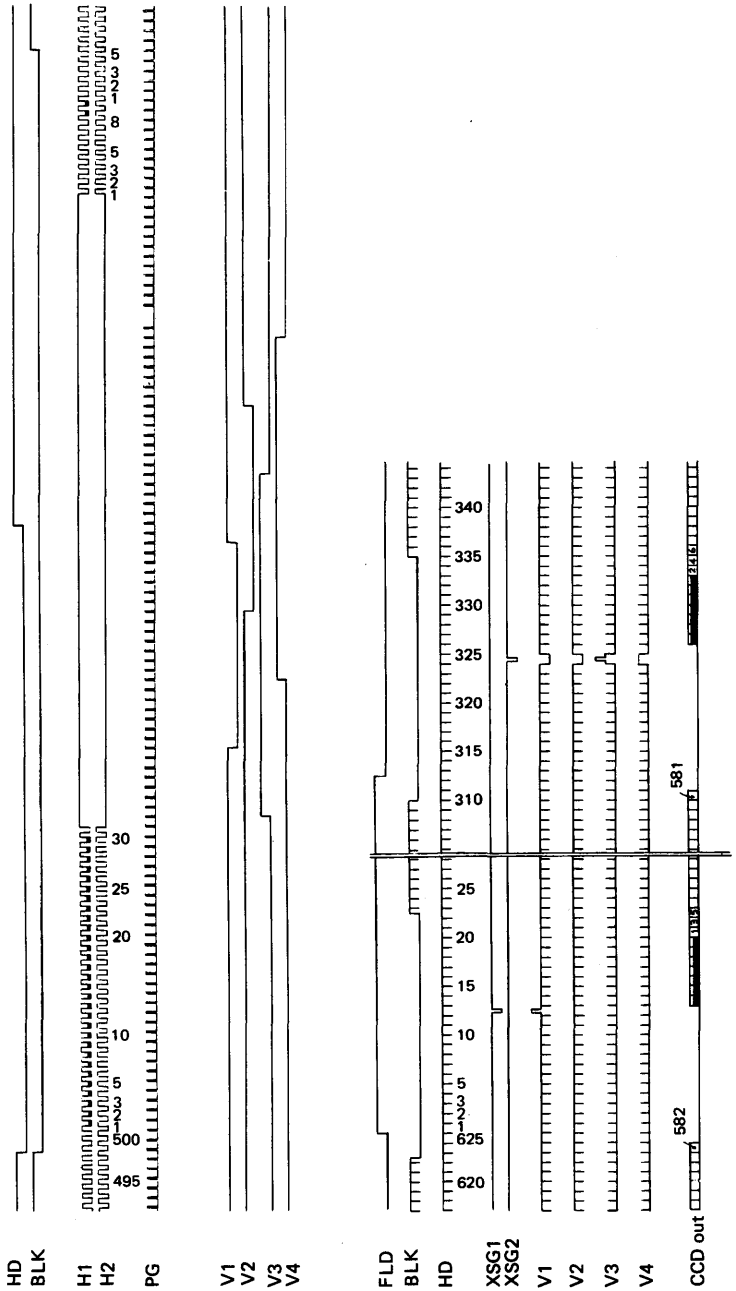
Fig. 9 Test Circuit

Note) XV1 denotes inverted level of V1. The others are the same.

Typical Spectral Response



Timing Chart (CCIR)



Notes on Application

1) Electrostatic protection
It is crucial that static discharge be controlled and minimized. Handle most carefully.

2) Soldering
Make sure that the package temperature does not exceed 80°C. Solder dipping in a mounting furnace causes broken glass, filter delamination, and other defects. Use a grounded 30 W soldering iron and solder in less than 2 seconds for each pin. Cool sufficiently when reworking or remounting.

3) Glass surface dust
Do not touch glass plates. Be careful not to have objects contact glass surface. Clean with a cotton bud when the glass surface is stained. Do not use an organic solvent other than ethyl alcohol. Store in a special container to prevent dust and dirt. To prevent dew condensation, preheat or precool when moving to a room in which temperature difference is great.

4) ROM for blemish compensation
This device is shipped in a special container together with ROM. Be most careful about combination when remounting.

5) Care must be taken to avoid exposure to strong light for a long time.

Interline-type CCD Image Sensor

Description

ICX022AL-3 is an interline-type CCD image sensor designed for B/W video cameras.

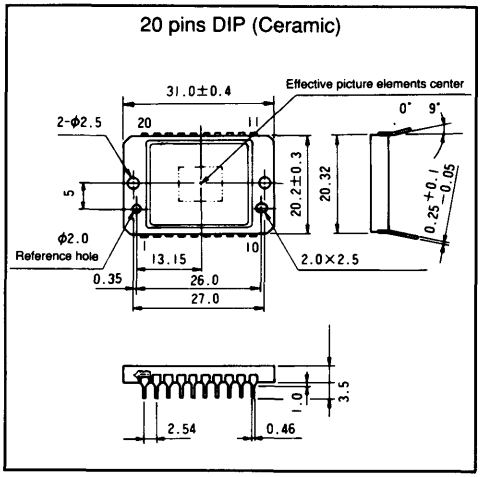
Effective pixels number 768 horizontally and 493 vertically.

Features

- Image size: 2/3 inches (8.8 mm(H) x 6.6 mm(V))
- Effective pixels: 768 (H) x 493 (V)
- Effective optical black
  - Horizontal: Front 5 pixels
    Back 45 pixels
  - Vertical: Front 16 pixels
    Back 4 pixels
- High resolution, high sensitivity and low noise.
- Low lag and low smear
- Low dark current
- Anti-blooming function
- Electronic shutter function
- Neither figure distortion nor microphonic noise.
- γ characteristics: 1

Package Outline

Unit: mm



Element Structure

- Interline type CCD image sensor
- Chip size: 10.0 mm(H) x 8.2 mm(V)
- Unit cell size: 11.0 μm(H) x 13.0 μm(V)
- Dummy bits: horizontal 22-bits, vertical 1-bit (even fields only)
- Built-in high-sensitivity output amplifier

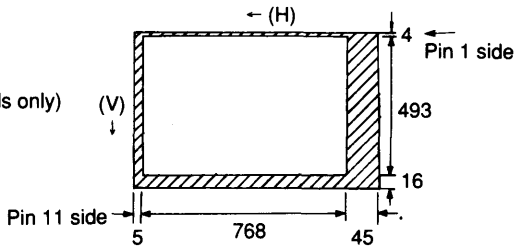
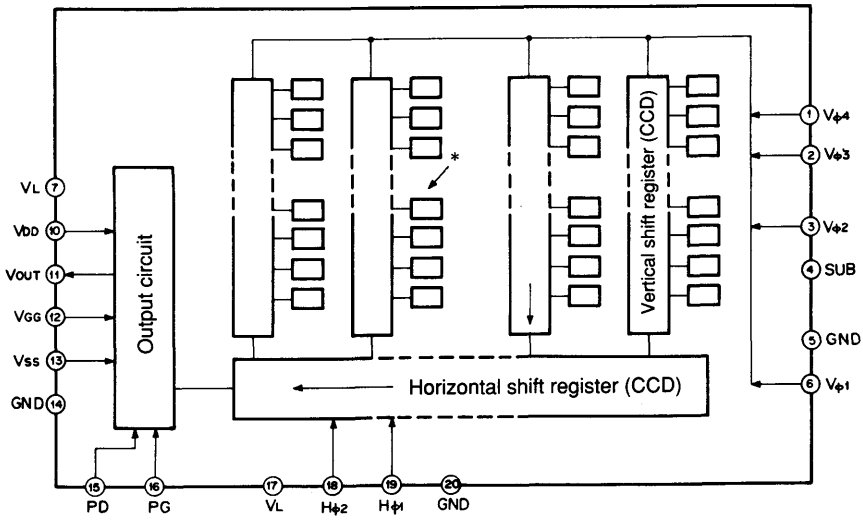


Fig. 1 Optical block configuration

Imaging Device Function Block and Pin Configuration



*Note) —□— : Photo sensor

Pin Description

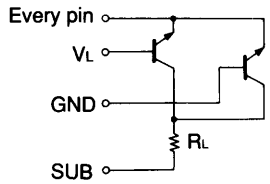
No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	Vφ1	Vertical register transfer clock	16	PG	Output reset clock
7	VL	Protective transistor bias	17	VL	Protective transistor bias
8	NC		18	Hφ2	Horizontal register transfer clock
9	NC		19	Hφ1	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB - GND	-0.3 to +55	V	
V_{DD}, PD, V_{OUT}, V_{SS} - GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS} - SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - - GND	-15 to +20	V	
Horizontal and vertical transfer clock inputs - - SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	15	V	Note 2
Potential difference between horizontal transfer clock inputs	17	V	
Hφ1, Hφ2 - Vφ4	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	
PG, V_{GG} - SUB	-55 to +10	V	Note 1
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L - V_L	-0.3 to +27	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This image sensor consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V. The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5 kΩ between V_{SS} or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5kΩ.

1) V_{DD}, PD, V_{OUT} and V_{SS} pins



2) Pins other than 1) (except V_L and GND)

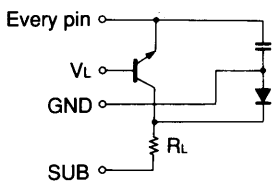


Fig. 2 Equivalent circuit

2. In case of clock width <10 μs and clock duty factor <0.1%, up to 27 V is guaranteed.

Electrical Characteristics
Bias conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	Note 1
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5%
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	-3		3	%	
Protection transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.
V_{SUB} code – Two digit indication

□ ↑ Integral part □ ↑ Decimal part

The integral code correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Numerical value	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground V_{SS} with a 390 Ω resistance

4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
2) Current flowing to the ground when a voltage of 20 V is applied to Vφ1, Vφ2, Vφ3, Vφ4, Hφ1 and Hφ2 pins in the order. Apply pin a voltage of 20 V to the SUB pins and ground pins other than those under test.
3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.

5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.

Clock Voltage Conditions
Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.5		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-10.5			V	
Horizontal transfer clock voltage	V_{HHH}			5.5	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	

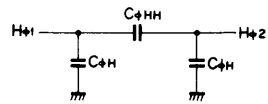


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("Vφ1" and "Vφ2") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tst/2" are expressed as "V_{T1}" (at Vφ1) and "V_{T3}" (at Vφ3). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

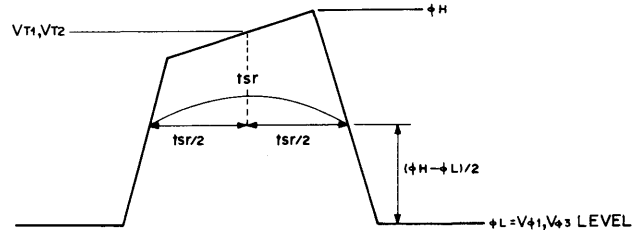


Fig. 5 Read clock wave length

2. Vertical clock voltage (Refer to Fig. 6)
T = 559 ns (with a horizontal driving frequency of 14.32MHz)

1) Definition of the vertical transfer clock amplitude
Level 2T after the rising edge of "Vφ3" is expressed as "V_{3A}".
Level T after the falling edge of "Vφ1" is expressed as "V_{1B}".
Level 2T after the rising edge of "Vφ4" is expressed as "V_{4A}".
Level T after the falling edge of "Vφ2" is expressed as "V_{2B}".
Level 2T after the rising edge of "Vφ1" is expressed as "V_{1A}".
Level T after the falling edge of "Vφ3" is expressed as "V_{3B}".
Level 4T after the rising edge of "Vφ2" is expressed as "V_{2A}".
Level 3T after the falling edge of "Vφ4" is expressed as "V_{4B}".

Vφ2 Level T after the falling edge of "Vφ1" is expressed as "V_{2C}".
Vφ3 Level T after the falling edge of "Vφ2" is expressed as "V_{3C}".
Vφ4 Level T after the falling edge of "Vφ3" is expressed as "V_{4C}".
Vφ1 Level 3T after the falling edge of "Vφ4" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in Vφ1 and Vφ3 only).

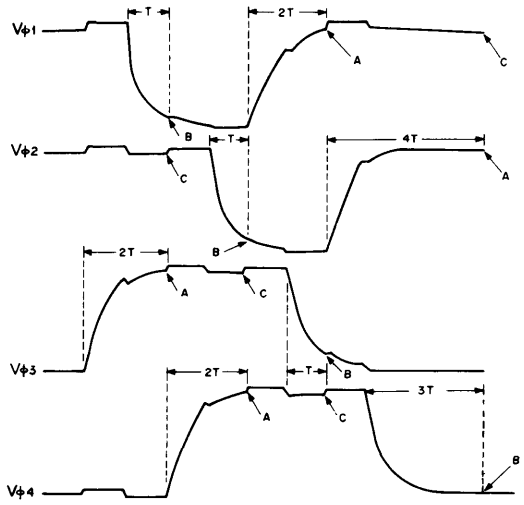


Fig. 6 Vertical transfer clock waveform
T = 559ns (with a horizontal driving frequency of 14.32 MHz)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".

   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
   And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10ns, thh ≥ 10ns, tho ≥ 5ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

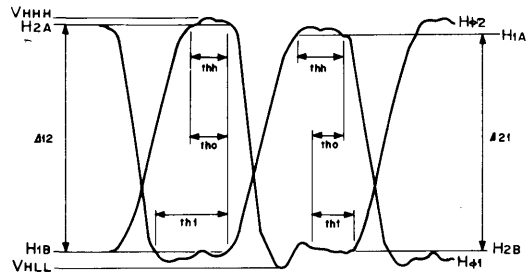


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

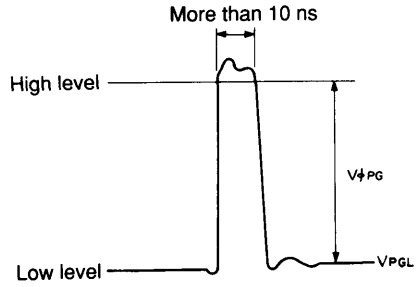


Fig. 8 Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as ϕ_L and the maximum value of the substrate clock waveform as ϕ_H.
   2) The period during which voltage level reaches (ϕ_H – ϕ_L)/2 is expressed as tsr. The difference of voltage level with ϕL at tsr/2 is defined as substrate clock voltage $V\phi_{SUB}$.

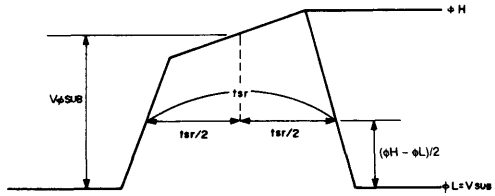


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1) Definition of ϕ_H (100%) and ϕ_L (0%)
   (1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock (PGϕ) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   (2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_3$) is applied.
   (3) For the substrate clock (SUBϕ), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".
2) Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.32MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
Hφ1	18	33.7	10	8	ns	Imaging period
Hφ2	18	33.7	10	8		
Hφ1	4.9		0.10	0.01	μs	Parallel-serial converting period
Hφ2		4.9	0.10	0.01		
φPG	12	53.7	2	2	ns	
Vφ1/Vφ2	61.6	1.6	0.1	0.1	μs	Imaging period
Vφ3/Vφ4	2.8	60.45	0.05	0.1		
VφT	2.4		0.2	0.1		Reading period
SUBφ	1.0		0.08	0.1	μs	Electron sweep-off period

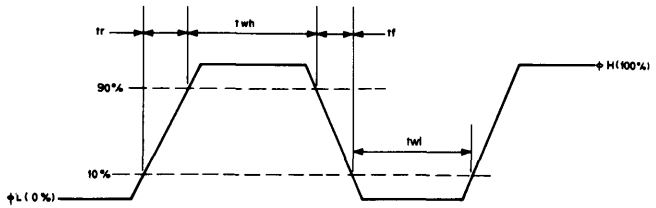


Fig. 10 Clock waveform

Imaging Characteristics

(For the testing circuit, see Fig. 11.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sg	140	190		mV	1	
Output saturation signal	Vsat	600			mV	2	Note
Blooming margin		1000			times	3	Note
Smear	Smr		0.007	0.015	%	4	
Video signal shading	Svg			25	%	5	
Dark signal output	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C

Note) Saturation signal and blooming margin are guaranteed only when the substrate voltage has been set to the voltage indicated on the back of the imaging device.

Test Methods

Conditions

1) The conditions required to drive the device through the following tests are converted by the bias conditions and the clock voltage conditions. The test circuit shown in Fig. 11 is used for evaluating and testing the characteristics.
2) Blemish are excluded from the following tests and the signal output is based on the optical black level unless otherwise specified. The value obtained at the output test point becomes the test value.

Standard imaging conditions

1) Shoot the PTB-100 pattern box (luminance 706 Nit, color temperature 3200°K) with no pattern, using a FUJINON H6 × 12.5D (F1.4) lens at F5.6. Use the CM-500S (1.0 mmt) filter to cut off infrared rays.
2) Shoot a light source (color temperature 3200°K) which provides a uniform brightness within 2% over the whole screen.
   For infrared cut-off filter, use the CM-500S (1.0 mmt)

1. Set the standard imaging condition 1) and test signal voltages the center of the screen.

2. Set to standard imaging condition 2) and adjust the light intensity to about ten times the intensity obtained at a signal voltage of 200 mV. Then obtain the minimum value of the signal voltage over the whole screen.

3. Set to imaging condition 2) and adjust the light intensity to about 1000 times the intensity obtained at a signal voltage of 200 mV. At that time make sure there is no blooming and the vertical resistor is not saturated.

4. Set to standard imaging condition 2) and adjust the light intensity so that the signal voltage (V_{SG}) becomes 200 mV. Then, turn V_T off and obtain the maximum value of the signal voltage "V_{SM}" after stopping the horizontal resistor 50 H at the effective picture element.

$$Smr = \frac{V_{SM}}{V_{SG}} \times \frac{1}{50} \times \frac{1}{10} \times 100\ (\%)$$

(Converted into 1/10 V system)

5. Set to standard imaging condition 2) and test the signal voltage to obtain maximum (V_G max) and minimum (V_G min) values.
   The light intensity is adjusted so that the average value of the signal voltage (V_G average) becomes about 200 mV.

$$Svg = \frac{V_{SG}max - V_{SG}min}{V_{SG}\ average} \times 100\ (\%)$$

6. Measure the mean voltage of the dark current signal based on the horizontal free-transfer level in a light-shaded condition with an ambient temperature of 55°C.

7. Following measurement 6, test the dark current signal voltage to obtain the maximum (Vdmax) and minimum (Vdmin) values. Spot defects are ignored in this test.

Electrical Characteristics Test Circuit

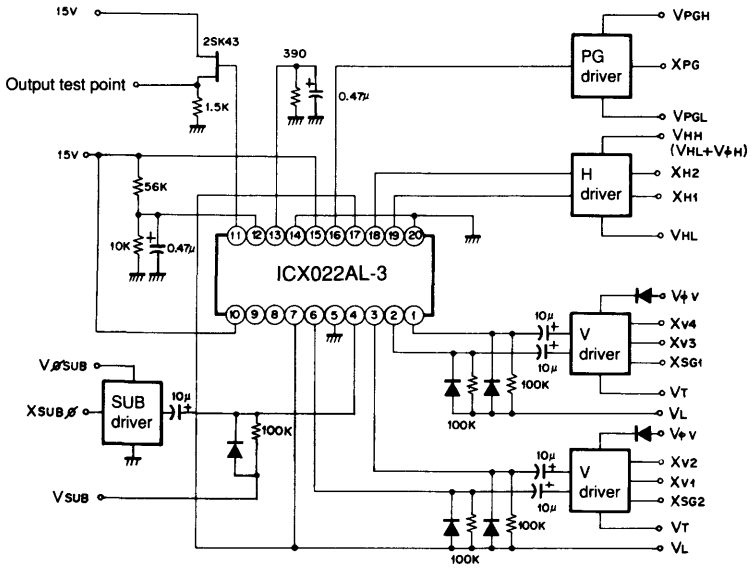
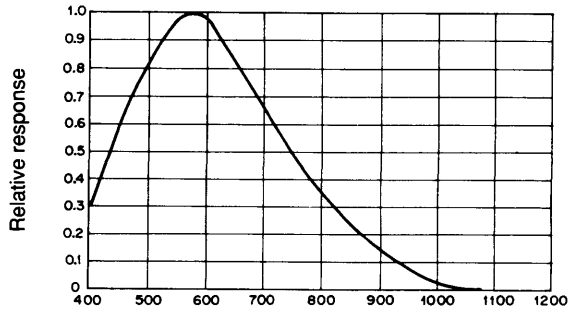


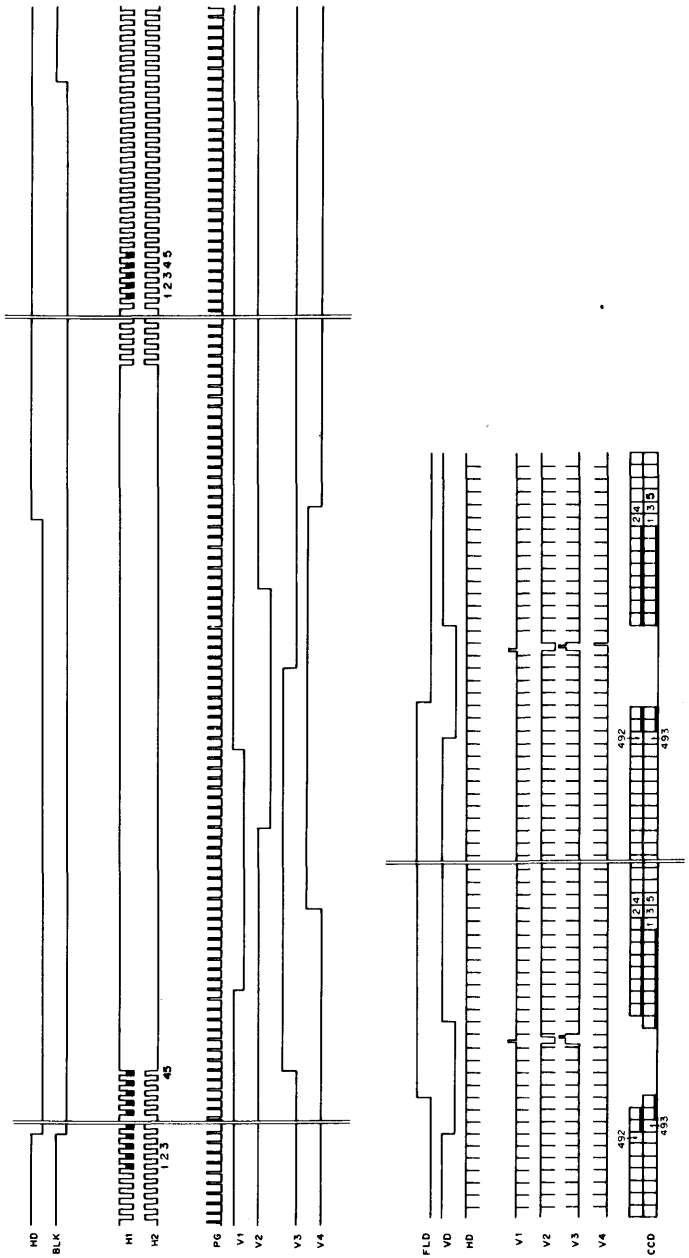
Fig. 11

Spectrum Sensitivity Characteristics (Typical example, excluding illuminant characteristics)

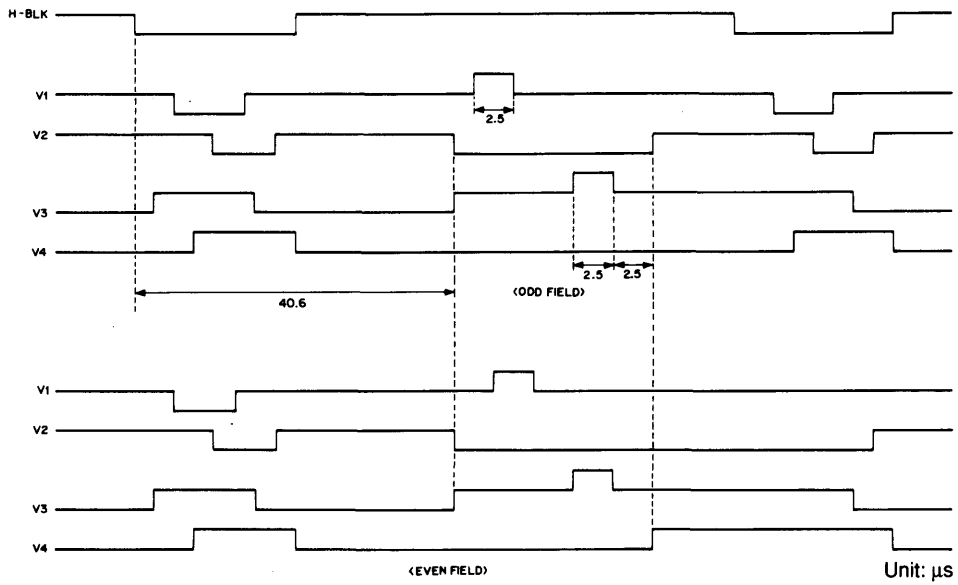
With a Fujinon lens H6 x 12.5D



Driving Pulse Timing Chart

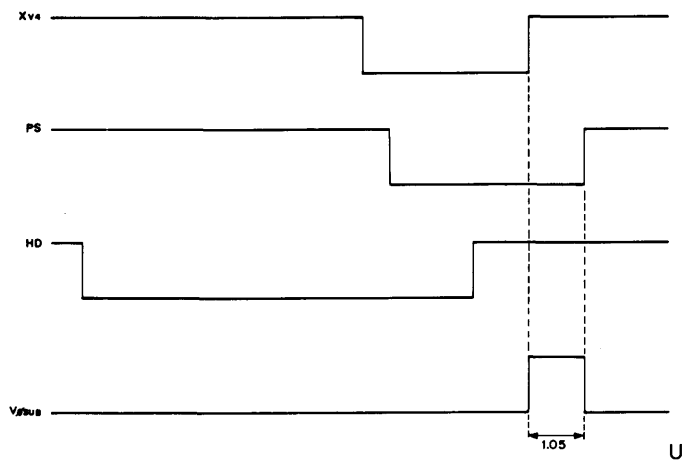


Sensor Read Clock Timing Chart



Unit: µs

Charge Drain Clock Timing Chart



Unit: µs

Handling Instructions

1. On electric screening
   To prevent damage to the CCD image sensor by static electricity, handle as follows.
   a) Either handle the device with bare hands, or use antistatic gloves and clothes. Conductive shoes are also required.
   b) Use a ground lead when directly touching the device.
   c) Cover the floor and working table with a conductive mat or equivalent to avoid static electricity.
   d) Discharge using ionized air is recommended.
   e) To ship the mounted boards, use cartons with antistatic properties.

2. On soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder-dipping of DIP in a mounting furnace may break glass. Use a grounded 30 W soldering iron a each pin for less than 2 seconds. When adjusting or removing soldered parts, let the CCD cool sufficiently.
   c) Do not use any solder-aspirating equipment to remove the imaging device. Should an electric solder-aspiration device be used, use only a device of the zero-cross type control system and be sure to ground the controller.

3. On contamination
   a) Keep the operation room clean (Class 1000 Will be expected).
   b) Do not touch the glass surface avoid contact with foreign objects. Blow off any dust the surface with a blower. (Ionized air is recommended to blow off any object sticking through static electricity.)
   c) Wipe off grass spots with an applicator moistened with ethanol. Be careful not to scratch the surface.
   d) To eliminate contamination, store the device in an exclusive case. During transportation minimize the difference in temperatures between locations to avoid moisture condensation.
   e) When a protection tape has been affixed for shipment, remove it just before use after applying appropriate antistatic measures. Do no reuse the removed tape.

4. Do not subject the device to light sources for extended periods. If a color element is subjected to strong light ray for an extended period, the color filter will be discolored. (Store the device in a dark place.)

5. Usage or storage of the device in high temperature or high humidity may seriously affect the performance.

6. The CCD image sensor is a high-precision optical part, that should not be subjected to mechanical shocks.

7. System data write complete ROM (with flow compensation address included)
   System data write complete ROM in equal quantity as ICX022AL-3 is attached.
   Analog those ROM with address for flow compensation have serial No. stuck on.
   Use in conjunction with ICX022AL-3 pairing the same serial No..

Interline-type CCD Image Sensor

Description

ICX024AL-3 is an interline-type CCD image sensor designed for B/W video cameras.

Effective pixels number 756 horizontally and 581 vertically.

Features

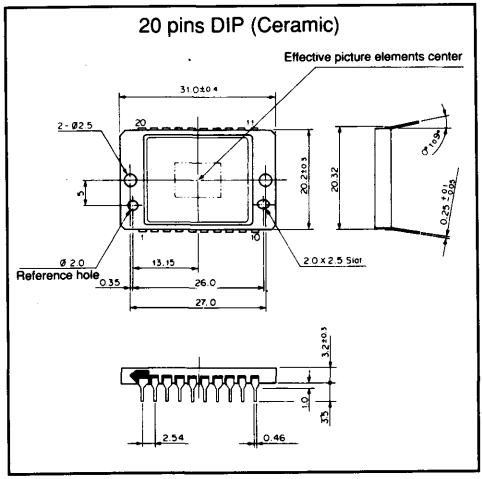
- Image size: 2/3 inches (8.8 mm(H) x 6.6 mm(V))
- Effective pixels : 756 (H) x 581 (V)
- Effective optical black
  Horizontal: Front 5 pixels
  Back 55 pixels
  Vertical: Front 19 pixels
  Back 6 pixels
- High resolution, high sensitivity and low noise.
- Low lag and low smear
- Low dark current
- Anti-blooming function
- Electronic shutter function
- Neither figure distortion nor microphonic noise.
- γ characteristics: 1

Element Structure

- Interline type CCD image sensor
- Chip size: 10.0 mm(H) x 8.2 mm(V)
- Unit cell size: 11.0 µm(H) x 11.0 µm(V)
- Dummy bits: horizontal 22-bits, vertical 1-bit (even fields only)
- Built-in high-sensitivity output amplifier

Package Outline

Unit: mm



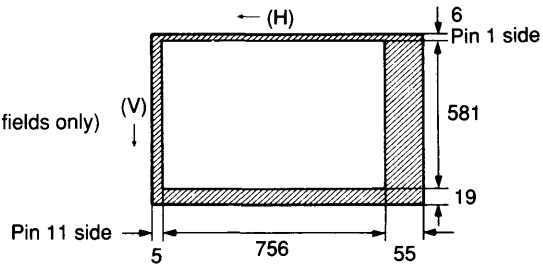
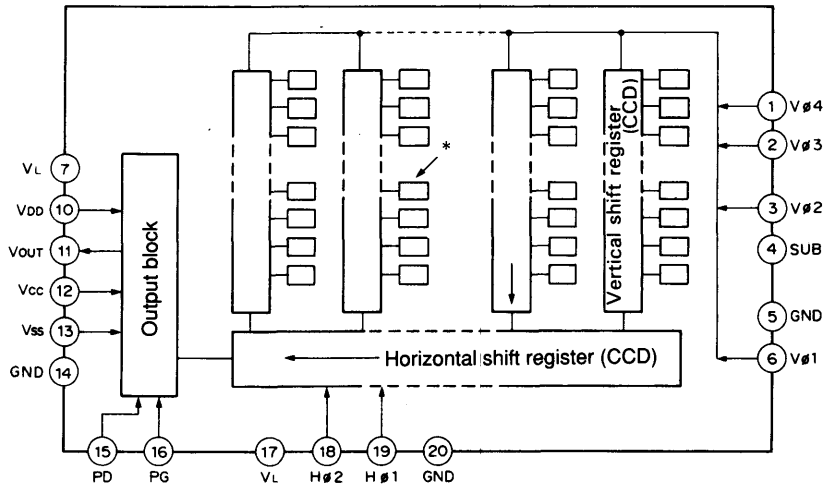


Fig. 1 Optical block configuration

Imaging Device Function Block and Pin Configuration



*Note) —□—: Photo sensor

Pin Description

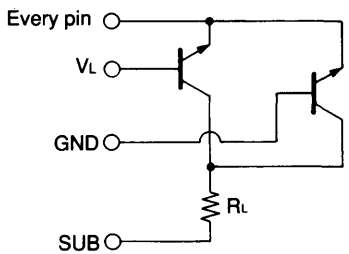
No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate
3	Vφ2	Vertical register transfer clock	13	VSS	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	Vφ1	Vertical register transfer clock	16	PG	Output reset clock
7	VL	Protective transistor bias	17	VL	Protective transistor bias
8	NC		18	Hφ2	Horizontal register transfer clock
9	NC		19	Hφ1	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB - GND	-0.3 to +5.5	V	
V_{DD}, PD, V_{OUT}, V_{SS} - GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS} - SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - GND	-15 to +20	V	
Horizontal and vertical transfer clock input - SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	15	V	Note 2
Potential difference between horizontal transfer clock inputs	17	V	
Hφ1, Hφ2 - Vφ4	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	
PG, V_{GG} - SUB	-55 to +10	V	Note 1
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L - V_L	-0.3 to +27	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This image sensor consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V. The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5 kΩ between V_{SS} or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5 Ω.

1) V_{DD}, PD, V_{OUT} and V_{SS} pins



2) Pins other than 1) (except V_L and GND)

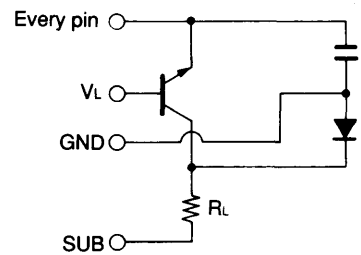


Fig. 2 Equivalent circuit

2. In case of clock width <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Electrical Characteristics

Bias conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5%
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	−3		3	%	
Protection transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.
V_{SUB} code – Two digit indication

□ □
↑ ↑
Integral part Decimal part

The integral code correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Numerical value	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground V_{SS} with a 390 Ω resistance

4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
2) Current flowing to the ground when a voltage of 20 V is applied to Vφ1, Vφ2, Vφ3, Vφ4, Hφ1 and Hφ2 pins in the order. Apply pin a voltage of 20 V to the SUB pins and ground pins other than those under test.
3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.

5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.

Clock Voltage Conditions

Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	−0.5		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	−10.5			V	
Horizontal transfer clock voltage	V_{HHH}			5.2	V	Note 3
	V_{HL}	−3.0		−1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	−3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	

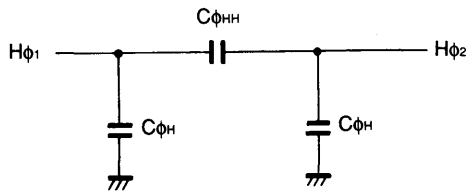


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("Vϕ1" and "Vϕ2") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes (ϕ_H – ϕ_L)/2 is expressed as "tsr". The voltage levels at "tst/2" are expressed as "V_{T1}" (at Vϕ1) and "V_{T3}" (at Vϕ3). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

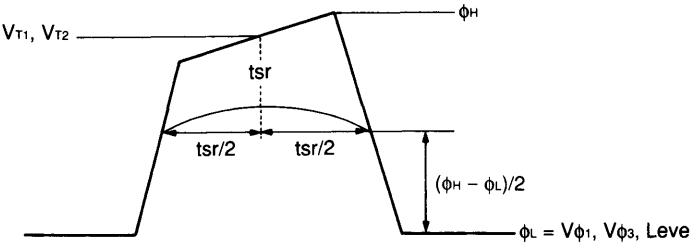


Fig. 5 Read clock wave length

2. Vertical clock voltage (Refer to Fig. 6)
T = 564 ns (with a horizontal driving frequency of 14.19MHz)

1) Definition of the vertical transfer clock amplitude
Level 2T after the rising edge of "Vϕ_3" is expressed as "V_{3A}".
Level T after the falling edge of "Vϕ_1" is expressed as "V_{1B}".
Level 2T after the rising edge of "Vϕ_4" is expressed as "V_{4A}".
Level T after the falling edge of "Vϕ_2" is expressed as "V_{2B}".
Level 2T after the rising edge of "Vϕ_1" is expressed as "V_{1A}".
Level T after the falling edge of "Vϕ_3" is expressed as "V_{3B}".
Level 4T after the rising edge of "Vϕ_2" is expressed as "V_{2A}".
Level 3T after the falling edge of "Vϕ_4" is expressed as "V_{4B}".

Vϕ_2 Level T after the falling edge of "Vϕ_1" is expressed as "V_{2C}".
Vϕ_3 Level T after the falling edge of "Vϕ_2" is expressed as "V_{3C}".
Vϕ_4 Level T after the falling edge of "Vϕ_3" is expressed as "V_{4C}".
Vϕ_1 Level 3T after the falling edge of "Vϕ_4" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "Vϕ_V".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}".
"V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in Vϕ_1 and Vϕ_3 only).

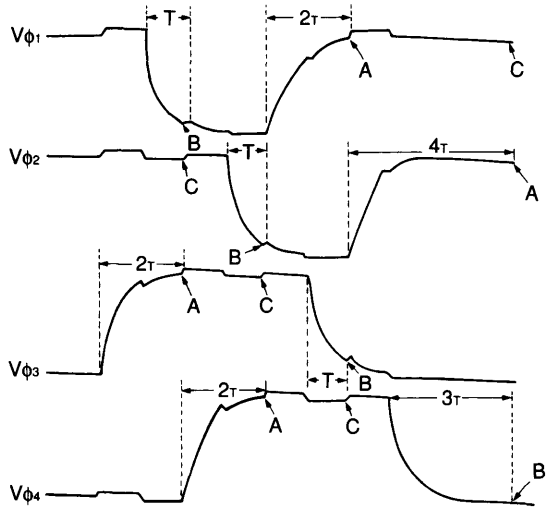


Fig. 6 Vertical transfer clock waveform
T = 564ns (with a horizontal driving frequency of 4 fsc)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".

   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
   And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

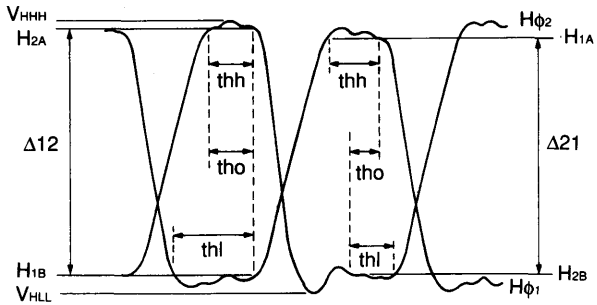


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

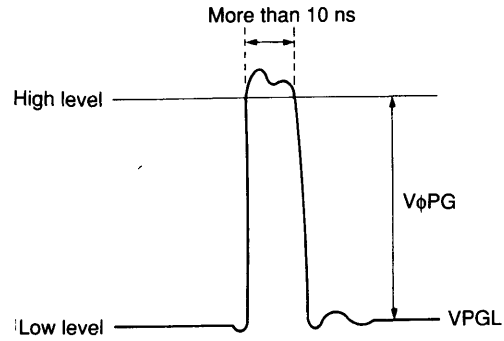


Fig. 8 Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as ϕ_L and the maximum value of the substrate clock waveform as ϕ_H.
   2) The period during which voltage level reaches $(\phi_H - \phi_L)/2$ is expressed as tsr. The difference of voltage level with φL at tsr/2 is defined as substrate clock voltage $V\phi_{SUB}$.

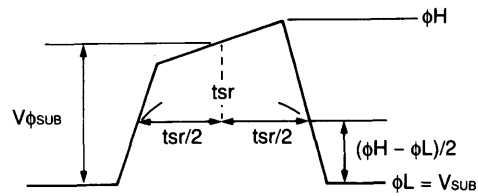


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1) Definition of ϕ_H (100%) and ϕ_L (0%)
   (1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   (2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_3$) is applied.
   (3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".
2) Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.19MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
Hφ1	18	33.7	10	8	ns	Imaging period
Hφ2	18	33.7	10	8		
Hφ1	4.9		0.10	0.01	μs	Parallel-serial converting period
Hφ2		4.9	0.10	0.01		
φPG	12	53.7	2	2	ns	
Vφ1/Vφ2	61.6	1.6	0.1	0.1	μs	Imaging period
Vφ3/Vφ4	2.8	60.45	0.05	0.1		
VφT	2.4		0.2	0.1		Reading period
SUBφ	1.0		0.08	0.1	μs	Electron sweep-off period

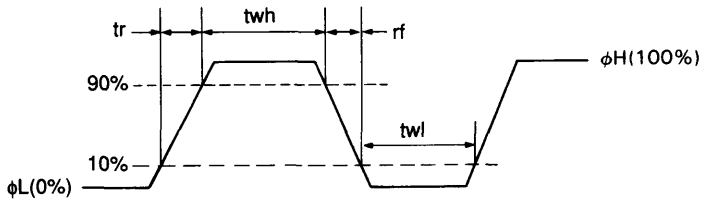


Fig. 10 Clock waveform

Imaging Characteristics

(For the testing circuit, see Fig. 11.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sg	130	180		mV	1	
Output saturation signal	Vsat	500			mV	2	Note
Blooming margin		800			times	3	Note
Smear	Smr		0.007	0.015	%	4	
Video signal shading	Svg			25	%	5	
Dark signal output	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C

Note) Saturation signal and blooming margin are guaranteed only when the substrate voltage has been set to the voltage indicated on the back of the imaging device.

Test Methods

Conditions

1) The conditions required to drive the device through the following tests are converted by the bias conditions and the clock voltage conditions. The test circuit shown in Fig. 11 is used for evaluating and testing the characteristics.
2) Blemish are excluded from the following tests and the signal output is based on the optical back level unless otherwise specified. The value obtained at the output test point becomes the test value.

Standard imaging conditions

1) Shoot the PTB-100 pattern box (luminance 706 Nit, color temperature 3200°K) with no pattern, using a FUJINON H6 × 12.5D (F1.4) lens at F5.6. Use the CM-500S (1.0 mmt) filter to cut off infrared rays.
2) Shoot a light source (color temperature 3200°K) which provides a uniform brightness within 2% over the whole screen.
   For infrared cut-off filter, use the CM-500S (1.0 mmt)

1. Set the standard imaging condition 1) and test signal voltages the center of the screen.

2. Set to standard imaging condition 2) and adjust the light intensity to about eight times the intensity obtained at a signal voltage of 200 mV. Them obtain the minimum value of the signal voltage over the whole screen.

3. Set to imaging condition 2) and adjust the light intensity to about 800 times the intensity obtained at a signal voltage of 200 mV. At that time make sure there is no blooming and the vertical resistor is not saturated.

4. Set to standard imaging condition 2) and adjust the light intensity so that the signal voltage (V_{SG}) becomes 200 mV. Then, turn V_T off and obtain the maximum value of the signal voltage "V_{SM}" after stopping the horizontal resistor 50 H at the effective picture element.

$$Smr = \frac{V_{SM}}{V_{SG}} \times \frac{1}{50} \times \frac{1}{10} \times 100\ (\%)$$

(Converted into 1/10 V system)

5. Set to standard imaging condition 2) and test the signal voltage to obtain maximum (V_G max) and minimum (V_G min) values.
The light intensity is adjusted so that the average value of the signal voltage (V_G average) becomes about 200 mV.

$$Svg = \frac{V_{SG}max - V_{SG}min}{V_{SG}\ average} \times 100\ (\%)$$

6. Measure the mean voltage of the dark current signal based on the horizontal free-transfer level in a light-shaded condition with an ambient temperature of 55°C.

7. Following measurement 6, test the dark current signal voltage to obtain the maximum (Vdmax) and minimum (Vdmin) values. Spot defects are ignored in this test.

Electrical Characteristics Test Circuit

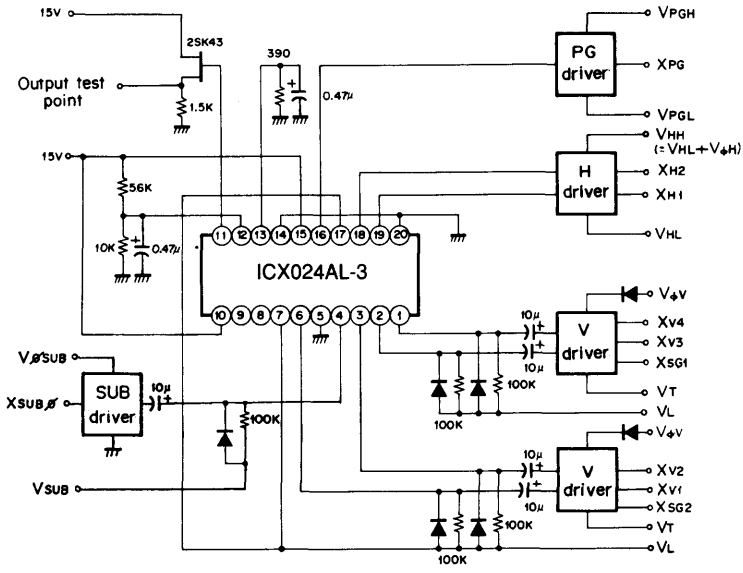
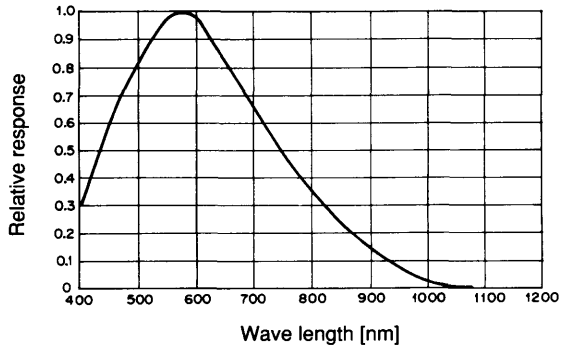
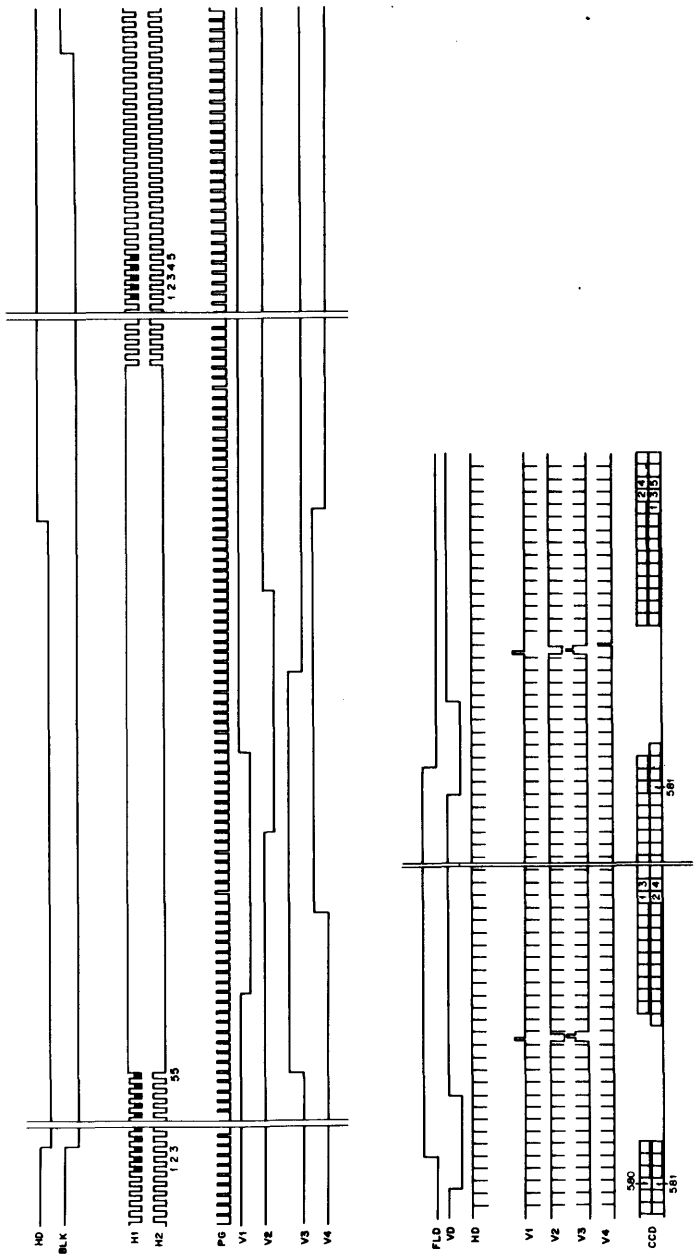


Fig. 11

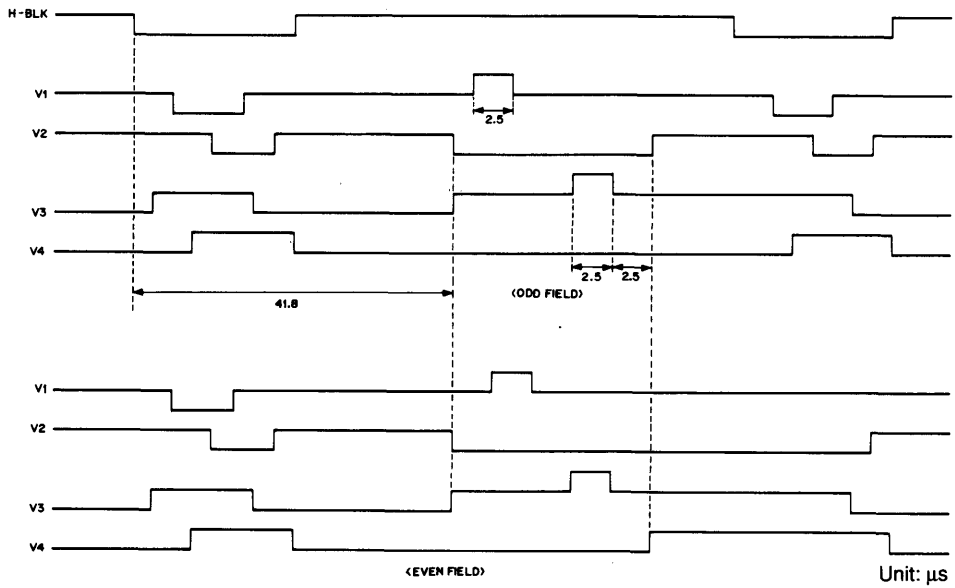
Spectrum Sensitivity Characteristics (Typical example, excluding illuminant characteristics)
With a Fujinon lens H6 x 12.5D



Driving Pulse Timing Chart

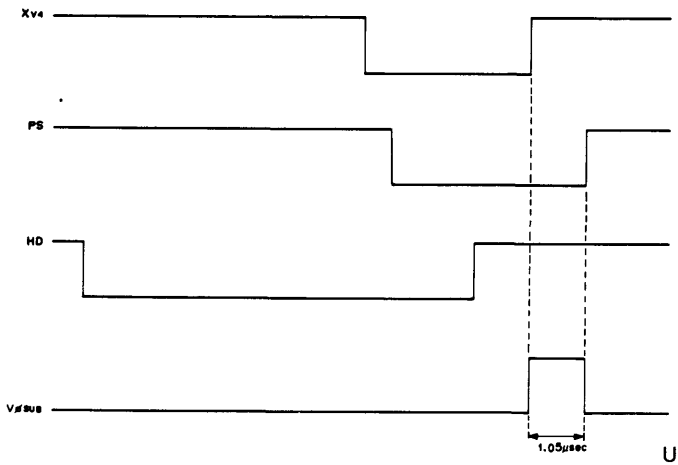


Sensor Read Clock Timing Chart



Unit: µs

Charge Drain Clock Timing Chart



Unit: µs

Handling Instructions

1. On electric screening
   To prevent damage to the CCD image sensor by static electricity, handle as follows.
   a) Either handle the device with bare hands, or use antistatic gloves and clothes. Conductive shoes are also required.
   b) Use a ground lead when directly touching the device.
   c) Cover the floor and working table with a conductive mat or equivalent to avoid static electricity.
   d) Discharge using ionized air is recommended.
   e) To ship the mounted boards, use cartons with antistatic properties.

2. On soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder-dipping of DIP in a mounting furnace may break glass. Use a grounded 30 W soldering iron a each pin for less than 2 seconds. When adjusting or removing soldered parts, let the CCD cool sufficiently.
   c) Do not use any solder-aspirating equipment to remove the imaging device. Should an electric solder-aspiration device be used, use only a device of the zero-cross type control system and be sure to ground the controller.

3. On contamination
   a) Keep the operation room clean (Class 1000 Will be expected).
   b) Do not touch the glass surface avoid contact with foreign objects. Blow off any dust the surface with a blower. (Ionized air is recommended to blow off any object sticking through static electricity.)
   c) Wipe off grass spots with an applicator moistened with ethanol. Be careful not to scratch the surface.
   d) To eliminate contamination, store the device in an exclusive case. During transportation minimize the difference in temperatures between locations to avoid moisture condensation.
   e) When a protection tape has been affixed for shipment, remove it just before use after applying appropriate antistatic measures. Do no reuse the removed tape.

4. Do not subject the device to light sources for extended periods. If a color element is subjected to strong light ray for an extended period, the color filter will be discolored. (Store the device in a dark place.)

5. Usage or storage of the device in high temperature or high humidity may seriously affect the performance.

6. The CCD image sensor is a high-precision optical part, that should not be subjected to mechanical shocks.

7. System data write complete ROM (with flow compensation address included)
   System data write complete ROM in equal quantity as ICX024AL-3 is attached.
   Analog those ROM with address for flow compensation have serial No. stuck on.
   Use in conjunction with ICX024AL-3 pairing the same serial No..

Solid-State Image Sensor for B/W Camera

Description

The ICX026BL is an interline transfer CCD solid-state imager suitable for EIA 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole Accumulation Diode) sensors.

This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

Features

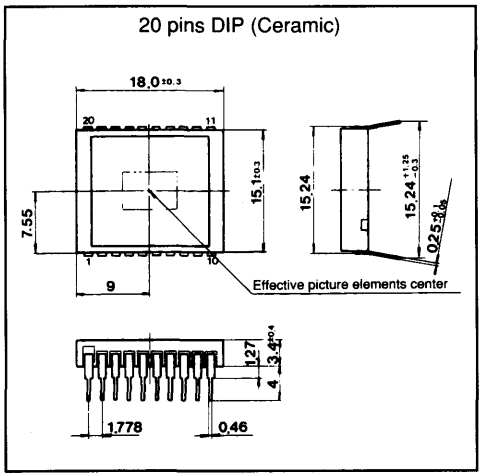
- High sensitivity (+6 dB compare with ICX026AL)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

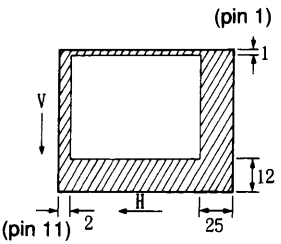
Device Structure

- Number of effective pixels 510 (H) × 492 (V)
- Number of total pixels 537 (H) × 505 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 9.8 µm (V)
- Optical black
  - Horizontal (H) direction Front 2 pixels Rear 25 pixels
  - Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon

Package Outline

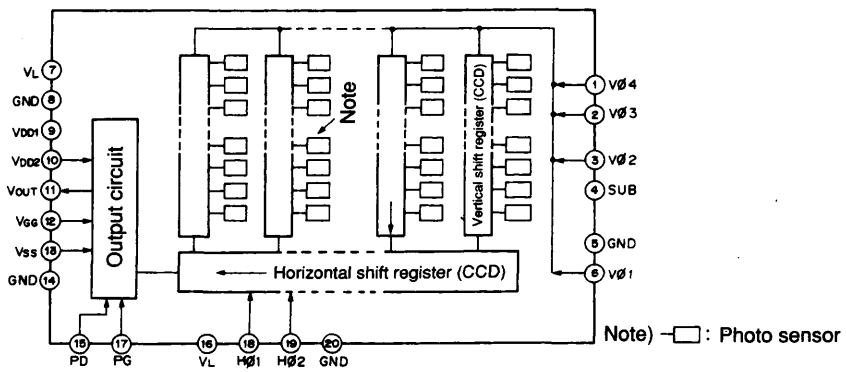
Unit: mm





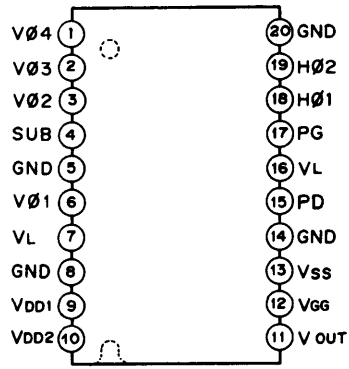
Optical black position (Top View)

Block Diagram



E89922-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD1	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD2	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	−0.3 to +55	V
• Supply voltage	VDD1, VDD2, PD, VOUT, Vss – GND	−0.3 to +18	V
	VDD1, VDD2, PD, VOUT, Vss – SUB	−55 to +10	V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	−15 to +20	V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	−65 to +10	V
• Voltage difference between vertical clock input pins		15	V* (Max.)
• Voltage difference between horizontal clock input pins		17	V (Max.)
• Hφ1, Hφ2 – Vφ4		−17 to +17	V
• PG, VGG – GND		−10 to +15	V
• PG, VGG – SUB		−55 to +10	V
• VL – SUB		−65 to +0.3	V
• Beside GND, SUB, VL – VL		−0.3 to +30	V
• Storage temperature		−30 to +80	°C
• Operating temperature		−10 to +55	°C

***Note)** +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%

Bias Conditions

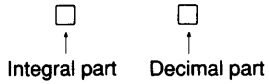
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display



The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical Value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, V_{SS} and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1 and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

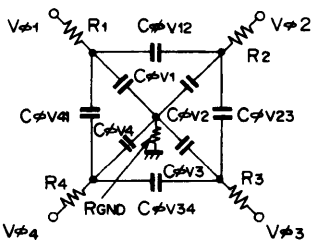
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	−0.2	0	0.2	V	1,2,3,6	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	−9.6	−9.0	−8.3	V	1,2,3,6	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	−0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	−0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0	32.0	34.0	V	4	*5

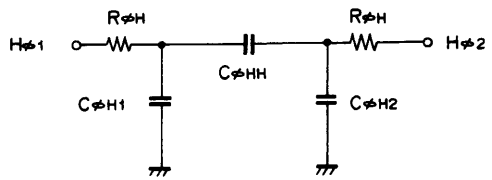
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		750		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

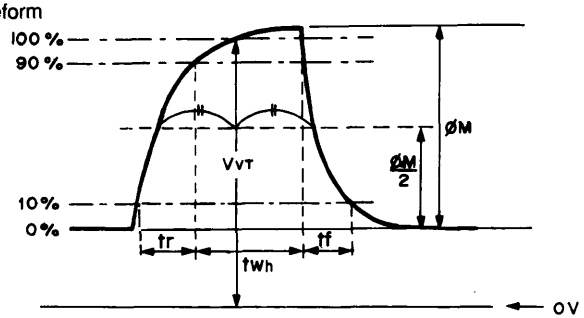


Fig.1

2. Vertical transfer clock waveform

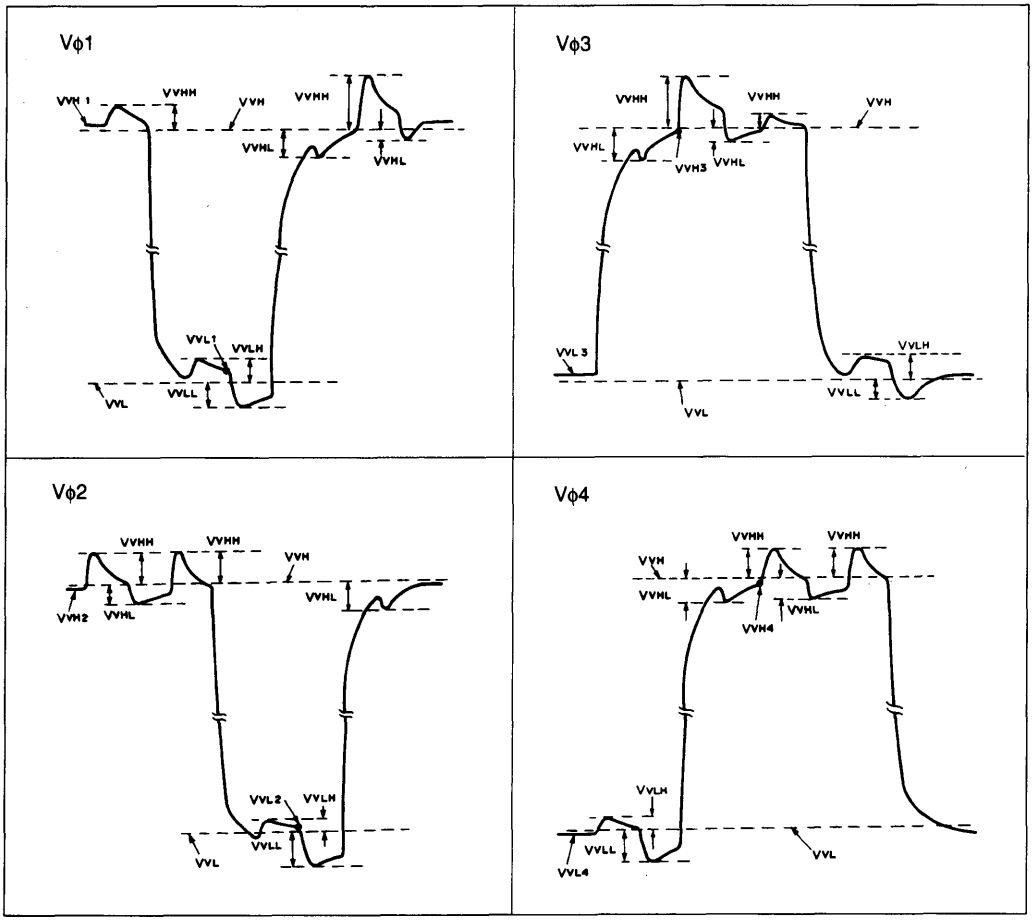


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

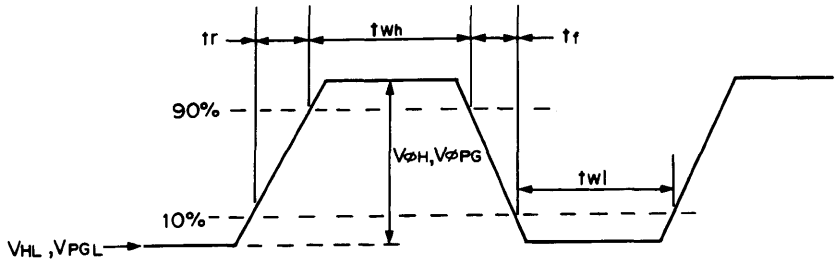


Fig. 3

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max		
Read out clock	V_T	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	Vφ1,Vφ2,Vφ3,Vφ4									0.45	0.015		0.25	µs	*
Horizontal transfer clock	Hφ	37	41		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	Hφ1		5.6						0.012			0.01		µs	During parallel serial conversion
Horizontal transfer clock	Hφ2					5.6			0.012			0.01		µs	During parallel serial conversion
Precharge gate clock	φPG	15	17		75	81			4			3		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	µs	During charge drain.

*Note) When vertical transfer clock driver CXD1250 is in use.

4. Substrate clock waveform

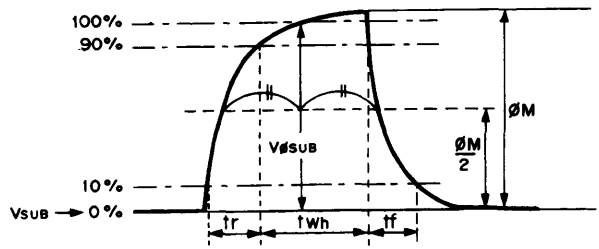


Fig. 4

Operating Characteristics Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	320		mV	1	
Saturation signal	Vsat	500			mV	2	Ta=55°C
Smear	SM		0.007	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SH			20	%	5	Zone 0, I
				25	%	5	Zone 0 to II'
Dark signal	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C
Flicker	F			2	%	8	
Lag	ΔVlag			0.5	%	9	

Test Method

Test conditions

① Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OPB) is set as the reference. The values obtained at A point in the figure of the Drive Circuit are utilized.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200K Halogen source), at F8 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average signals (V_A) indicated in each item.

1. Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Set to standard imaging condition II. Adjust light intensity to 10 times when the average signal V_A=150mV. Then test signal Min. Value.

3. Set to standard imaging condition II. Adjust light intensity to 500 times when the average signal V_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value V_{SM} of signal output.

   $SM = (V_{SM}/V_A) \times 1/500 \times 1/10 \times 100$ (%) ($^1/_{10}$V)

4. Set to standard imaging condition II. Adjust light intensity to 1000 times when the average signal V_A=150mV. Then check that there is no blooming.

5. Video signal shading SH
   Set to standard imaging condition II. Test signal Max. (Vmax) and Min. (Vmin) values. Adjust light intensity to obtain an average signal (V_A) of about 150mV.

   $SH = (Vmax - Vmin)/V_A \times 100$ (%)

6. Test the average signal when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

7. Following test 6, test Max. (Vd max) and Min. (Vd min) of signal output. Only keep spot defects out of this range.

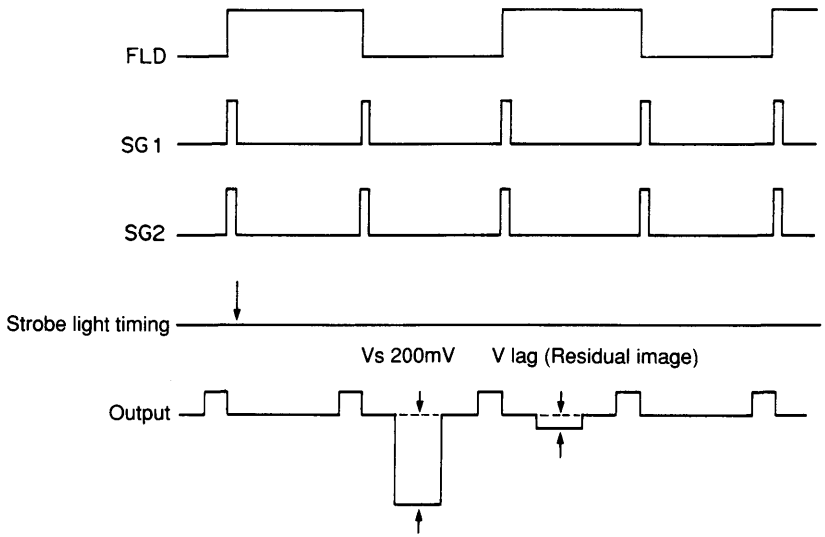
   ΔVdt = Vd max − Vd min

8. Set to imaging condition II. Test the output signal difference (ΔVf) between even and odd field. At that time, adjust light intensity to obtain an average signal (V_A) of about 150 mV.

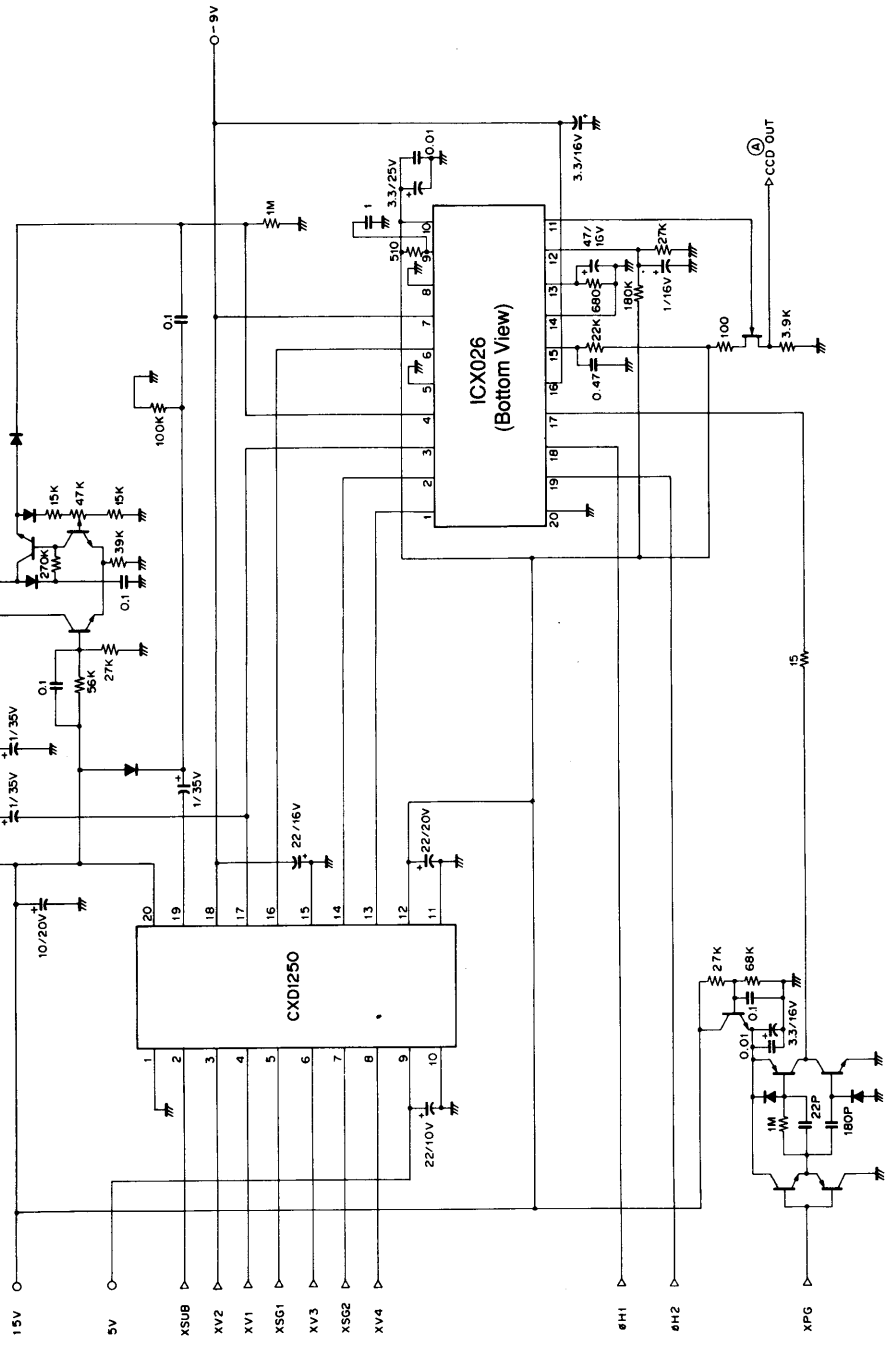
   $F = (\Delta Vf/V_A) \times 100$ (%)

9. Light a stroboscopic tube with the following timing and test the residual image.

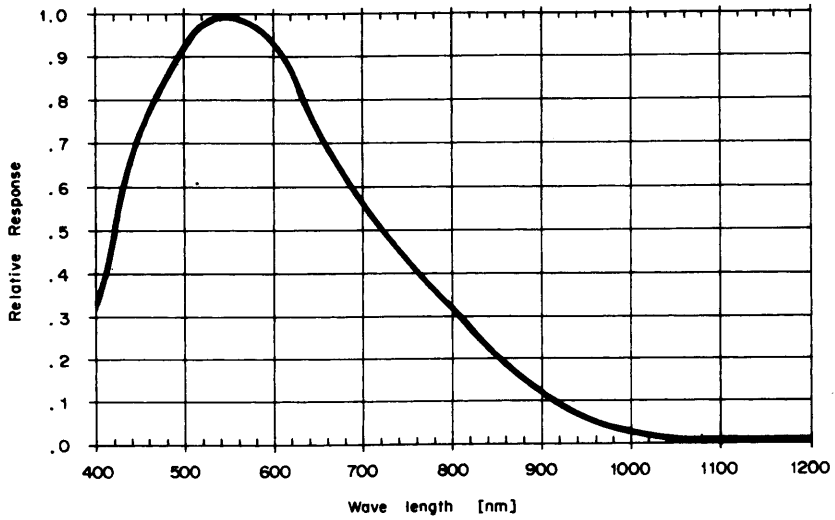
   $\Delta Vlag = (Vlag/Vs) \times 100$ (%)



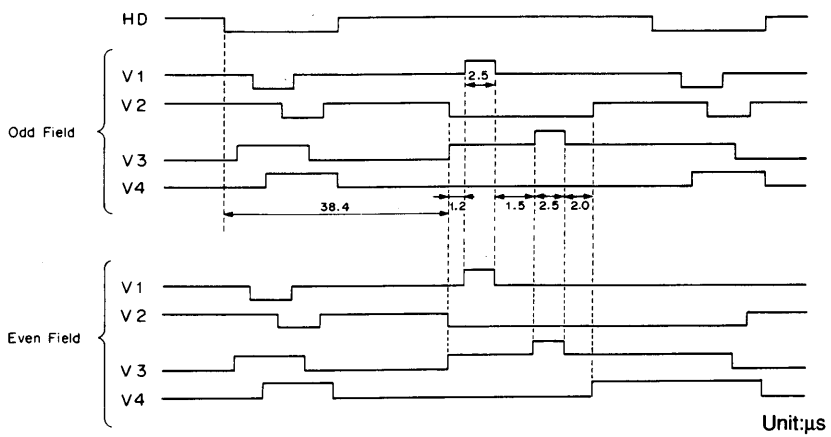
Drive Circuit



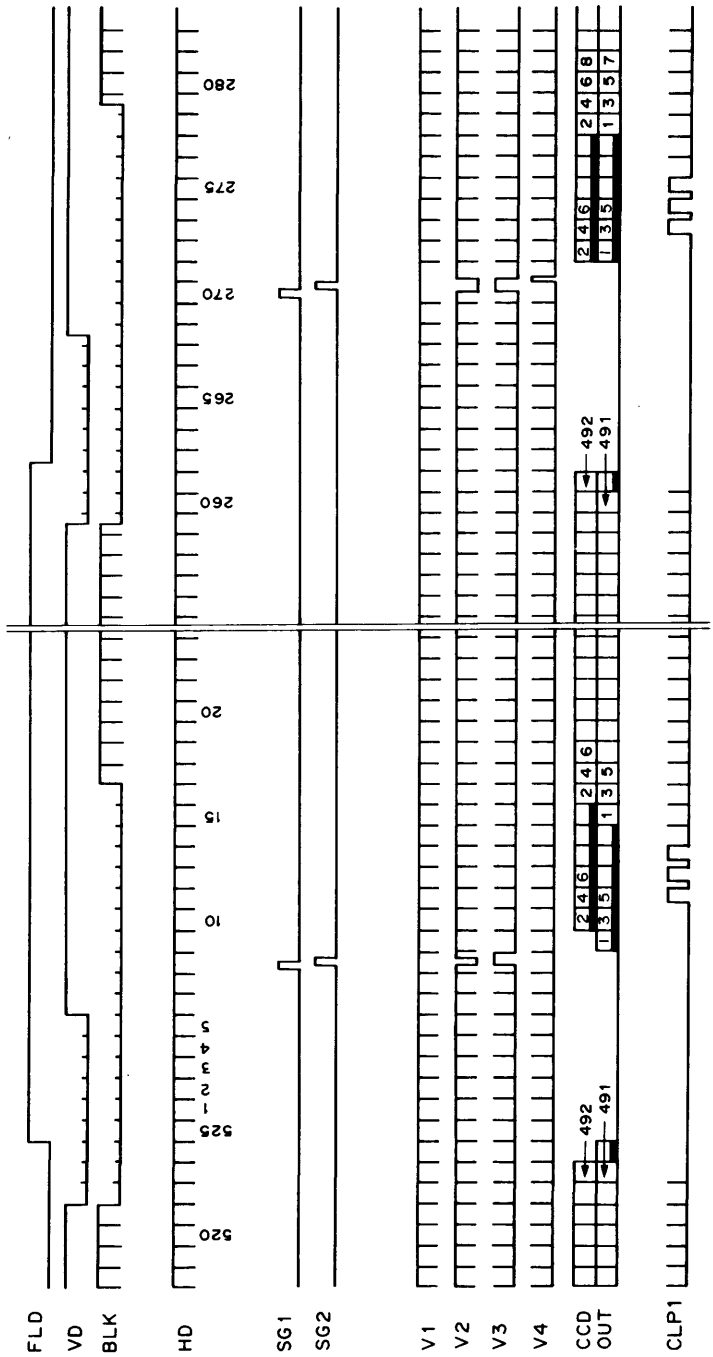
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



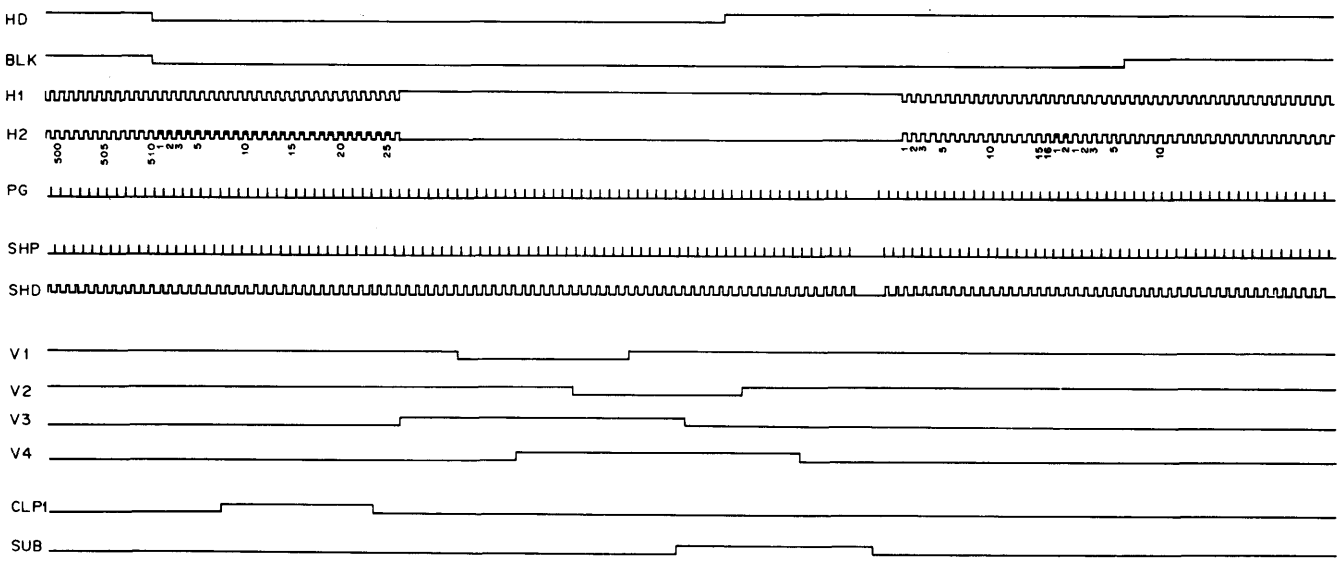
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY®

ICX027BL

Solid-State Image Sensor for B/W Camera

Description

The ICX027BL is an interline transfer CCD solid-state imager suitable for CCIR 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole Accumulation Diode) sensors.

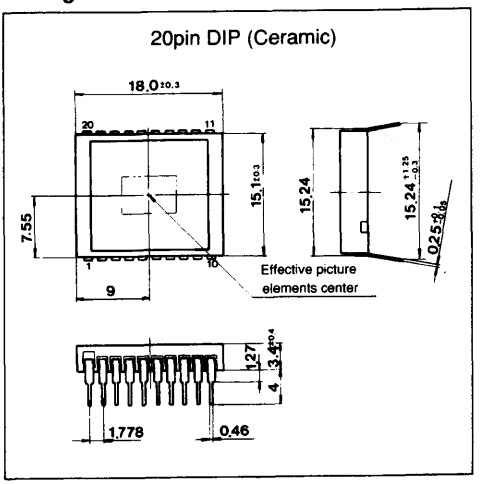
This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

Features

- High sensitivity (+6 dB compare with ICX027AL)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

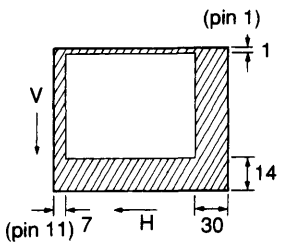
Package Outline

Unit: mm



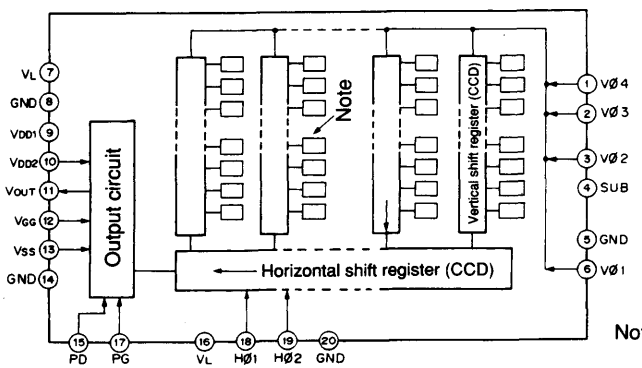
Device Structure

- Number of effective pixels 500 (H) × 582 (V)
- Number of total pixels 537 (H) × 597 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 µm (H) × 8.3 µm (V)
- Optical black
  - Horizontal (H) direction Front 7 pixels Rear 30 pixels
  - Vertical (V) direction Front 14 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

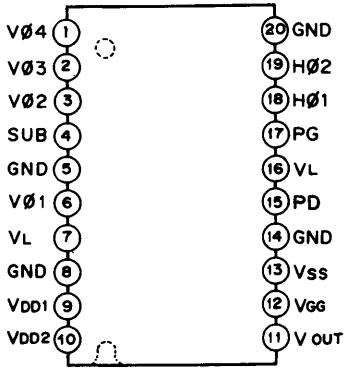
Block Diagram



Note)—□ : Photo sensor

E89923-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD1	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD2	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	−0.3	to	+55	V
• Supply voltage	VDD1, VDD2, PD, VOUT, Vss – GND	−0.3	to	+18	V
	VDD1, VDD2, PD, VOUT, Vss – SUB	−55	to	+10	V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	−15	to	+20	V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	−65	to	+10	V
• Voltage difference between vertical clock input pins			15		V* (Max.)
• Voltage difference between horizontal clock input pins			17		V (Max.)
• Hφ1, Hφ2 – Vφ4		−17	to	+17	V
• PG, VGG – GND		−10	to	+15	V
• PG, VGG – SUB		−55	to	+10	V
• VL – SUB		−65	to	+0.3	V
• Beside GND, SUB, VL – VL		−0.3	to	+30	V
• Storage temperature		−30	to	+80°C	
• Operating temperature		−10	to	+55°C	

***Note)** +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%

Bias Conditions

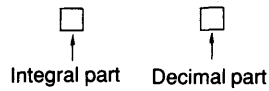
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display



The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical Value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, V_{SS} and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1 and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

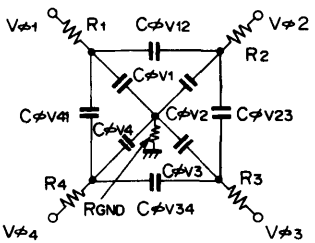
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	−0.2	0	0.2	V	1,2,3,6	V_{VH}=(V_{VH1}+V_{VH2})/2
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	−9.6	−9.0	−8.3	V	1,2,3,6	V_{VL}=(V_{VL3}+V_{VL4})/2
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}$=V_{VHn}-V_{VLn} (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	−0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	−0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0	32.0	34.0	V	4	*5

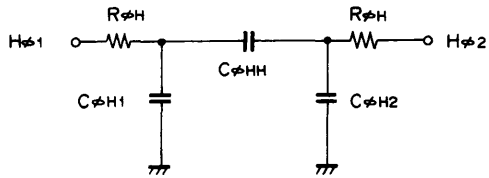
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1400		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		900		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

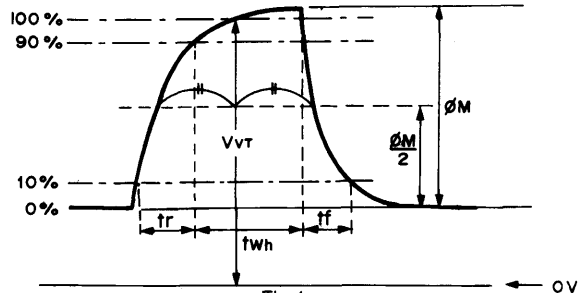


Fig.1

2. Vertical transfer clock waveform

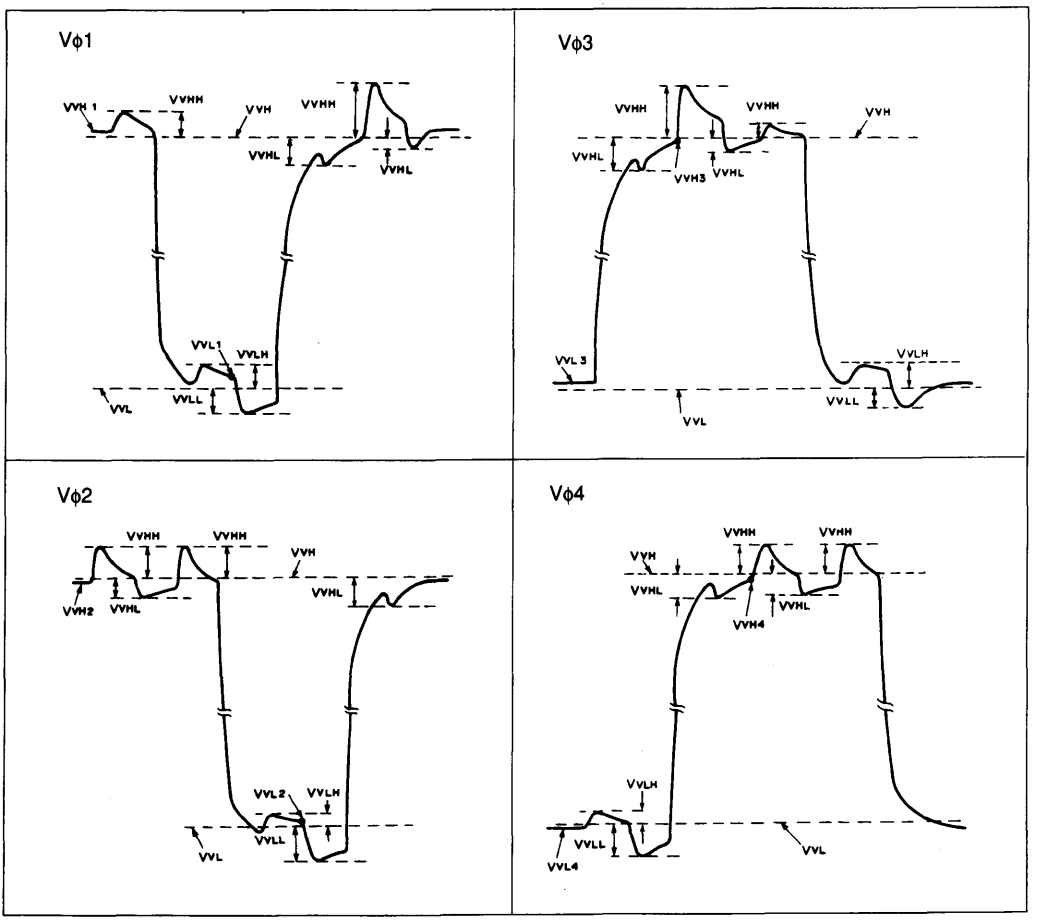


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

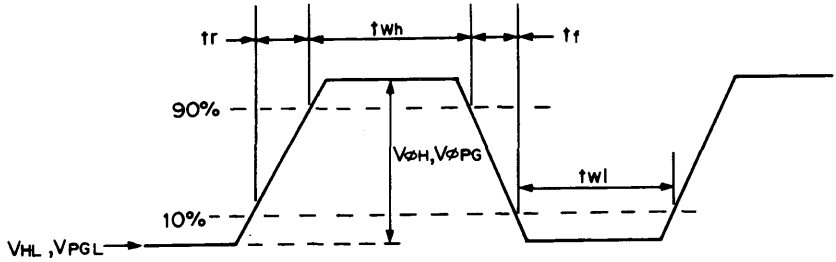


Fig. 3

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	VT	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	Vφ1,Vφ2,Vφ3,Vφ4									0.45	0.015		0.25	µs	*
Horizontal transfer clock	Hφ	38	42		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	Hφ1		5.6						0.012			0.01		µs	During parallel serial conversion
Horizontal transfer clock	Hφ2					5.6			0.012			0.01		µs	During parallel serial conversion
Precharge gate clock	φPG	15	17		76	82			4			3		ns	
Substrate clock	φSUB	1.5	2.1							0.5			0.5	µs	During charge drain

***Note)** When vertical transfer clock driver CXD1250 is in use.

4. Substrate clock waveform

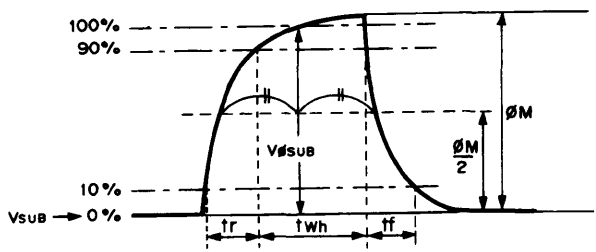


Fig. 4

Operating Characteristics

Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	220	300		mV	1	
Saturation signal	Vsat	450			mV	2	Ta=55°C
Smear	SM		0.007	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SH			20	%	5	Zone 0, I
				25	%	5	Zone 0 to II'
Dark signal	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C
Flicker	F			2	%	8	
Lag	ΔVlag			0.5	%	9	

Test Method

Test conditions

① Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OPB) is set as the reference. The values obtained at A point in the figure of the Drive Circuit are utilized.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200 K Halogen source), at F8 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200 K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average signals (V_A) indicated in each item.

1. Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Set to standard imaging condition II. Adjust light intensity to 10 times when the average signal V_A=150mV. Then test signal Min. Value.

3. Set to standard imaging condition II. Adjust light intensity to 500 times when the average signal V_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value V_{SM} of signal output.

   $SM = (V_{SM}/V_A) \times {}^1/_{500} \times {}^1/_{10} \times 100$ (%) ($^1/_{10}$V)

4. Set to standard imaging condition II. Adjust light intensity to 1000 times when the average signal V_A=150mV. Then check that there is no blooming.

5. Video signal shading SH
   Set to standard imaging condition II. Test signal Max. (Vmax) and Min. (Vmin) values. Adjust light intensity to obtain an average signal (V_A) of about 150mV.

   $SH = (Vmax - Vmin)/V_A \times 100$ (%)

6. Test the average signal when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

7. Following test 6, test Max. (Vd max) and Min. (Vd min) of signal output. Only keep spot defects out of this range.

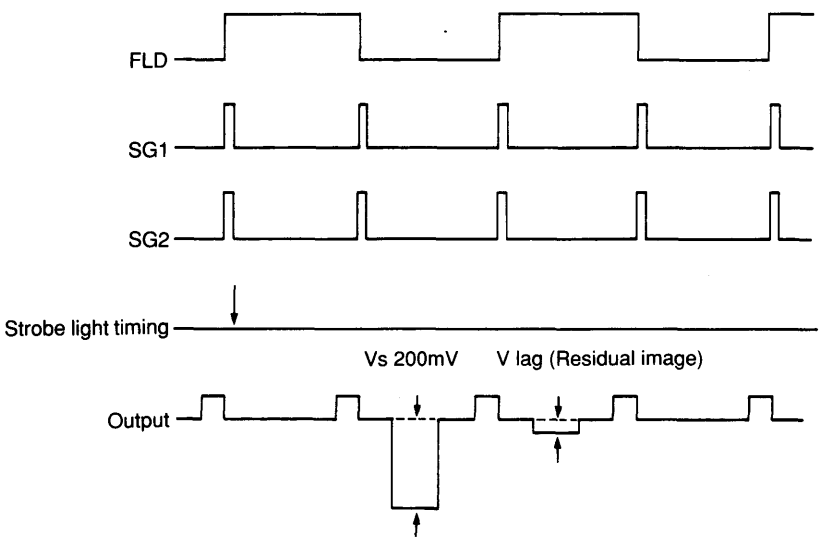
   ΔVdt = Vd max - Vd min

8. Set to imaging condition II. Test the output signal difference (ΔVf) between even and odd field. At that time, adjust light intensity to obtain an average signal V_A of about 150mV.

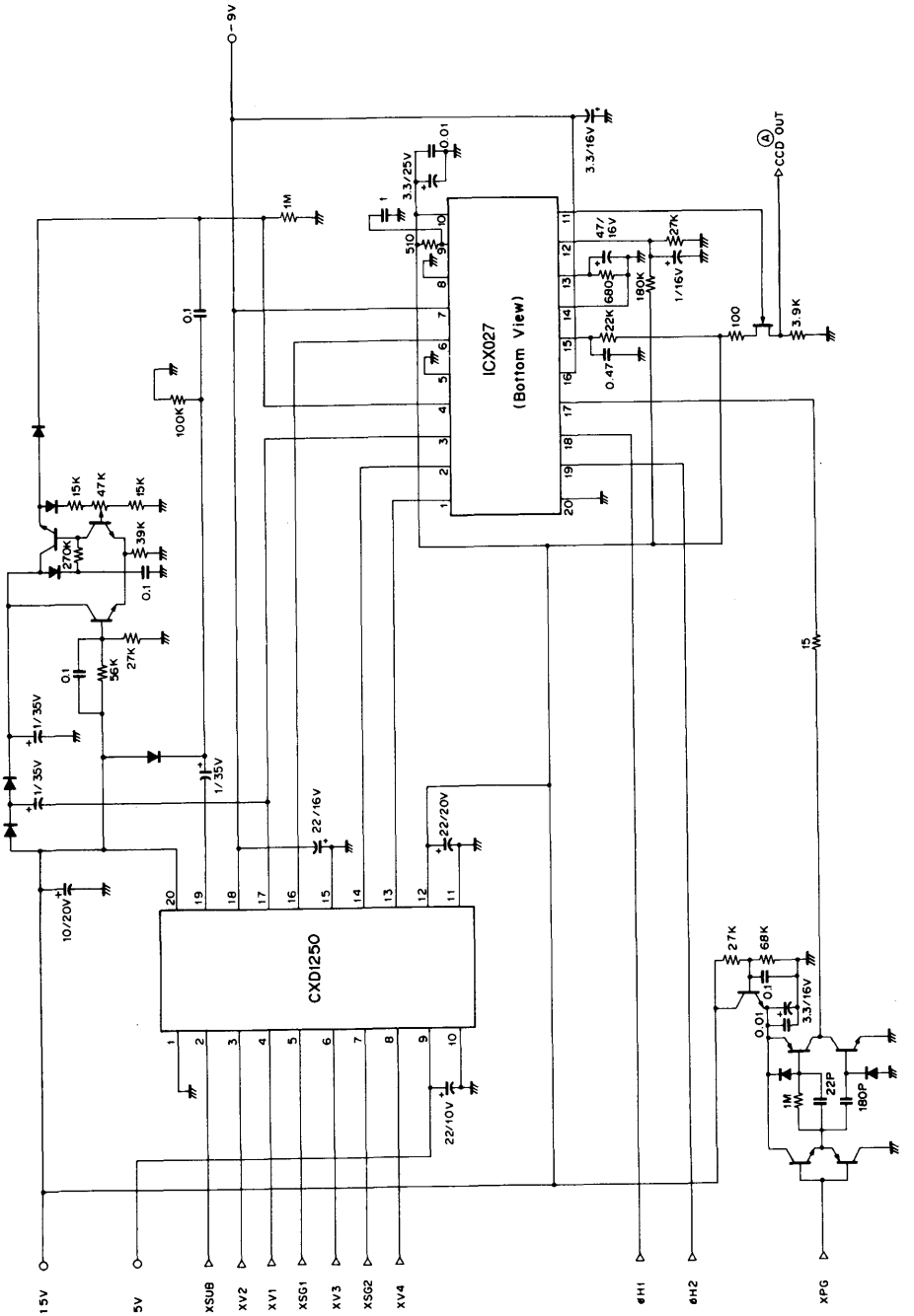
   $F = (\Delta Vf/V_A) \times 100$ (%)

9. Light a stroboscopic tube with the following timing and test the residual image.

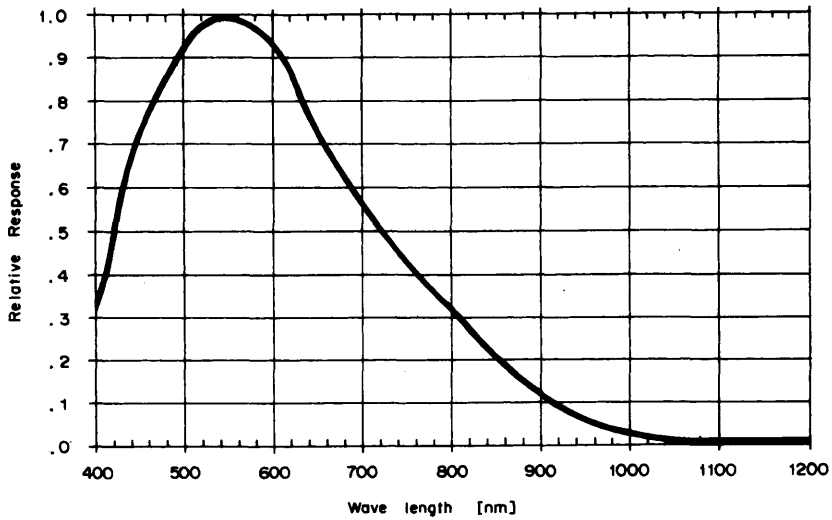
   $\Delta Vlag = (Vlag/Vs) \times 100$ (%)



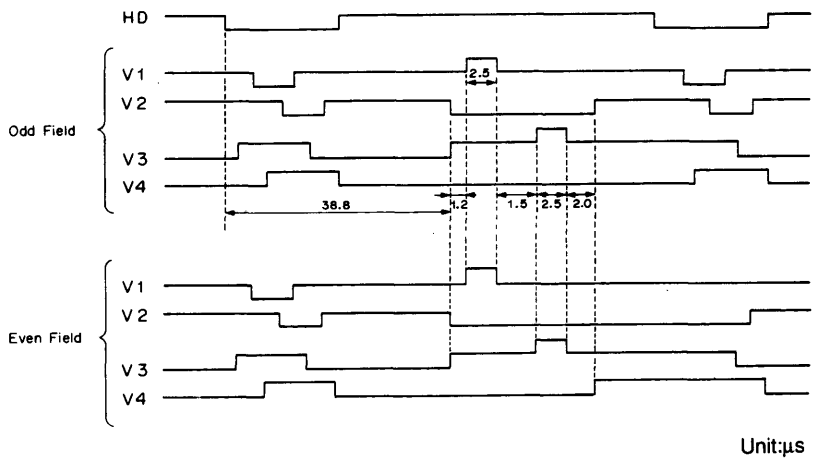
Drive Circuit



Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)

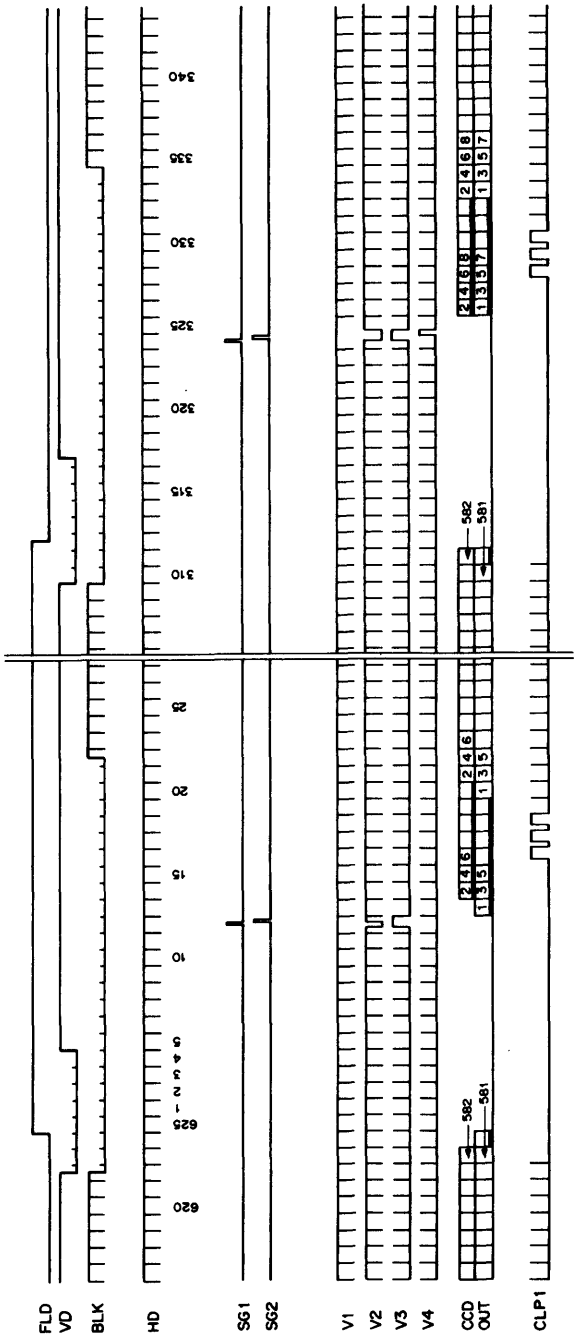


Using Read Out Clock Timing Chart

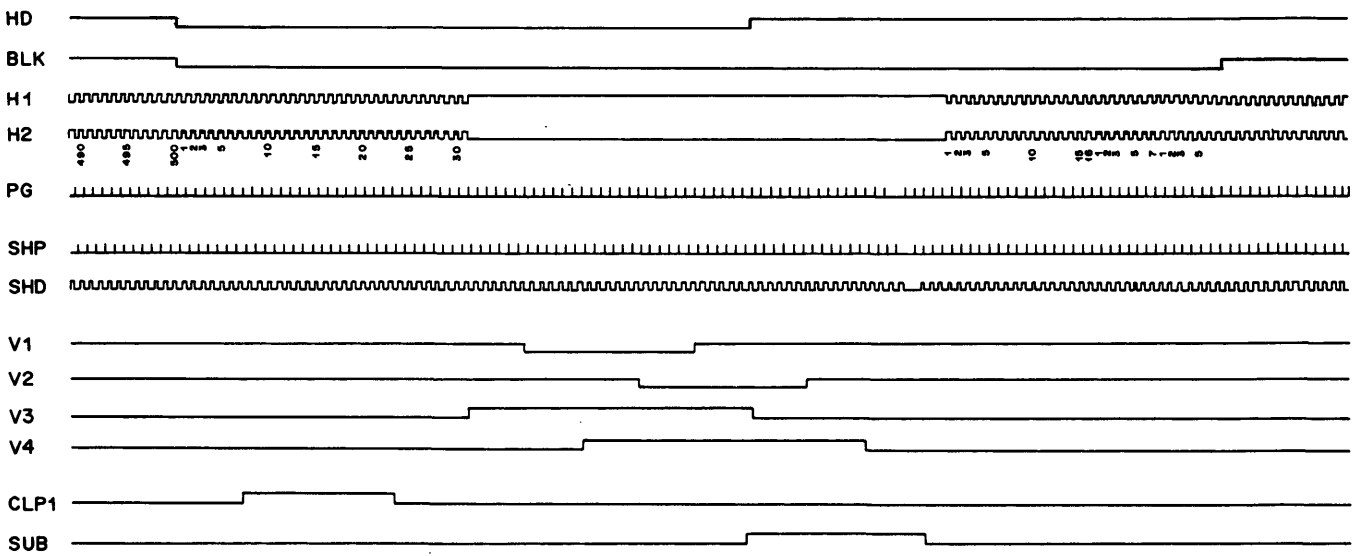


Unit:µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

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a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
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e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

SONY

ICX038AL

Solid-State Image Sensor for B/W Camera

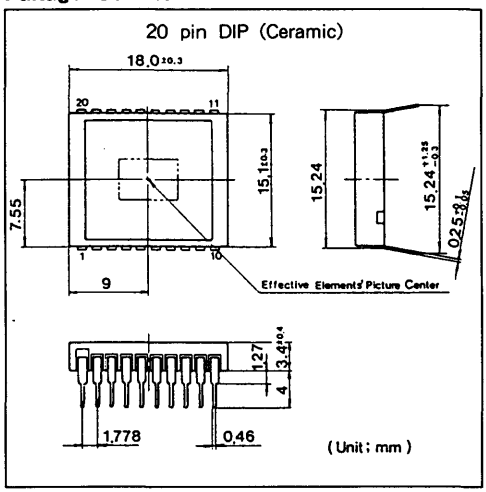
Description

ICX038AL is an interline transfer CCD solid-state imager suitable for EIA 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole - Accumulation Diode) sensors.

This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

Pakage Outline

Unit : mm

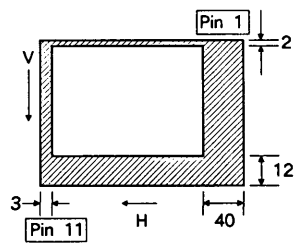


Features

- High image, high sensitivity and low dark current
- Consecutive various speed shutter
  1/60sec.(Typ.), 1/100sec. to 1/10000sec.
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

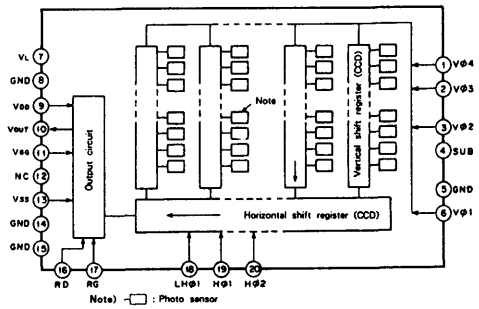
- Optical size 1/2 inch format
- Number of effective pixels
  768 (H) × 494 (V) Approx. 380k pixels
- Number of total pixels
  811 (H) × 508 (V) Approx. 410k pixels
- Interline transfer CCD image sensor
- Chip size 7.95mm (H) × 6.45mm (V)
- Unit cell size 8.4 µm (H) × 9.8 µm (V)
- Optical black Horizontal (H) direction Front 3 pixels Rear 40 pixels
  Vertical (V) direction Front 12 pixels Rear 2 pixels
- Number of dummy bits Horizontal 22
  Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

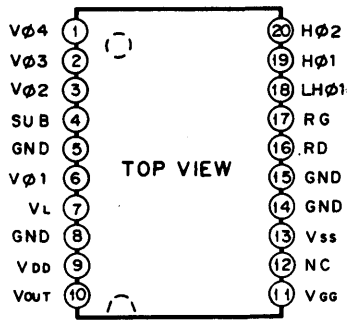
E89X30 – ST

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	V φ 4	Vertical register transfer clock	11	V_{GG}	Output amplifier gate bias
2	V φ 3	Vertical register transfer clock	12	NC	
3	V φ 2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	GND	GND
6	V φ 1	Vertical register transfer clock	16	RD	Reset drain bias
7	V_L	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	LH φ 1	Horizontal register final stage transfer clock
9	V_{DD}	Output amplifier drain supply	19	H φ 1	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	H φ 2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		− 0.3 to + 55	V	
Supply voltage	V_{DD}, V_{RD}, V_{OUT}, Vss − GND	− 0.3 to + 18	V	
	V_{DD}, V_{RD}, V_{OUT}, Vss − SUB	− 55 to + 10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4 − GND	− 15 to + 20	V	
	V φ 1, V φ 2, V φ 3, V φ 4 − SUB	to + 10	V	
Voltage difference between vertical clock input pins		to + 15	V	* (Max.)
Voltage difference between horizontal clock input pins		to + 17	V	
H φ 1, H φ 2 − V φ 4		− 17 to + 17	V	
LH φ 1, RG, V_{GG} − GND		− 10 to + 15	V	
LH φ 1, RG, V_{GG} − SUB		− 55 to + 10	V	
V_L − SUB		− 65 to + 0.3	V	
Beside GND, SUB-V_L		− 0.3 to + 30	V	
Storage temperature		− 30 to + 80	℃	
Operating temperature		− 10 to + 60	℃	

* **Note)** + 27V (Max.) when clock width < 10 μs, duty factor < 0.1 %.

Bias Conditions

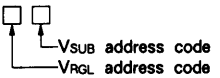
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 390 Ω resistor				± 5 %
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	− 3		+ 3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0.5		5.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	− 3		+ 3	%	
Protective transistor bias	V_L	*3				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*** 2)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3 %.

V_{SUB} code address − 1 digit display
V_{RGL} code address − 1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	0	1	2	3	4	5	6	7	8	9
Numerical value	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

< Example > "5L" → V_{RGL} = 3.0V
V_{SUB} = 12.0V

*** 3)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* **4)** 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss and SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V φ 1, V φ 2, V φ 3, V φ 4, H φ 1 and H φ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, LH φ 1 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

* **5)** Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

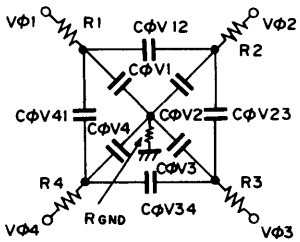
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	− 0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	− 0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	V φ v	8.3	9.0	9.65	V	2	V φ v = V_{VHn} − V_{VLn} (n = 1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.1	V	2	
	$V_{VH3} - V_{VH}$	− 0.25		0.1	V	2	
	$V_{VH4} - V_{VH}$	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V φ H	4.75	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	V_{LHH}	4.45	5.0	5.55	V	4	
	V_{LHL}	− 4.7	− 4.0	− 3.5	V	4	
	V φ LH	8.0	9.0	10.0	V	4	
Reset gate clock voltage	V φ RG	4.5	5.0	5.5	V	5	* 6
	$V_{RGLH} - V_{RGLL}$			0.8	V	5	Low level coupling
Substrate clock voltage	V φ SUB	23.0	24.0	25.0	V	6	

* 6) No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

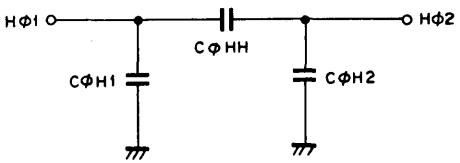
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	−0.2	0	0.2	V	5	
	$V_{\phi RG}$	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1800		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		2200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		450		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		270		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		62		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH}$		8		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		68		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	



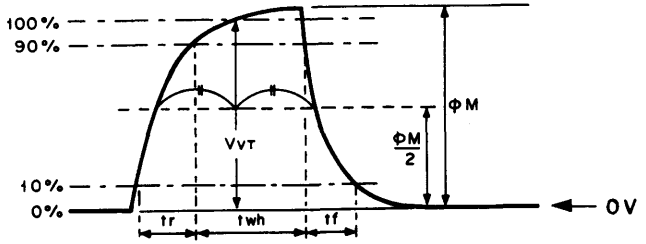
Vertical transfer clock equivalent circuit



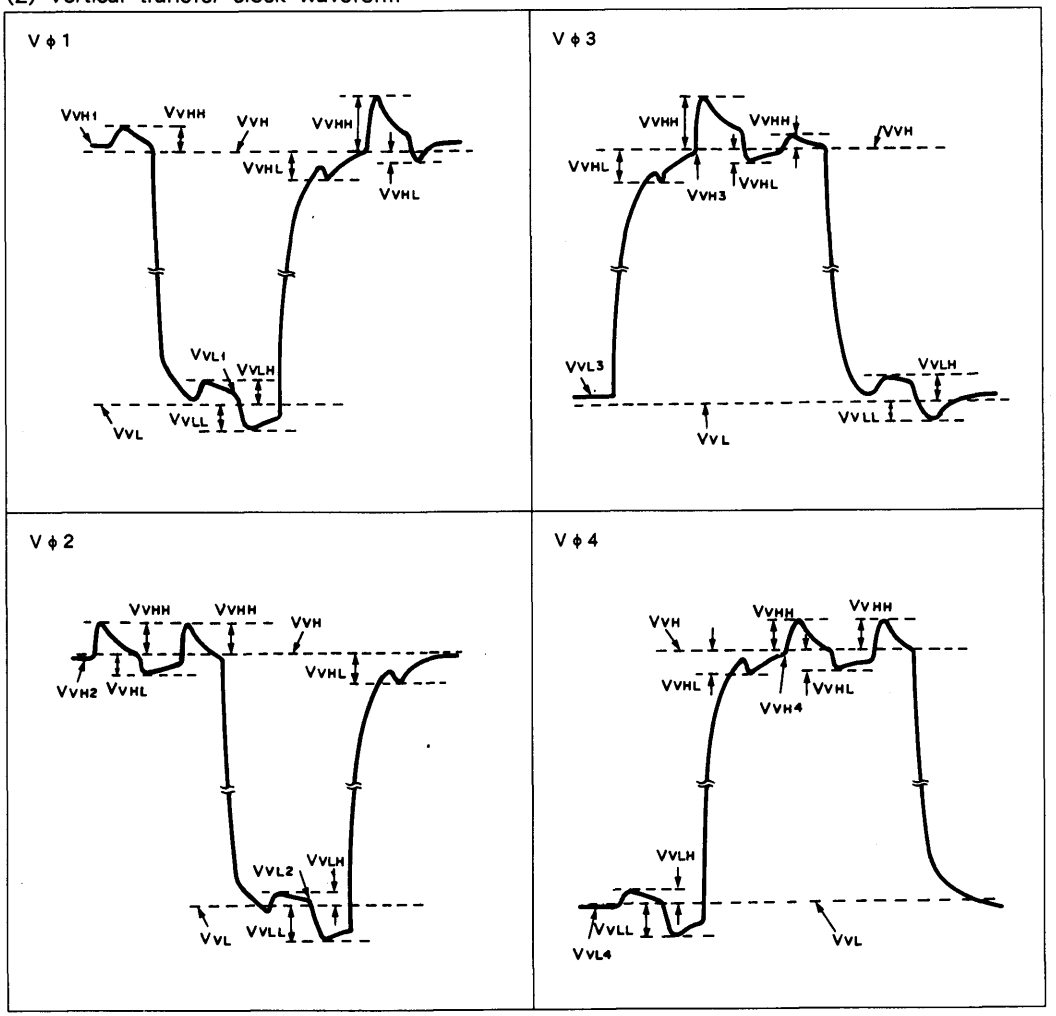
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

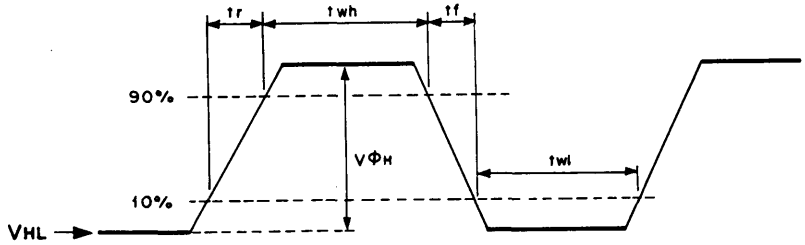
(1) Read out clock waveform



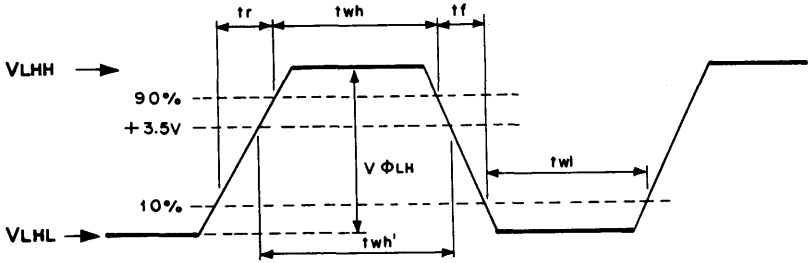
(2) Vertical transfer clock waveform



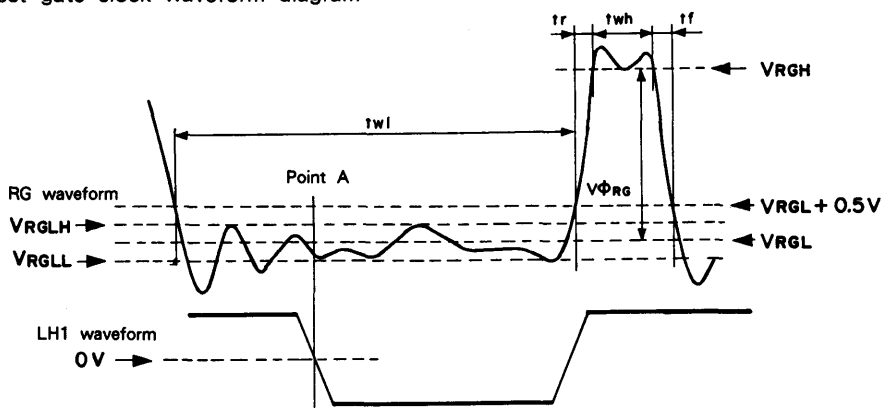
(3) Horizontal transfer clock waveform diagram



(4) Horizontal final stage transfer clock waveform diagram



(5) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

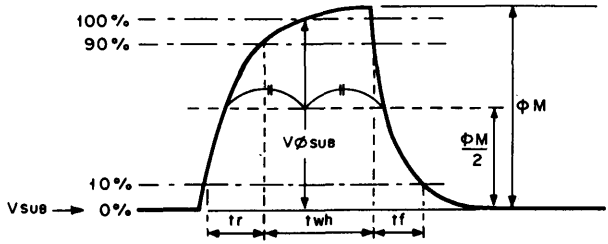
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

V_{RGH} is the minimum value for twh period.

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(6) Substrate clock waveform



Clock switching characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		μs	During read out
Vertical transfer clock	V φ 1, V φ 2, V φ 3, V φ 4										0.015		0.25	μs	* 7
Horizontal transfer clock	H φ		20			20			15	19	*8	15	19	ns	During imaging
Horizontal final stage clock	LH φ		24		22	27			10			9		ns	During imaging
Horizontal transfer /horizontal final stage clock	H φ 1, LH φ		5.38						0.01			0.01		μs	During parallel serial conversion.
Horizontal transfer clock	H φ 2					5.38			0.01			0.01		μs	
Reset gate clock	φ RG	11	13			51			3			3		ns	
Substrate clock	φ SUB	1.5	1.8							0.5			0.5	μs	During charge drain.

* **7)** When vertical transfer clock driver CXD1250 is in use.
* **8)** tf ≧ tr − 2 ns

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H φ	16	20		ns	*9
Horizontal transfer/ horizontal final stage clock	H φ 2, LH φ	15	20		ns	*10

* **9)** "two" is the overlap period of horizontal transfer clocks H φ 1 and H φ 2's twh and twl.
* **10)** "two" is the overlap period of horizontal transfer clock H φ 2's twl and horizontal final stage transfer clock LH φ's twh'

Operating Characteristics (Ta = 25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	150	190		mV	1	
Saturation signal	Vsat	500			mV	2	Ta = 60℃
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta = 60℃
Dark signal shading	Δ Vdt			1	mV	6	Ta = 60℃
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone chart of Video signal shading

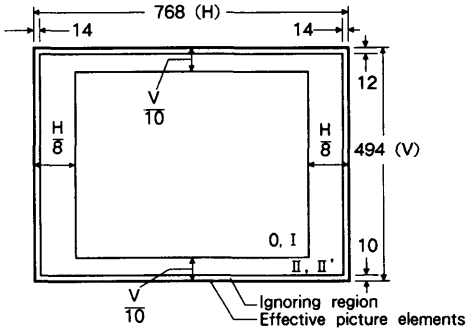


Image Sensor Characteristics Test Method

◎Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained at Ⓐ point in the figure of the Drive Circuit are utilized.

◎Definition of standard imaging conditions

① Standard imaging condition I : (As imaging device) Use a pattern box (luminance 706 Nit, color temperature 3200k Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (1.0mmt) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Signal output average value in this condition is called V_A.

② Standard imaging condition II : Image a light source (color temperature of 3200k) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (1.0mmt) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A), then test signal output minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A). Stop read out clock. When the charge drain executed by the electric shutter at the respective H blankings takes place, test the maximum value Vsm of signal output.

   $$Sm = \frac{Vsm}{V_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax) and minimum (Vmin) values of signal output.

   $$SH = (Vmax - Vmin)/V_A \times 100\ (\%)$$

5. Dark signal
   Test signal output average value Vdt when the device ambient temperature is at 60℃ and light is obstructed with horizontal idle transfer level as reference.

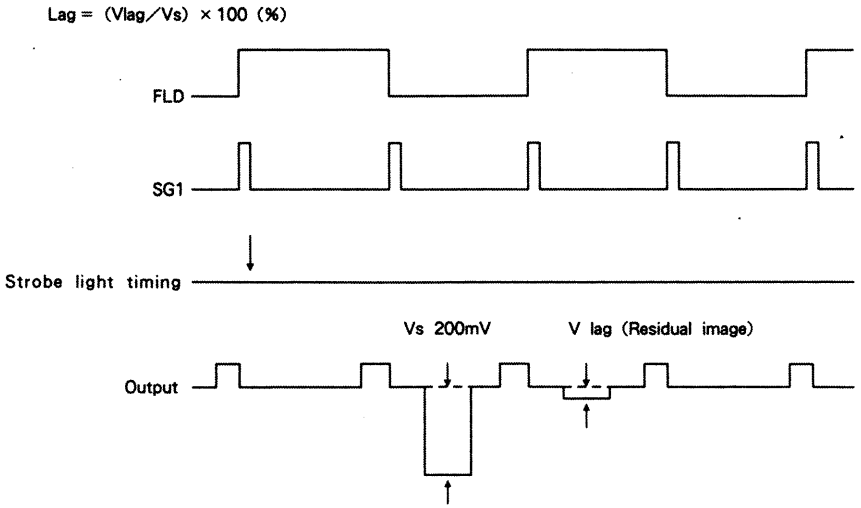
6. Dark signal shading
   Following 5, test maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

   $$\Delta Vdt = Vdmax - Vdmin$$

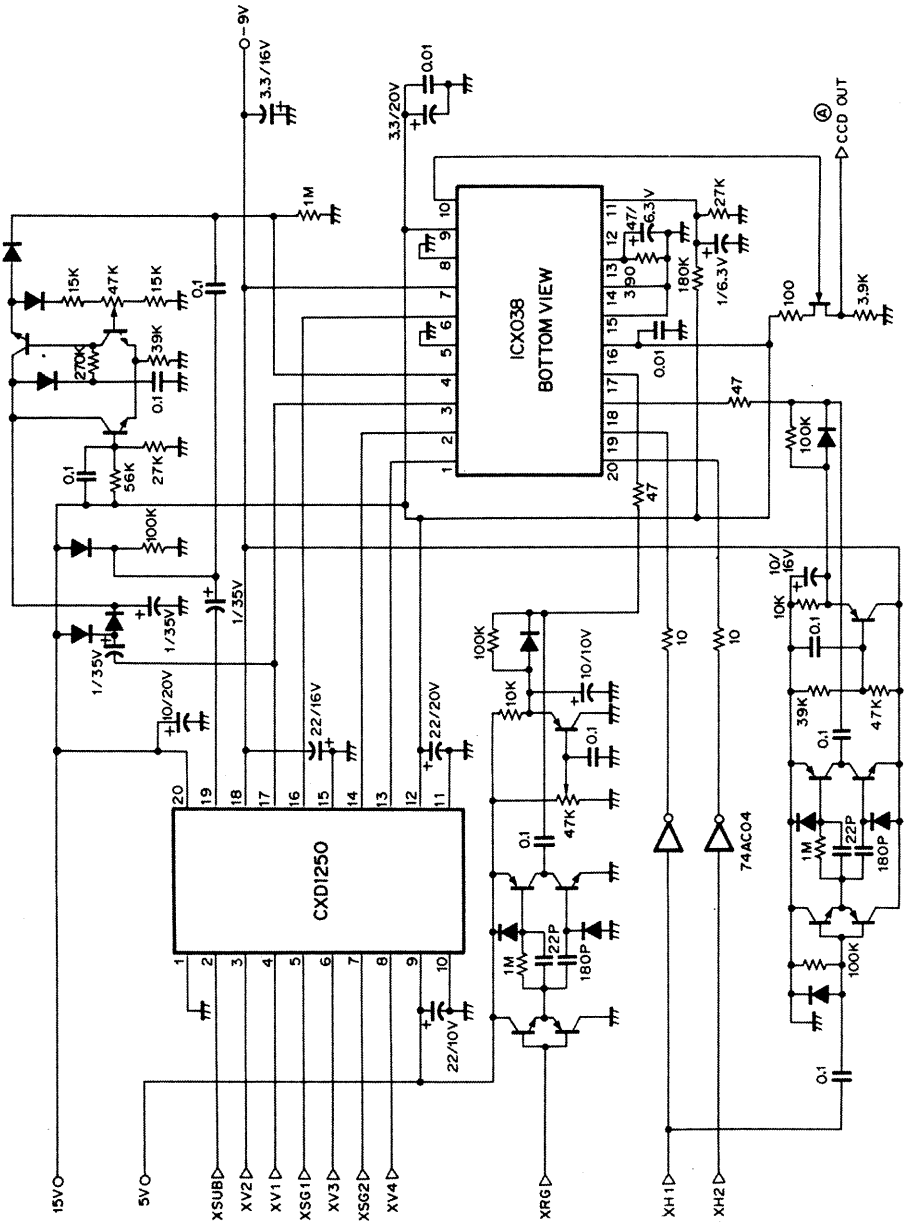
7. Flicker
Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A). Then test the signal output difference (ΔVf) between even field and odd field.

$$F = (\Delta Vf / V_A) \times 100\ (\%)$$

8. Residual image
Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

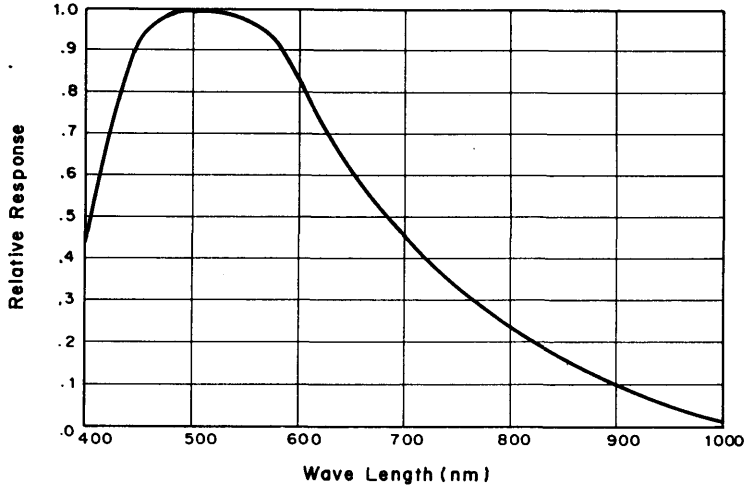


Drive Circuit

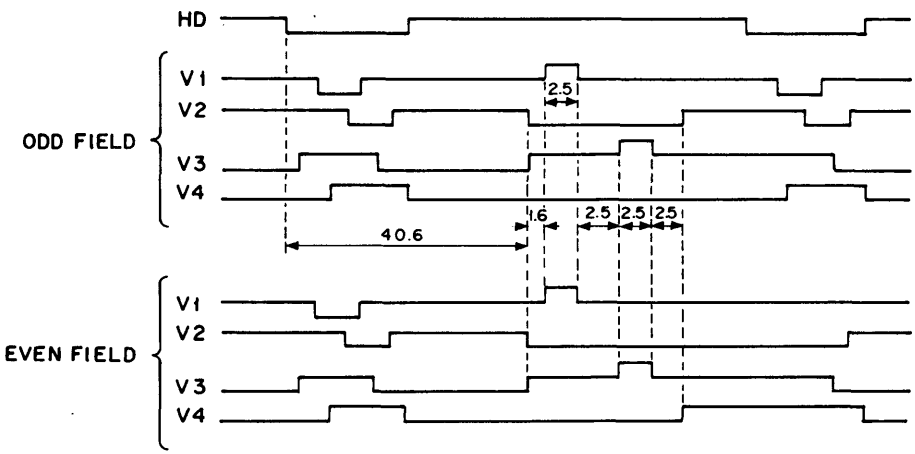


Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

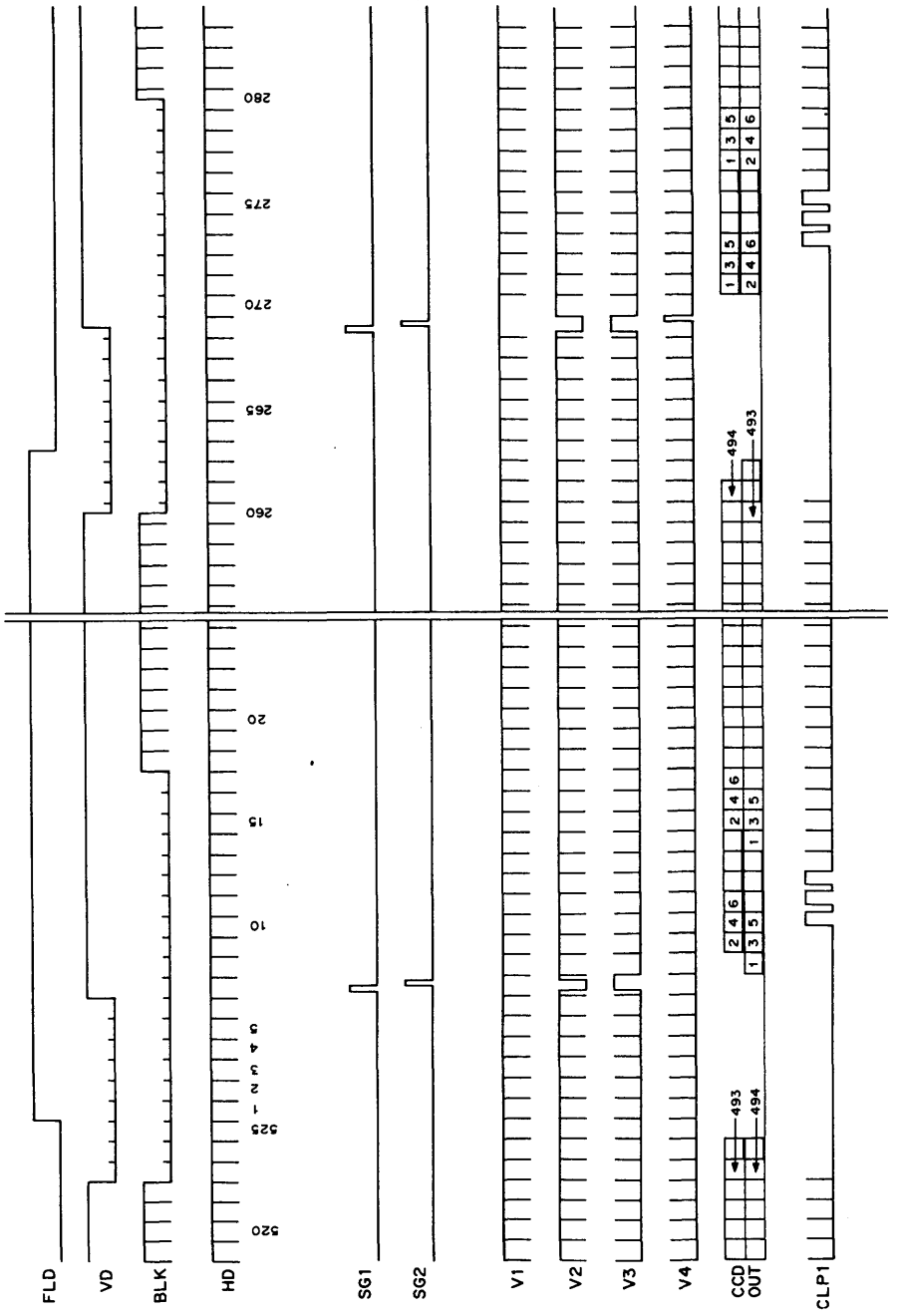


Using read out clock timing chart

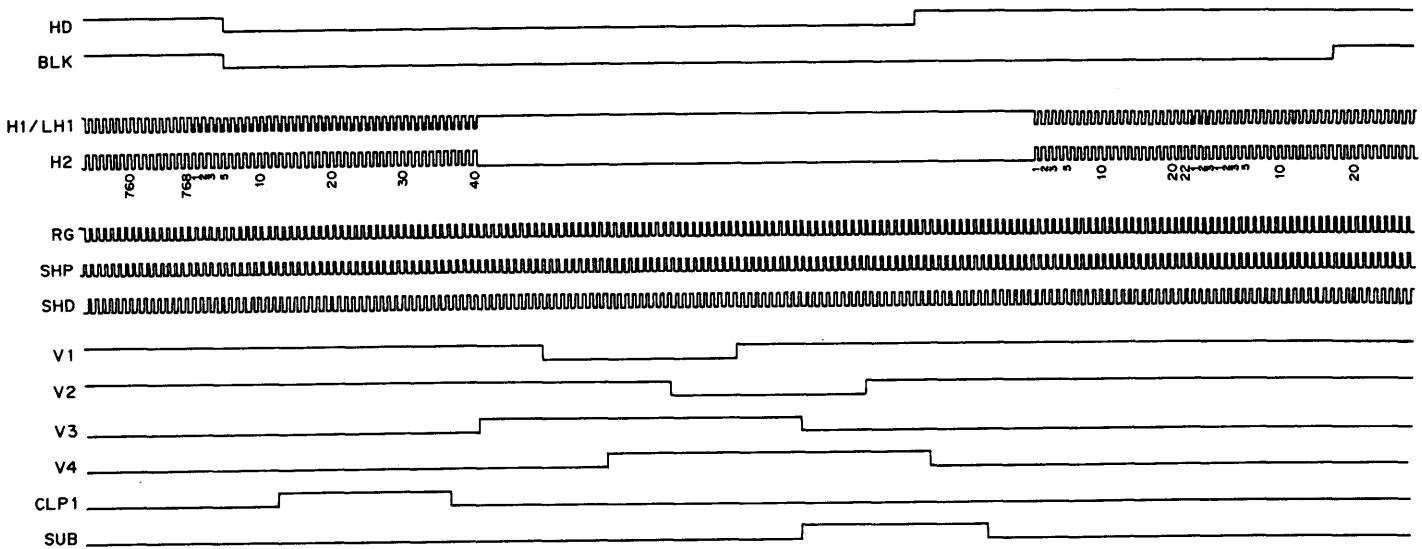


Unit : μs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



SONY®

ICX038AL

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80℃.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor.
Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect, there is no ROM or serial number.

Solid-State Image Sensor for B/W Camera

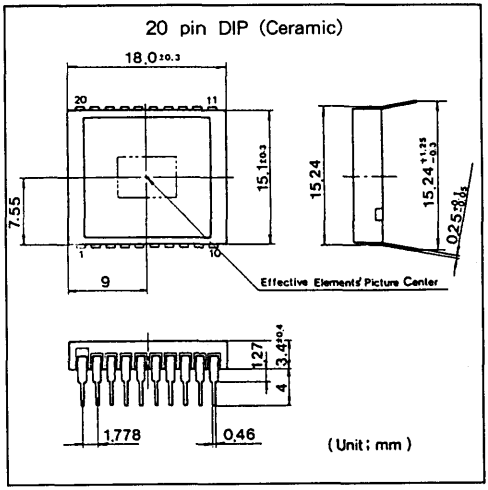
Description

ICX039AL is an interline transfer CCD solid-state imager suitable for CCIR 1/2 inch B/W video cameras. High sensitiveness is achieved through the adoption of HAD (Hole - Accumulation Diode) sensors.

This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

Pakage Outline

Unit : mm

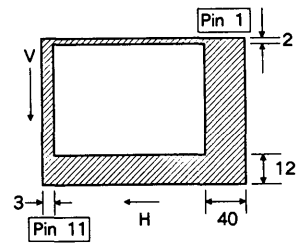


Features

- High image, high sensitivity and low dark current
- Consecutive various speed shutter
  1/50sec.(Typ.), 1/100sec. to 1/10000sec.
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

Device Structure

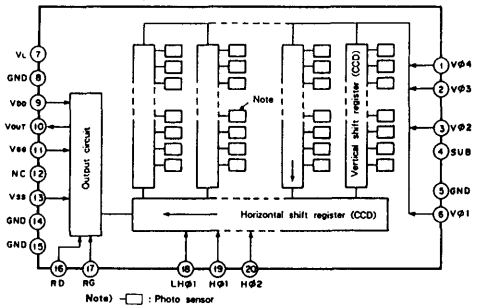
- Optical size 1/2 inch format
- Number of effective pixels
  752 (H) × 582 (V) Approx. 440k pixels
- Number of total pixels
  795 (H) × 596 (V) Approx. 470k pixels
- Interline transfer CCD image sensor
- Chip size 7.95mm (H) × 6.45mm (V)
- Unit cell size 8.6 μm (H) × 8.3 μm (V)
- Optical black Horizontal (H) direction Front 3 pixels Rear 40 pixels
  Vertical (V) direction Front 12 pixels Rear 2 pixels
- Number of dummy bits Horizontal 22
  Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

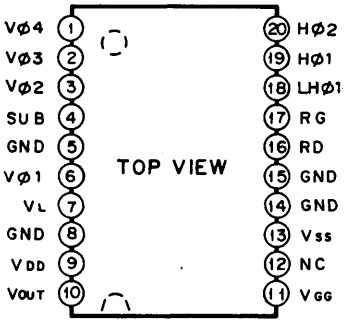
E89X34 – ST

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	V φ 4	Vertical register transfer clock	11	V_{GG}	Output amplifier gate bias
2	V φ 3	Vertical register transfer clock	12	NC	
3	V φ 2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	GND	GND
6	V φ 1	Vertical register transfer clock	16	RD	Reset drain bias
7	V_L	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	LH φ 1	Horizontal register final stage transfer clock
9	V_{DD}	Output amplifier drain supply	19	H φ 1	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	H φ 2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		− 0.3 to + 55	V	
Supply voltage	V_{DD}, V_{RD}, V_{OUT}, Vss − GND	− 0.3 to + 18	V	
	V_{DD}, V_{RD}, V_{OUT}, Vss − SUB	− 55 to + 10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4 − GND	− 15 to + 20	V	
	V φ 1, V φ 2, V φ 3, V φ 4 − SUB	to + 10	V	
Voltage difference between vertical clock input pins		to + 15	V	* (Max.)
Voltage difference between horizontal clock input pins		to + 17	V	
H φ 1, H φ 2 − V φ 4		− 17 to + 17	V	
LH φ 1, RG, V_{GG} − GND		− 10 to + 15	V	
LH φ 1, RG, V_{GG} − SUB		− 55 to + 10	V	
V_L − SUB		− 65 to + 0.3	V	
Beside GND, SUB-V_L		− 0.3 to + 30	V	
Storage temperature		− 30 to + 80	℃	
Operating temperature		− 10 to + 60	℃	

* **Note)** + 27V (Max.) when clock width < 10 μs, duty factor < 0.1 %.

Bias Conditions

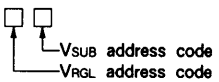
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 390 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0.5		5.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*3				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*** 2)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ±3%.

V_{SUB} code address − 1 digit display
V_{RGL} code address − 1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	0	1	2	3	4	5	6	7	8	9
Numerical value	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

< Example > "5L" → V_{RGL} = 3.0V
V_{SUB} = 12.0V

*** 3)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

*4) 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss and SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to Vϕ1, Vϕ2, Vϕ3, Vϕ4, Hϕ1 and Hϕ2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, LHϕ1 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

*5) Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

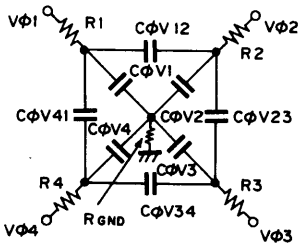
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	−0.05	0	0.05	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VH3}, V_{VH4}	−0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	−9.6	−9.0	−8.5	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	VϕV	8.3	9.0	9.65	V	2	VϕV = $V_{VHn}-V_{VLn}$ (n = 1 to 4)
	$\lvert V_{VH1}-V_{VH2}\rvert$			0.1	V	2	
	$V_{VH3}-V_{VH}$	−0.25		0.1	V	2	
	$V_{VH4}-V_{VH}$	−0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	VϕH	4.75	5.0	5.25	V	3	
	V_{HL}	−0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	V_{LHH}	4.45	5.0	5.55	V	4	
	V_{LHL}	−4.7	−4.0	−3.5	V	4	
	VϕLH	8.0	9.0	10.0	V	4	
Reset gate clock voltage	VϕRG	4.5	5.0	5.5	V	5	*6
	$V_{RGLH}-V_{RGLL}$			0.8	V	5	Low level coupling
Substrate clock voltage	VϕSUB	23.0	24.0	25.0	V	6	

*6) No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

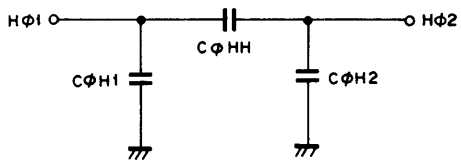
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	−0.2	0	0.2	V	5	
	$V_{\phi RG}$	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1800		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		2200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		450		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		270		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		62		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH}$		8		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		68		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	



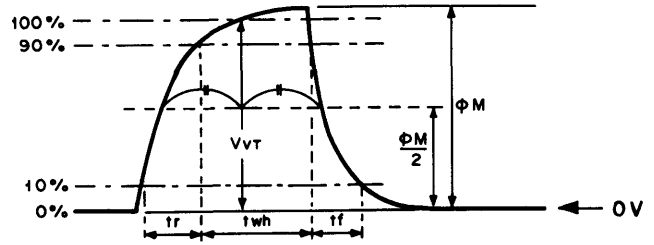
Vertical transfer clock equivalent circuit



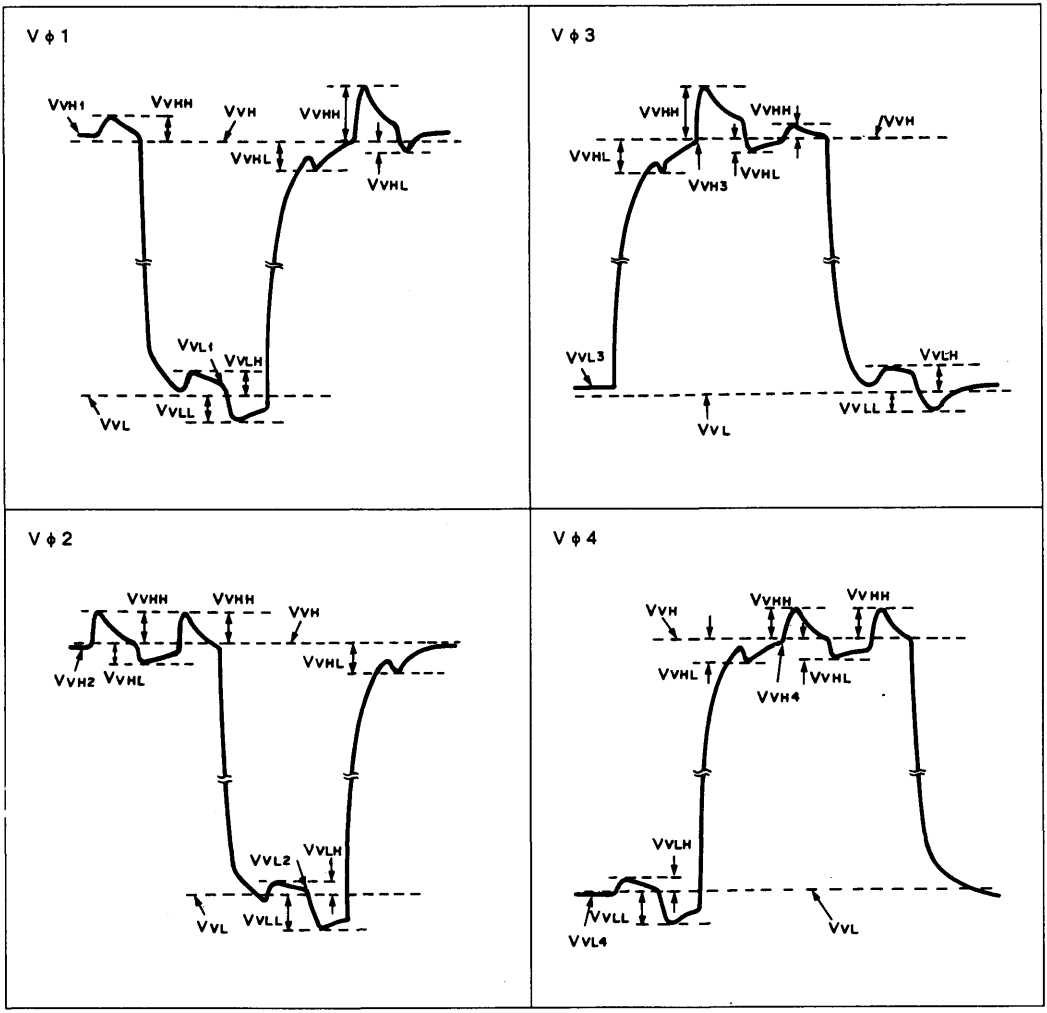
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

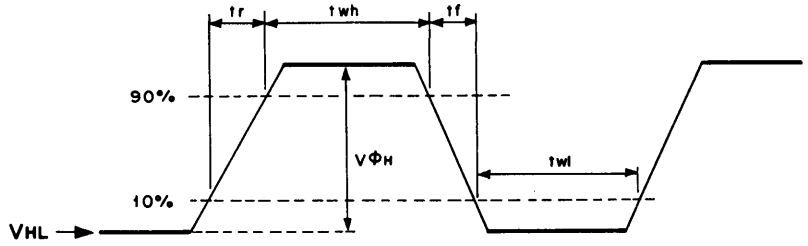
(1) Read out clock waveform



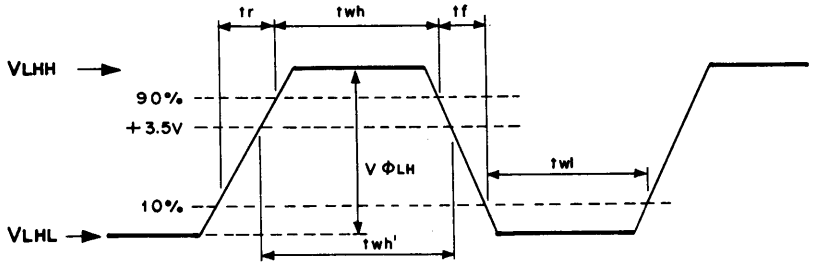
(2) Vertical transfer clock waveform



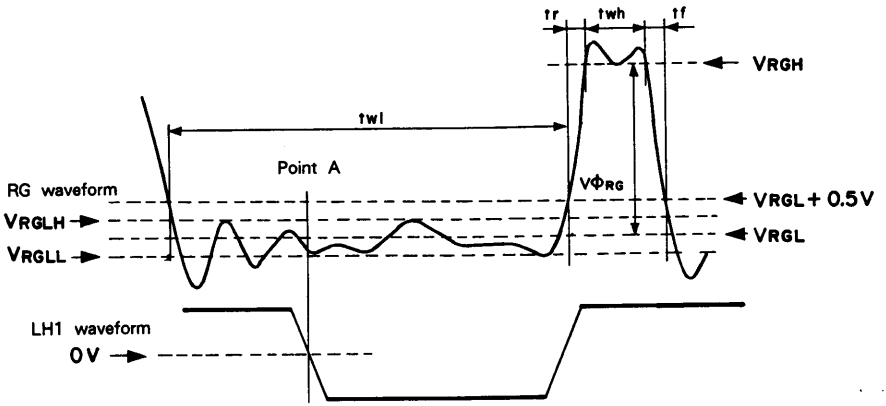
(3) Horizontal transfer clock waveform diagram



(4) Horizontal final stage transfer clock waveform diagram



(5) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

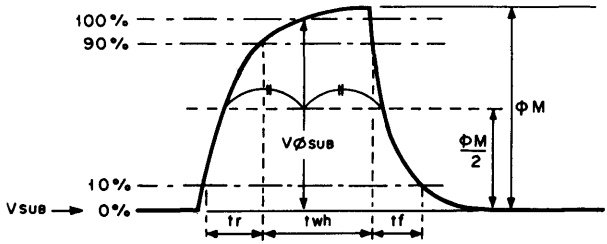
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

V_{RGH} is the minimum value for twh period.

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(6) Substrate clock waveform



Clock switching characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		μs	During read out
Vertical transfer clock	V φ 1, V φ 2, V φ 3, V φ 4										0.015		0.25	μs	* 7
Horizontal transfer clock	H φ		20			20			15	19	*8	15	19	ns	During imaging
Horizontal final stage clock	LH φ		24		22	27			10			9		ns	During imaging
Horizontal transfer /horizontal final stage clock	H φ 1, LH φ		5.38						0.01			0.01		μs	During parallel serial conversion.
Horizontal transfer clock	H φ 2					5.38			0.01			0.01		μs	
Reset gate clock	φ RG	11	13			51			3			3		ns	
Substrate clock	φ SUB	1.5	1.8							0.5			0.5	μs	During charge drain.

* **7)** When vertical transfer clock driver CXD1250 is in use.
* **8)** tf ≧ tr − 2 ns

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H φ	16	20		ns	*9
Horizontal transfer/ horizontal final stage clock	H φ 2, LH φ	15	20		ns	*10

* **9)** "two" is the overlap period of horizontal transfer clocks H φ 1 and H φ 2's twh and twl.
* **10)** "two" is the overlap period of horizontal transfer clock H φ 2's twl and horizontal final stage transfer clock LH φ's twh'

Operating Characteristics

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	140	180		mV	1	
Saturation signal	Vsat	450			mV	2	Ta = 60°C
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta = 60°C
Dark signal shading	Δ Vdt			1	mV	6	Ta = 60°C
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone chart of Video signal shading

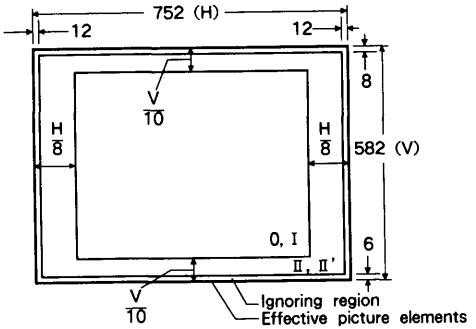


Image Sensor Characteristics Test Method

◎Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained at Ⓐ point in the figure at the Drive Circuit are utilized.

◎Definition of standard imaging conditions

① Standard imaging condition I : (As imaging device) Use a pattern box (luminance 706 Nit, color temperature 3200k Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (1.0mmt) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Signal output average value in this condition is called V_A.

② Standard imaging condition II : Image a light source (color temperature of 3200k) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (1.0mmt) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A), then test signal output minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A). Stop read out clock. When the charge drain executed by the electric shutter at the respective H blankings takes place, test the maximum value Vsm of signal output.

   $$Sm = \frac{Vsm}{V_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax) and minimum (Vmin) values of signal output.

   $$SH = (Vmax - Vmin)/V_A \times 100\ (\%)$$

5. Dark signal
   Test signal output average value Vdt when the device ambient temperature is at 60℃ and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
   Following 5, test maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

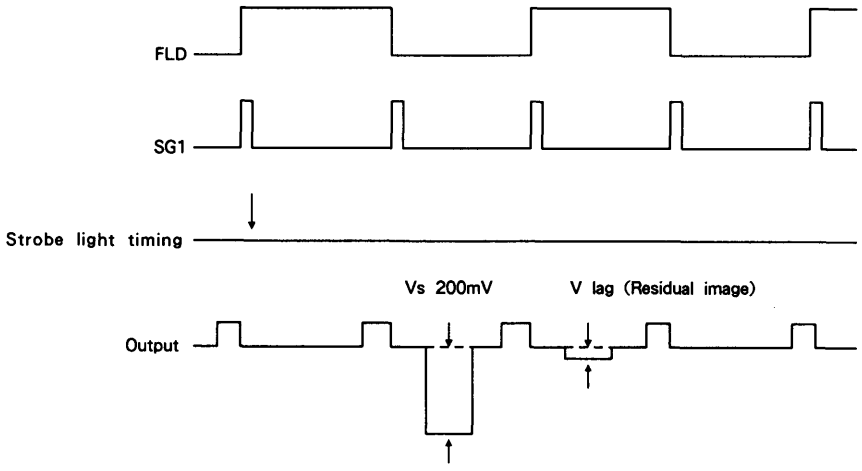
   $$\Delta Vdt = Vdmax - Vdmin$$

7. Flicker
Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A). Then test the signal output difference (ΔVf) between even field and odd field.

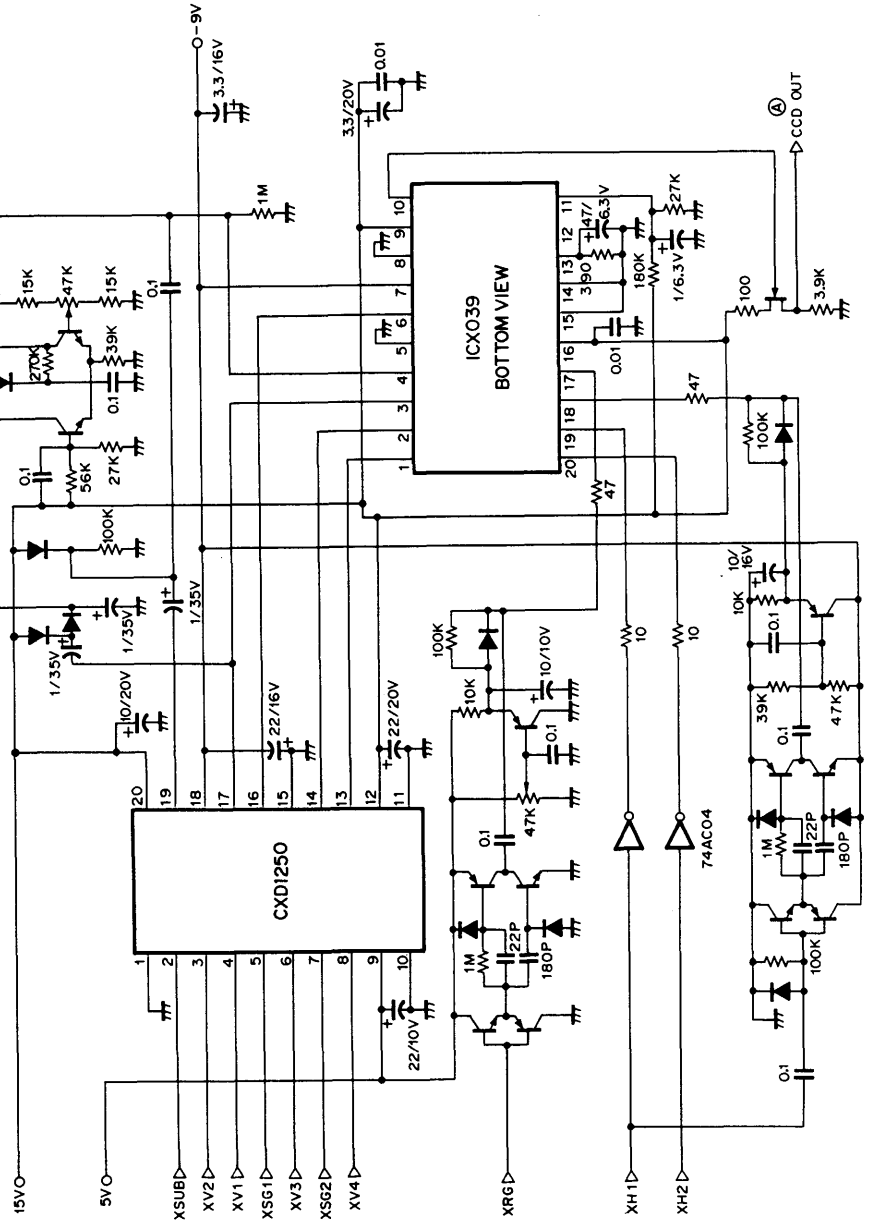
$$F = (\Delta Vf / V_A) \times 100\ (\%)$$

8. Residual image
Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag/Vs) × 100 (%)

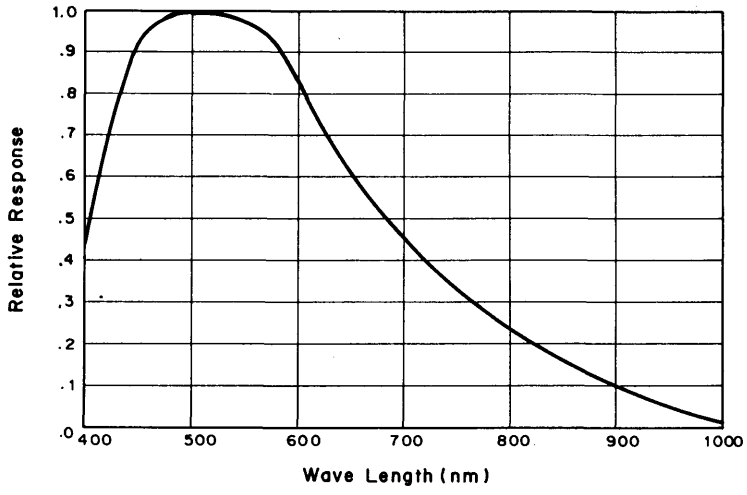


Drive Circuit

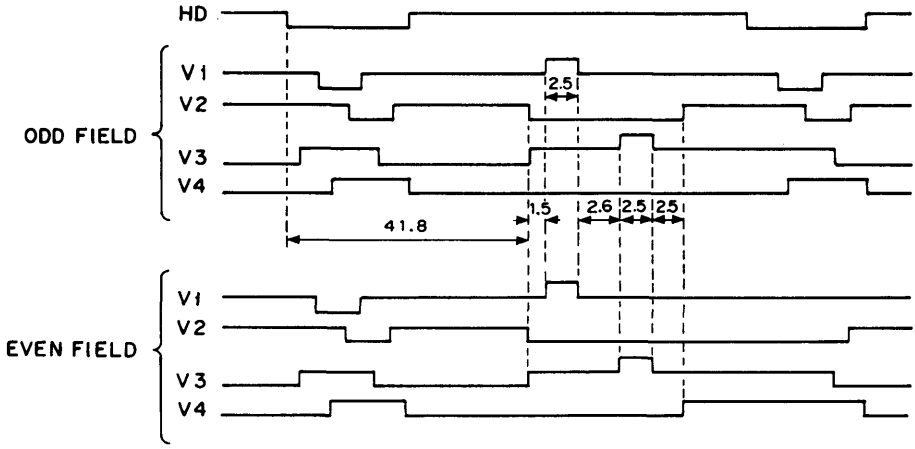


Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

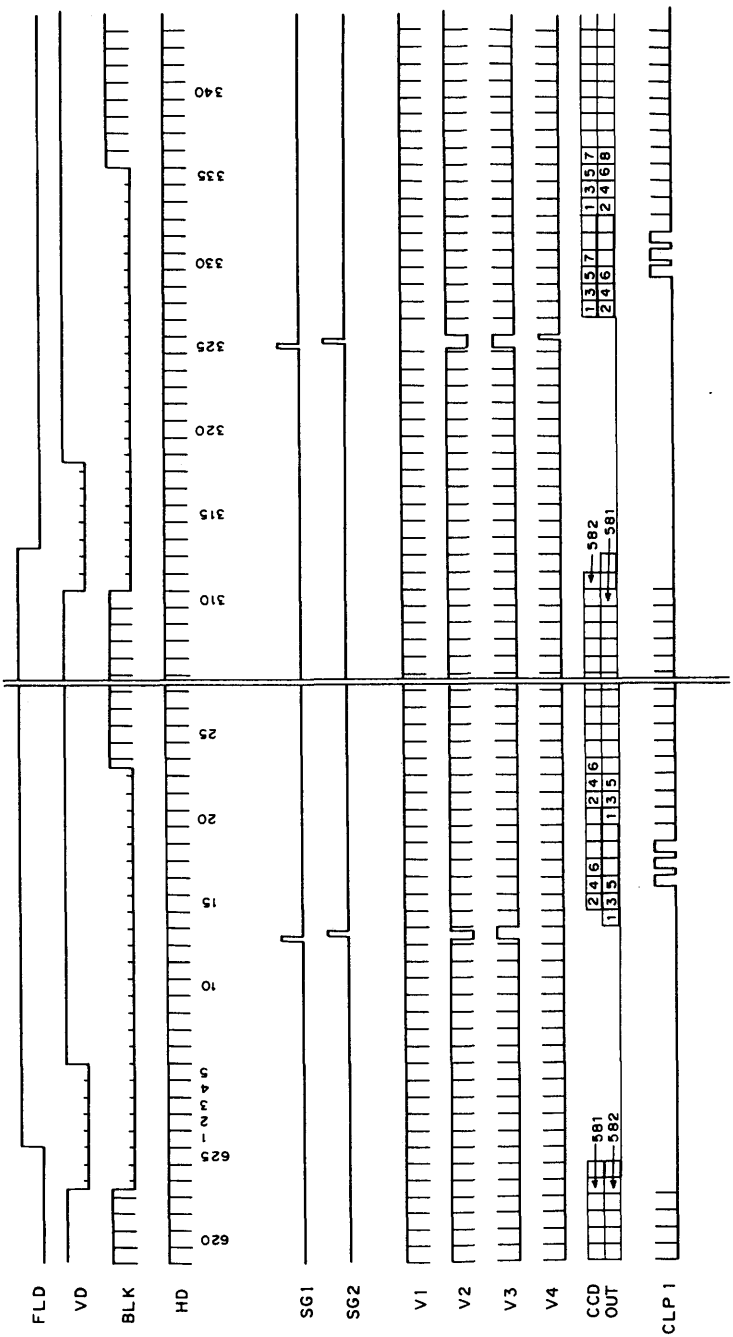


Using read out clock timing chart

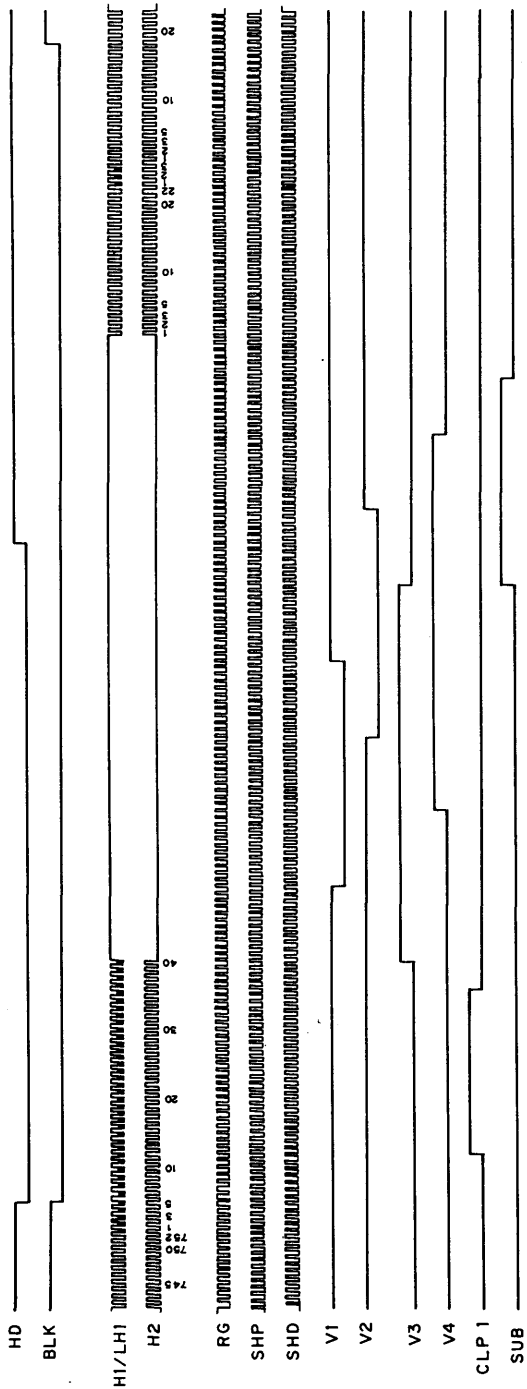


Unit : μs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80℃.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

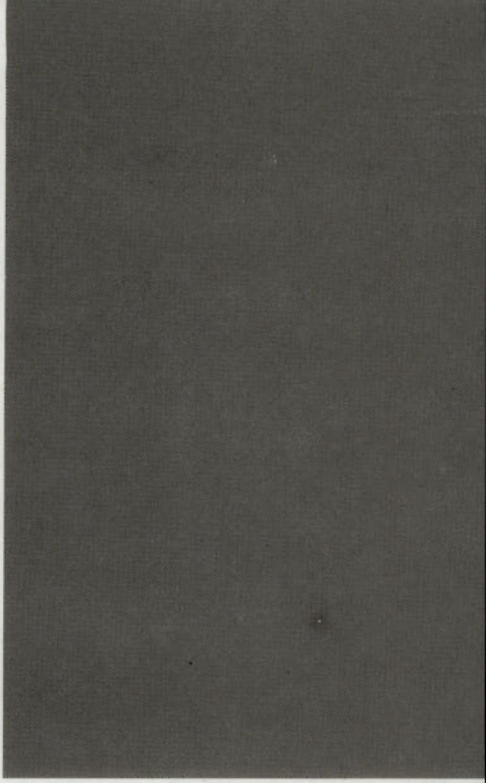
3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

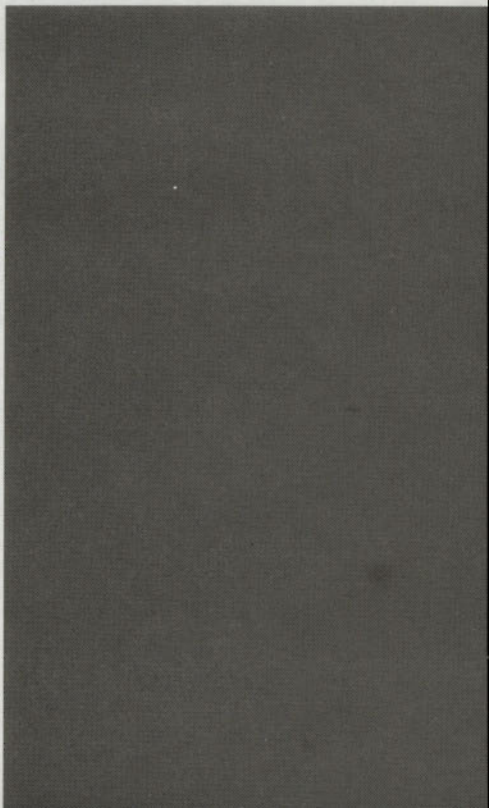
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor.
Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect, there is no ROM or serial number.



CCD Camera (Color)



2) CCD Camera (Color)

Type	Application	Function				Page
		Optical size (inch)	TV System	Picture elements (H×V)	Remarks	
ICX018CK	CCD Image Sensor for color	2/3	NTSC	510×492		149
ICX021CK		2/3	PAL	500×582		
IU018CK-AB	CCD Image Sensor for color unit	2/3	NTSC	510×492	Optical low-pass filter IR cut filter	161
IU021CK-AB		2/3	PAL	500×582	Optical low-pass filter IR cut filter	
ICX022AK-3	CCD Image Sensor for color	2/3	NTSC	768×493		164
ICX024AK-3	CCD Image Sensor for color	2/3	PAL	756×581		179
IU022AK-30A IU022AK-40A	CCD Image Sensor for color unit	2/3	NTSC	768×493	Optical low-pass filter IR cut filter	194
IU024AK-30A IU024AK-40A		2/3	PAL	756×581	Optical low-pass filter IR cut filter	
ICX022AN-3	CCD Image Sensor for color	2/3	NTSC	768×493		197
ICX024AN-3	CCD Image Sensor for color	2/3	PAL	756×581		214
ICX026BK	CCD Image Sensor for color	1/2	NTSC	510×492	600mil shrink package	231
ICX027BK	CCD Image Sensor for color	1/2	PAL	500×582	600mil shrink package	246
ICX038AK	CCD Image Sensor for color	1/2	NTSC	768×494	600mil shrink package	261
ICX039AK	CCD Image Sensor for color	1/2	PAL	752×582	600mil shrink package	278

SONY ICX018CK/ICK021CK

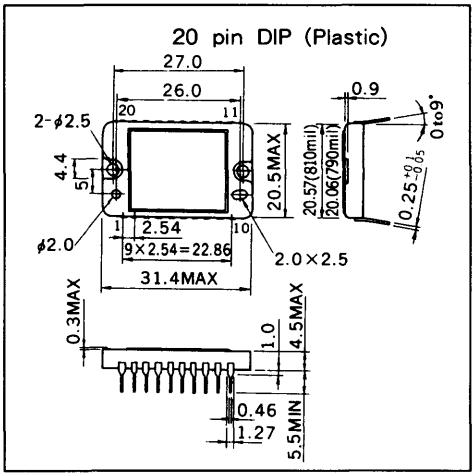
Solid-State Image Device for NTSC/CCIR Color TV System

Description

ICX018CK and ICX021CK are interline transfer CCD solid-state imaging devices developed for NTSC one-chip color cameras. The color coding of G-stripe, R/B line sequential system.
ICX018CK : for NTSC
ICX021CK : for CCIR

Package Outline

Unit : mm



Features

- Number of effective pixels
  ICX018CK : 510 (H) × 492 (V)
  ICX021CK : 500 (H) × 582 (V)
- Number of optical black elements

Horizontal (H) direction	ICX018CK	ICX021CK
in front	2 pixels	2 pixels
in back	20 pixels	30 pixels
Vertical (V) direction		
in front	12 pixels	14 pixels

- High sensitivity
- Low smear
- Anti-blooming
- Low lag, no burning
- Resistance to electro-magnetic field and microphonic noise.
- Precise image geometry
- γ characteristic 1
- ROM for blemish compensation and correlated double sampling attached with the device.

Layout of Optical Black Elements

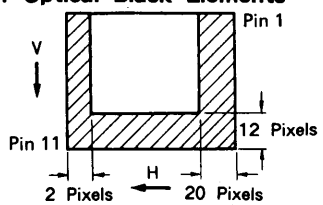


Fig. 1-a. ICX018CK (NTSC)

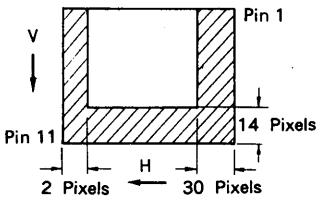


Fig. 1-b. ICX021CK (CCIR)

Device Organization

- Interline transfer CCD image sensor
- Unit cell size
  ICX018CK: 17 µm (H) × 13 µm (V)
  ICX021CK: 17 µm (H) × 11 µm (V)
- Number of dummy bits: 8 bits horizontal, 1 bit vertical (even field only)
- Chip size: 10.0 mm (H) × 9.3 mm (V)
- Thin polysilicon gate MOS diode sensor using the multi-layer interference effect.
- On-chip, high-sensitivity output amplifier
- Hybrid filter, G stripe, R/B line sequential
- P-sub, P-well structure

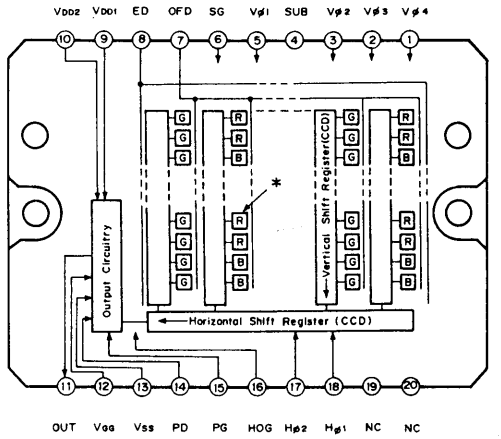
81103 – ST

Absolute Maximum Ratings

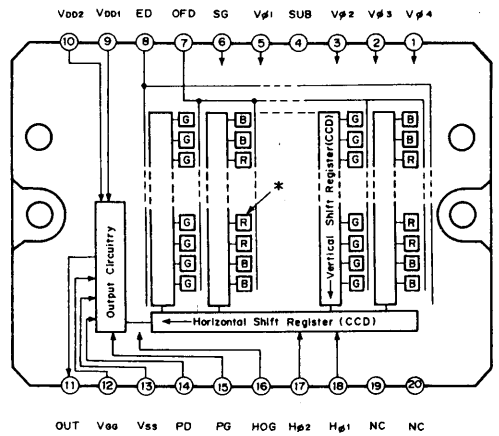
• Supply voltages V_{DD1}, V_{DD2}, and V_{PD}	−0.3 to +30 V	(SUB = 0V)
• Horizontal and vertical clock pins − SUB	−20 to +20 V	(SUB = 0V)
• Between horizontal clocks, between vertical clocks	22 V	(SUB = 0V)
• Horizontal and vertical clock pins − Sensor gate	18 V	(SUB = 0V)
• Pins other than those listed above	−0.3 to +20 V	(SUB = 0V)
• Storage temperature	−30 to +80 °C	
• Operating temperature	−10 to +55 °C	

Block Diagram and Pin Configuration (Top View)

ICX018CK



ICX021CK



* Note: □ ; Photosensor

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock input	11	OUT	Signal output*
2	Vφ3	Vertical register transfer clock input	12	V_{GG}	Output amplifier gate bias*
3	Vφ2	Vertical register transfer clock input	13	V_{SS}	Output amplifier source bias*
4	SUB	Substrate	14	PD	Output reset drain*
5	Vφ1	Vertical register transfer clock input	15	PG	Output reset clock*
6	SG	Sensor gate bias	16	HOG	Horizontal register read out control bias*
7	OFD	Anti-blooming bias*	17	Hφ2	Horizontal register transfer clock input
8	ED	Edge drain bias*	18	Hφ1	Horizontal register transfer clock input
9	V_{DD1}	Power supply*	19	NC	
10	V_{DD2}	Power supply*	20	NC	

* **Note)** Never supply negative voltage to pins.

DC Bias Conditions

(Some of the characteristics shown below are determined by the recommended circuit in Fig. 4. Refer to Note 1 through 8.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Substrate bias	V_{SUB}		0		V	V_{SUB} = GND
Output circuit supply voltages	V_{DD1}	19	20	21	V	$V_{DD1} = V_{DD2}$
	V_{DD2}	19	20	21	V	
	V_{PD}	17	18.1	19.2	V	Note 1
	V_{SS}	Grounded with 2.2 kΩ resistor				Note 2
	V_{GG}	7	9	10	V	Note 1
Anti-blooming bias	V_{OFD}	11	12	13	V	Note 3
Edge drain bias	V_{ED}					$V_{ED} = V_{OFD}$
HOG bias	V_{HOG}	0.8	1.0	1.2	V	
Sensor gate bias	V_{SG}	8.5	9.5	10.5	V	Note 3

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
DC supply current	I_{DD}		3.2	4	mA	Note 4
Input current 1	I_{in1}			1	μA	Note 5
Input current 2	I_{in2}			10	μA	Note 6

Clock Voltage Conditions

(Some of the characteristics shown below are determined by the recommended circuit in Fig. 4.)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Read out pulse	V_{VT}	11.0	13.0	14.0	V	Note 3
Vertical transfer clocks						
Low level	V_{VL}	−5.5	−5.0	−4.5	V	Note 3
Amplitude	$V\phi V$	6.8	7.5		V	
Horizontal transfer clocks						
Low level	V_{HL}	−4.4	−4.0	−3.6	V	
High level	V_{HH}	0.8	1.0	4.4	V	Note 7
Amplitude	$V\phi H$	4.75	5.0	8.8	V	Note 7
Output reset clock						
Low level	V_{PGL}	1.0	1.3	1.7	V	Note 8
High level	V_{PGH}	8.9	9.3	10.5	V	
Amplitude	V_{PG}	7.2	8.0	8.8	V	

Clock Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical transfer clock vs. GND	$C\phi V$		6200		pF	
Between vertical transfer clocks	$C\phi VV$		1800		pF	
Output reset clock	$C\phi PG$		14		pF	

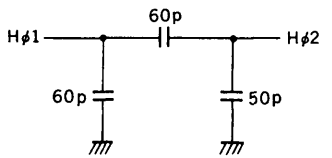


Fig. 3. Horizontal Transfer Clock Equivalent Circuit

Note)

1. V_{PD}, V_{GG} and V_{HOG} should be produced from V_{DD1}, and V_{DD2}. Resistance precision should be ±5%. See Figs. 4 and 5.
2. V_{SS} should be self-biased and should be connected to GND through a 2.2 kΩ (±5%) resistor.
3. $V_{VHH} \pm 5.1 \leqq V_{SG} \leqq V_{VT} - 1.5$ $V_{VT} \leqq V_{OFD} + 2$ (unit : V)
   V_{VHH} is the maximum level of the waveforms containing couplings of vertical transfer clocks V φ 1 to V φ 4 excluding the period in which a three level VT is pulsed.
4. Total output amplifier current, when the load resistance is 2.2 kΩ.
5. The current to the substrate when 20V is sequentially applied to pins V φ 1, V φ 2, V φ 3, V φ 4, H φ 1, and H φ 2.

6. The current to the substrate when 20V is applied to SG, ED, OFD, PD and HOG independently. The pins which have not been measured, should be connected to the ground.

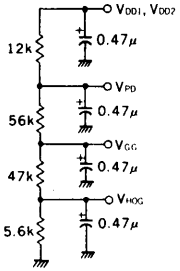


Fig. 4. Recommended Circuit for Bias Setting of VDD1, VDD2, VPD, VGG, and VHOG.

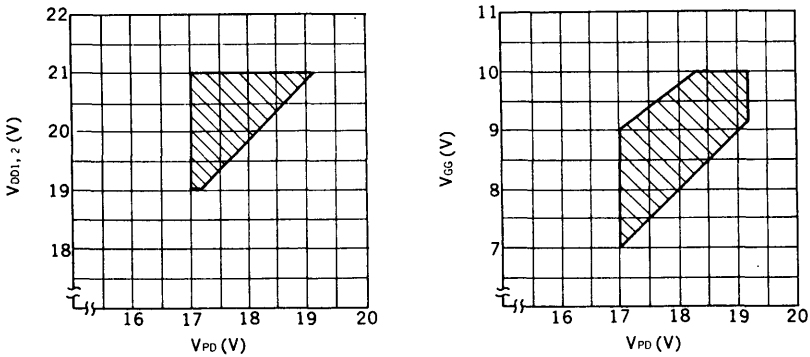


Fig. 5. Bias Setting Range of VDD1, VDD2, VPD, and VGG.
The shaded section is the recommended operating range.

7. V_{HH}, $V_{\phi H}$, and V_{HL} are determined as follows.

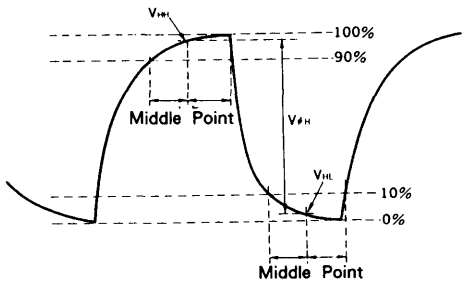


Fig. 6. Horizontal Transfer Clock Waveform

8. V_{PGL}, V_{PGH}, and $V_{\phi PG}$ are determined as follows.

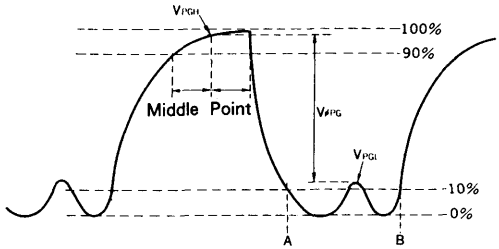


Fig. 7. Output Reset Clock Waveform

V_{PGL} is defined by the maximum level between Points A and B. Be careful not to allow ringing on the low side to be less than 0V.

Drive Pulse Waveform Conditions (ICX018CK)

Symbol	tWH			tWL			tr			tf			Unit	Condition
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$H_{\phi 1}$		42			42			10			10		ns	During scanning time
$H_{\phi 2}$		42			42			10			10			
$H_{\phi 1}$		6.8						0.01			0.01		µs	During parallel-serial conversion
$H_{\phi 2}$		0						0			0			
PG	10	42			42			10			10		ns	Normally PG=$H_{\phi 1}$
$V_{\phi 1}/V_{\phi 2}$		61.2			2.1			0.1			0.1	0.5	µs	During scanning time
$V_{\phi 3}/V_{\phi 4}$		3.6			59.6			0.1			0.1	0.5		
$V_{\phi 1}/V_{\phi 3}$		19						1			1			During read out from sensor

Drive Pulse Waveform Conditions (ICX021CK)

Symbol	tWH			tWL			tr			tf			Unit	Condition
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$H_{\phi 1}$		43			43			10			10		ns	During scanning time
$H_{\phi 2}$		43			43			10			10			
$H_{\phi 1}$		6.87						0.01			0.01		µs	During parallel-serial conversion
$H_{\phi 2}$		0						0			0			
PG	10	43			43			10			10		ns	Normally PG=$H_{\phi 1}$
$V_{\phi 1}/V_{\phi 2}$		61.8			2.12			0.1			0.1	0.5	µs	During scanning time
$V_{\phi 3}/V_{\phi 4}$		3.64			60.2			0.1			0.1	0.5		
$V_{\phi 1}/V_{\phi 3}$		19.2						1			1			During read out from sensor

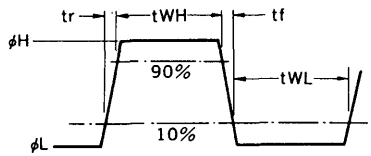


Fig. 8. Pulse Waveform

Operating Characteristics (ICX018CK) Ta = 25°C. See the Test Circuit.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Method	Condition
Sensitivity	Sg	75	110	145	mV	1	
	Rr	0.55	0.8	1.0		1	
	Rb	0.35	0.5	0.8		1	
Saturation output voltage	Vsat	400	530	850	mV	2	
Video signal shading	SV1		12	27	%	3	
Non-uniformity between color signal channels	Δ Srg			11	%	4	
	Δ Sbg			11	%	4	
Smear	SM		0.01	0.04	%	5	
Dark signal	Vdt			13	mV	6	Ta = 55°C
Dark signal shading	Δ Vdt			4	mV	7	Ta = 55°C
Flicker	F			6	%	8	

Operating Characteristics (ICX021CK) Ta = 25°C. See the Test Circuit.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Method	Condition
Sensitivity	Sg	65	95	125	mV	1	
	Rr	0.55	0.8	1.0		1	
	Rb	0.35	0.5	0.8		1	
Saturation output voltage	Vsat	360	440	850	mV	2	
Video signal shading	SV1		12	27	%	3	
Non-uniformity between color signal channels	Δ Srg			11	%	4	
	Δ Sbg			11	%	4	
Smear	SM		0.01	0.04	%	5	
Dark signal	Vdt			13	mV	6	Ta = 55°C
Dark signal shading	Δ Vdt			4	mV	7	Ta = 55°C
Flicker	F			6	%	8	

Test Method

- **Test conditions**
  1) The device drive conditions in the following measurements should be adjusted to the typical values of the DC and clock voltage conditions.(See Fig. 9).
  2) In measurements mentioned below, blemishes should be excluded. Unless specified, the optical black level should be the reference for the signal output, and the value measured at Point B in Fig. 9 should be used.
- **Definition of standard imaging condition**

  Standard imaging condition I : Use pattern box (brightness 706 nt, 3200° K Halogen source) at F5.6 with FUJINON lens H6 × 12.5D (F1.4). CM-500S (1.0 mmt) should be used as an IR cut filter.

  Standard imaging condition II : Uniformity of the light source within 2%. The light-source color temperature should be 3200° K, and CM-500S (1.0 mmt) should be used as an IR cut filter. The quantity of light should be adjusted to the average value of output voltage Vs shown in each item.

1. Set to the Standard imaging condition I and measure output signals (Sr, Sg, and Sb) in the center of the screen for the R, G, and B channels.
   $Rr \equiv Sr/Sg \qquad Rb \equiv Sb/Sg$
2. Set to the standard imaging condition II, adjust the intensity of light, check anti-blooming, then measure the minimum values of each color signal of the R, G, and B channels for the whole screen.
3. After setting up standard imaging condition II, set the pattern box on the entire screen and measure the maximum and minimum output voltages of Channels G (Vgmax, Vgmin) adjusting V_S to 300 mV.

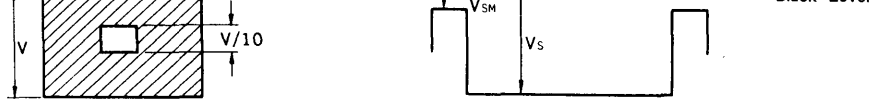
$$SV1 \equiv \frac{Vgmax - Vgmin}{V_S} \times 100\ (\%)$$

4. In accordance with Method 5, measure non-uniformity of R and B channels in various parts of the screen using Channel G as a standard. In measurements adjust the output gain for Channels R and B to that for G in terms of the average signal. Measure the maximum and minimum values of the difference with G.

$$\Delta Srg \equiv \frac{(Vr - Vg)\ max - (Vr - Vg)\ min}{V_S} \times 100\ (\%)$$

$$\Delta Sbg \equiv \frac{(Vb - Vg)\ max - (Vb - Vg)\ min}{V_S} \times 100\ (\%)$$

5. After setting up standard imaging condition II, set the pattern box on a vertical 1/10 screen. Measure the average signal voltage V_S of Channel G and maximum value V_{SM} of Channels R, G, and B of signal voltage during vertical blanking. (V_S = 300 mV, 1/10V method)



$$SM \equiv \frac{V_{SM}}{V_S} \times 100\ (\%)$$

6. Average dark signal at ambient temperature of 55°C.
7. Measure maximum and minimum dark signal (Vdmax, Vdmin). Blemishes should be excluded. The temperature should be 55°C.
   $\Delta Vdt \equiv (V_d max - V_d min)$
8. Measure the signal difference : ΔVf between even field and odd field, after setting up standard imaging condition II. (V_S = 300 mV)

$$F \equiv \frac{\Delta Vf}{V_S} \times 100\ (\%)$$

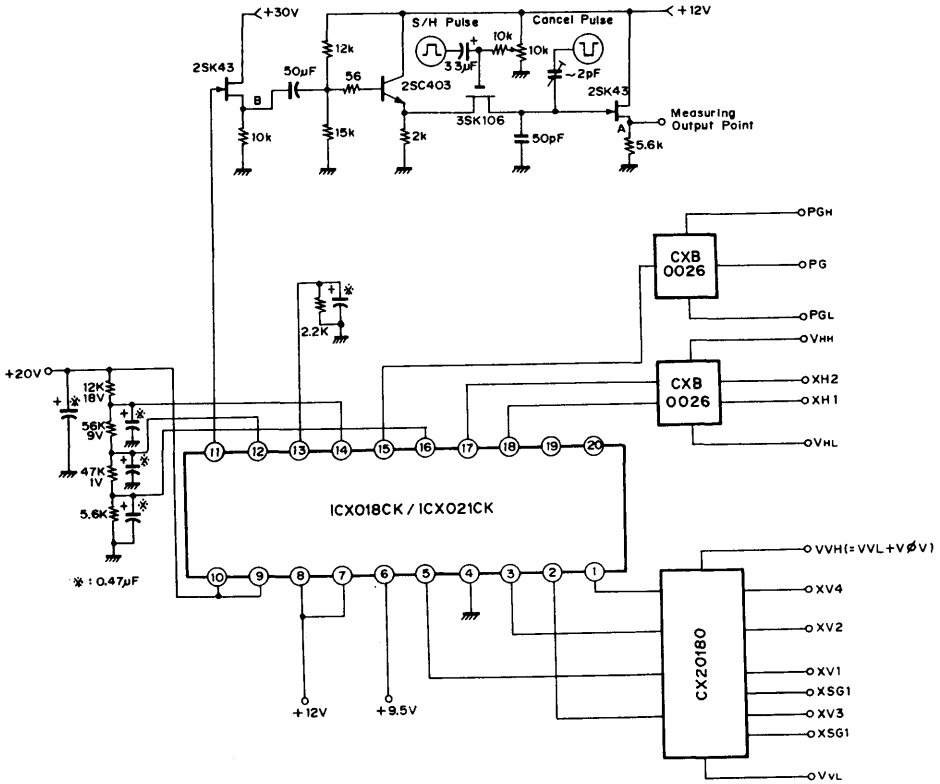
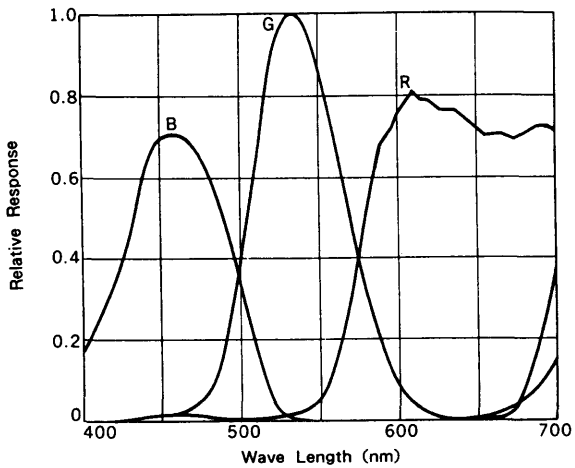


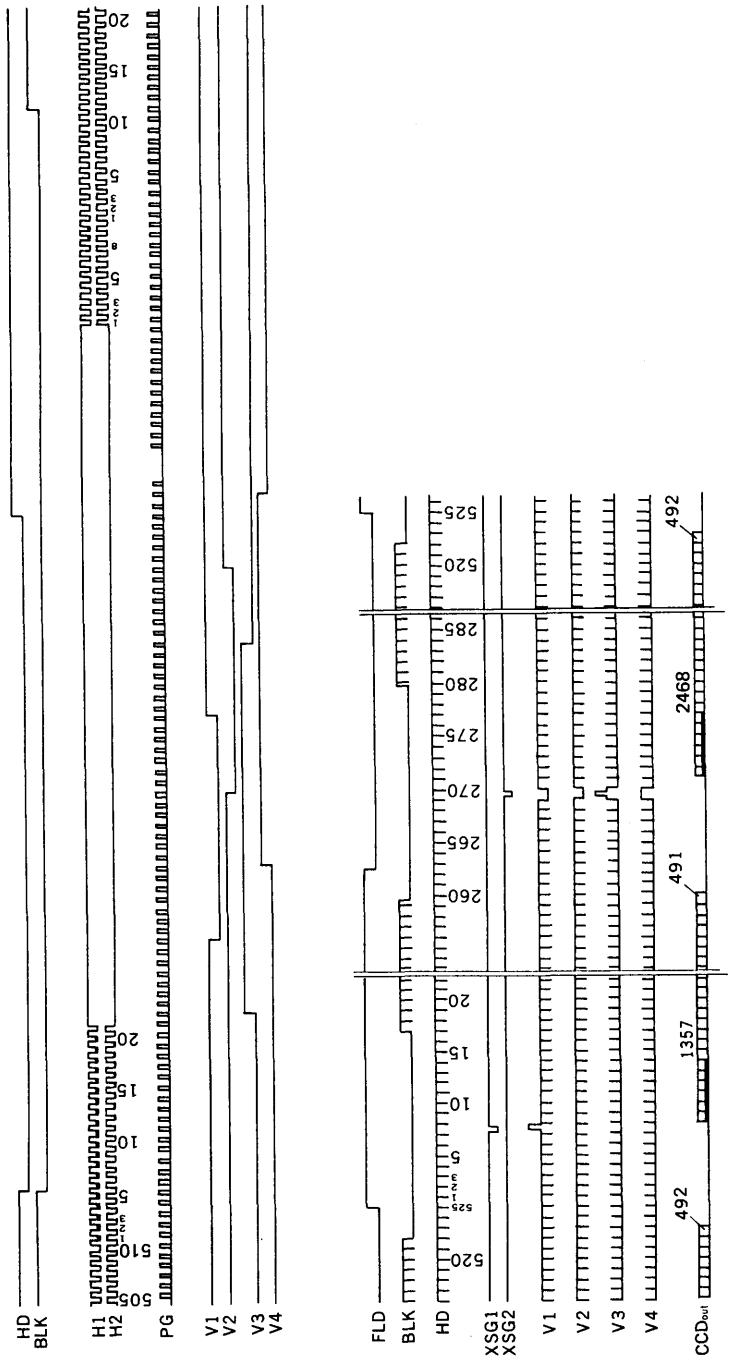
Fig. 9. Test Circuit

Note) XV1 denotes inverted level of V1. The others are the same.

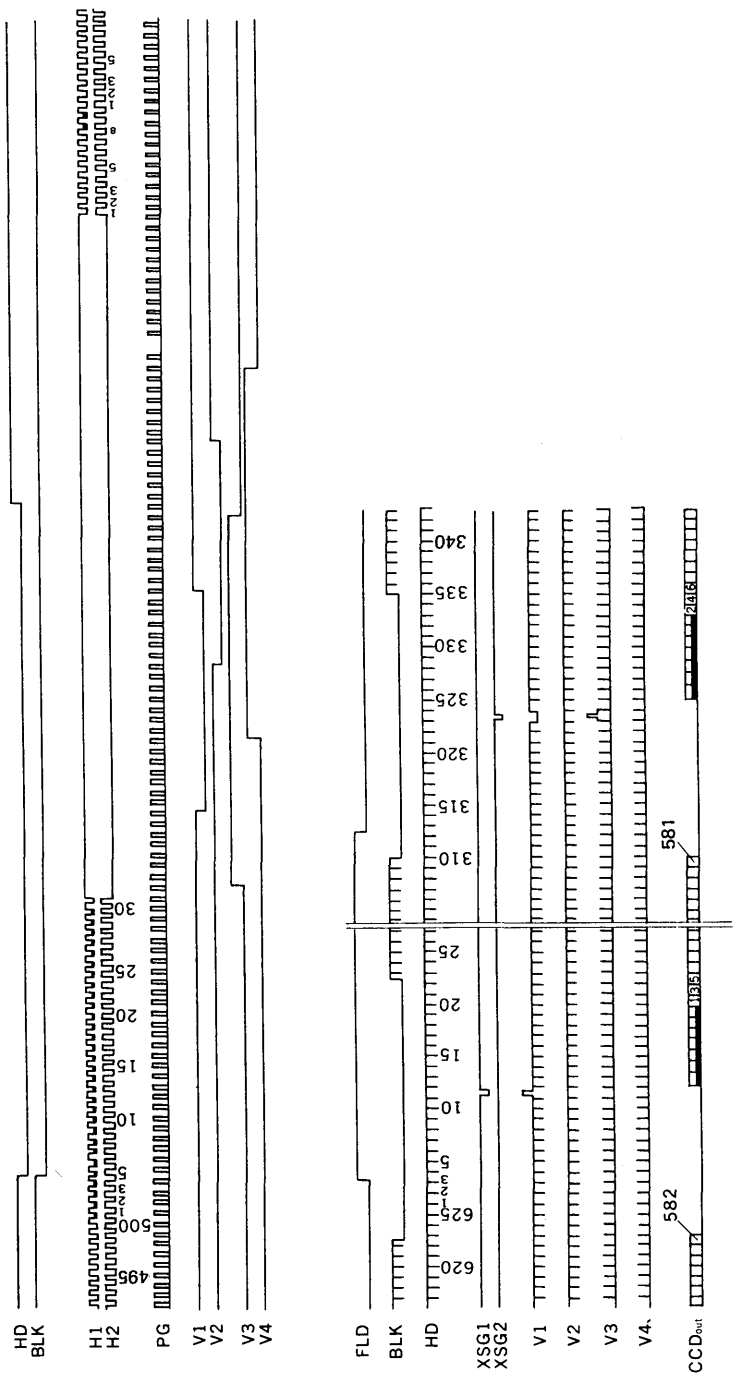
Typical Spectral Response (Light source characteristics are not included.)



Timing Chart (ICX018CK NTSC)



Timing Chart (ICX021CK CCIR)



Handling

1. Electrostatic Protection
   It is crucial that static discharge be controlled and minimized. Handle most carefully.
2. Soldering
   Make sure that the package temperature does not exceed 80℃. Solder dipping in a mounting furnace causes broken glass, filter delamination, and other defects. Use a grounded 30W soldering iron and solder in less than 2 seconds for each pin. Cool sufficiently when reworking or remounting.
3. Glass surface dust
   Do not touch glass plates. Be careful not to have objects contact glass surface. Clean with a cotton bud when the glass surface is stained. Do not use an organic solvent other than ethyl alcohol. Store in a special container to prevent dust and dirt. To prevent dew condensation, preheat or precool when moving to a room in which temperature difference is great.
4. ROM for blemish compensation and correlated double sampling.
   This device is shipped in a special container together with ROM. Be most careful about combination when remounting.
5. Care must be taken to avoid exposure to strong light for a long time.
6. Use CX20180 for V clock driver.

SONY IU018CK-AB/IU021CK-AB

CCD Imaging Blocks for Color Camera

Description

IU018CK-AB and IU021CK-AB are solid state imaging blocks developed for color video cameras. They incorporate an image correction optical filter (Optical crystal low pass filter, infrared cut filter) indispensable for solid state imaging devices.

These blocks can easily be attached to the rear of a lens or the mount of an interchangeable lens to provide a lightweight, compact imaging system.

Pin Configuration (Top View)

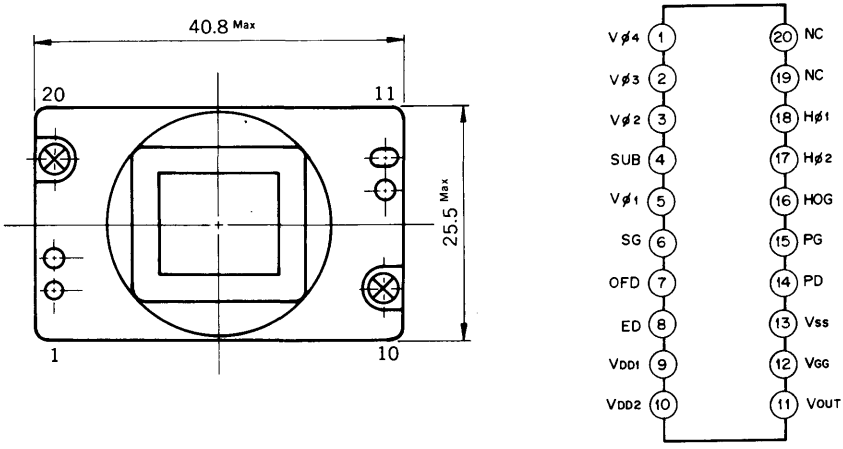


Fig. 1

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V_{\phi 4}$	Vertical register transfer clock input	11	V_{OUT}	Signal output
2	$V_{\phi 3}$	Vertical register transfer clock input	12	V_{GG}	Output amplifier gate bias
3	$V_{\phi 2}$	Vertical register transfer clock input	13	V_{SS}	Output amplifier source bias
4	SUB	Substrate	14	PD	Precharge drain bias
5	$V_{\phi 1}$	Vertical register transfer clock input	15	PG	Output reset clock input
6	SG	Sensor bias	16	HOG	Horizontal register read out control bias
7	OFD	Anti-blooming bias	17	$H_{\phi 2}$	Horizontal register transfer clock input
8	ED	Edge drain bias	18	$H_{\phi 1}$	Horizontal register transfer clock input
9	V_{DD1}	Supply voltage	19	NC	
10	V_{DD2}	Supply voltage	20	NC	

81018-HP

Package Outline (Unit : mm)

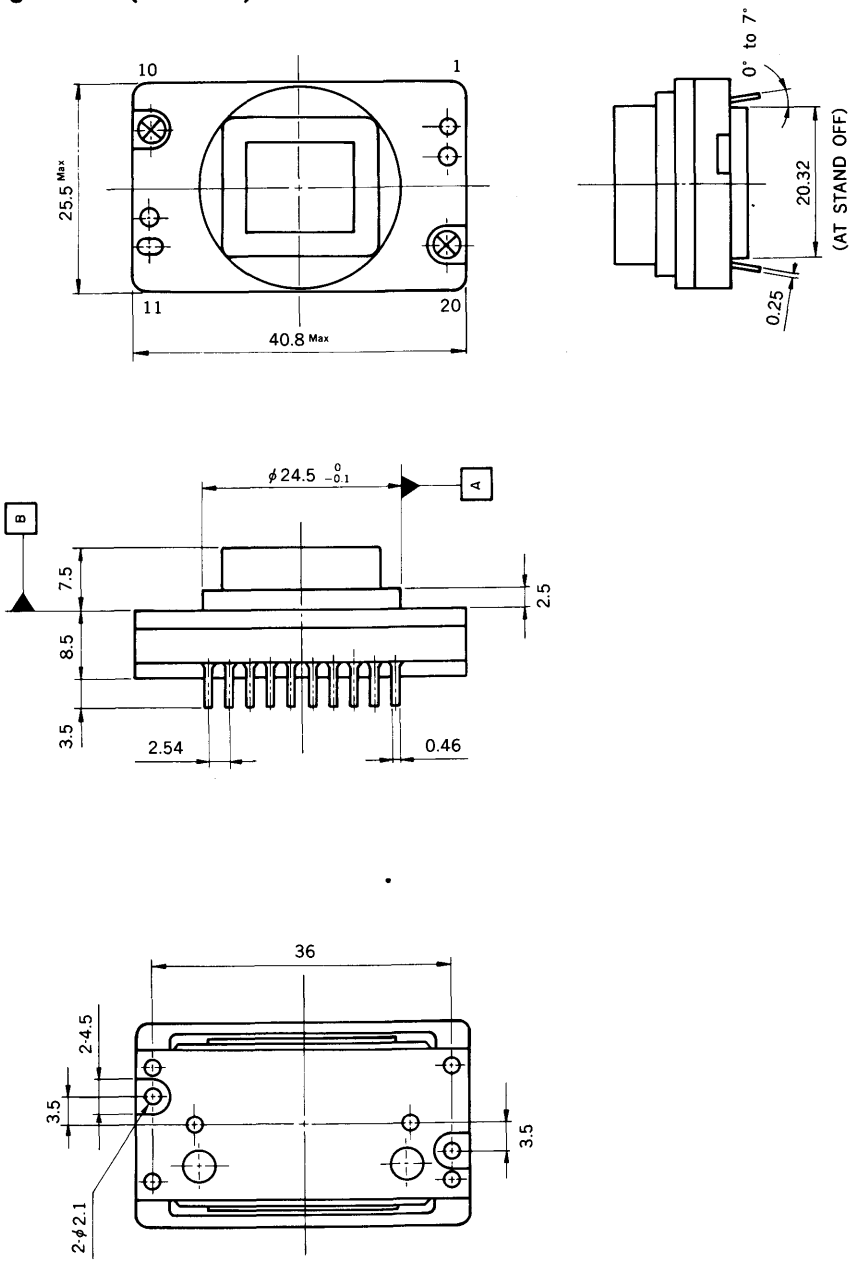


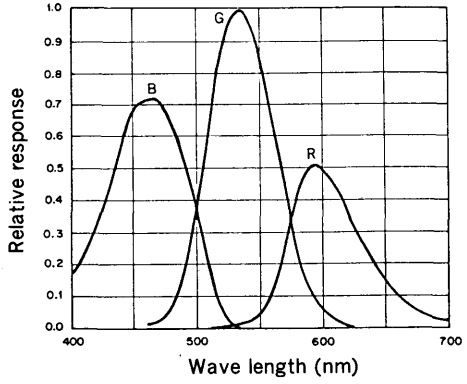
Fig. 2

Configuration and Optical Characteristics

Item	Ratings	Unit	Remark
Appearance, size, attachment	See the Package Outline (Fig. 2)		
Optical axis	Within the ϕ11.2 circle with the Ref. A center are the effective elements.	mm	Fig. 2 Standard location A
Image rotation	Within ±1	deg	ϕ2.1 spot
Back focus	1.74±0.3	mm	(In AIR) Fig. 2 Standard surface B
Tilt	60	μm	Fig. 2 Standard surface B
Optical thickness	9.75	mm	BK-7 equivalent (including optical filter assembly and optical parts of CCD)
Optical filter	Four-layer laminated type		
Spectral sensitivity characteristics	See Fig. 3		
Weight	24	g	

Note) See the specifications of ICX018CK and ICX021CK for Imaging Characteristics, Electrical Characteristics and Absolute Maximum Ratings.

Spectral sensitivity characteristics example



(Fig. 3)

Environmental Characteristics

Item	Condition	Requirements
Vibration	7G, 10 to 30Hz, 300sec sweep, each 15min for x, y, z directions	The above structure satisfies optical characteristics.
Impact	80G, in 6 directions	
Low temperature durability	−30°C, 240 hours	
High temperature durability	80°C, 240 hours	
Heat cycle	−30°C to 25°C to 80°C 30min to 5min to 30min 10cycles	
High temperature and high humidity durability	60°C, 95%, 240 hours	

Interline-type CCD Solid Image Sensor

Description

ICX022AK-3 is an interline-type CCD solid imaging device designed for color video cameras.
Effective pixels number 768 horizontally and 493 vertically.

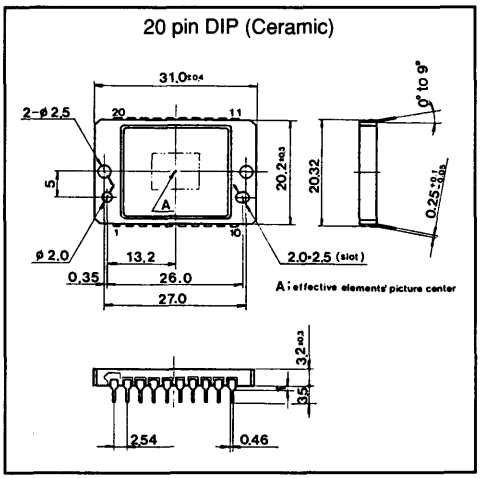
Color filters incorporated Ye, G and Cy are vertical stripe filters of high resolution and high sensitivity.

The device employs the field integration system to obtain a high resolution.

Element Structure

- Interline type CCD image sensor
- Effective pixels: 768 (H) x 493 (V)
- Image size: 2/3 inches (8.8 mm (H) x 6.6 mm (V))
- Color filters (on-chip): Ye, G, Cy vertical stripe filters
- Field integration system
- Electronic shutter function
- Anti-blooming function
- Chip size: 10.0 mm (H) x 8.2 mm (V)
- Unit Cell size: 11.0 µm (H) x 13.0 µm (V)
- Effective optical black
  Horizontal: Front 5pixels
  Back 45pixels
  Vertical: Front 16pixels
  Back 4pixels
- Dummy bits: horizontal 22-bits, vertical 1-bit (even fields only)

Package Outline Unit: mm



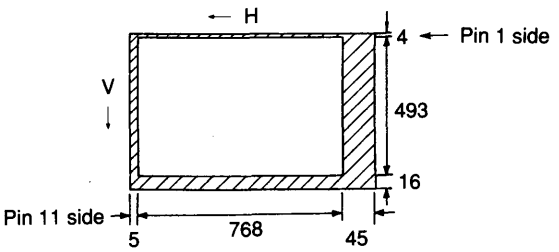
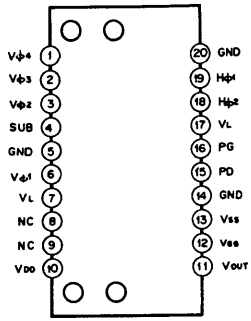


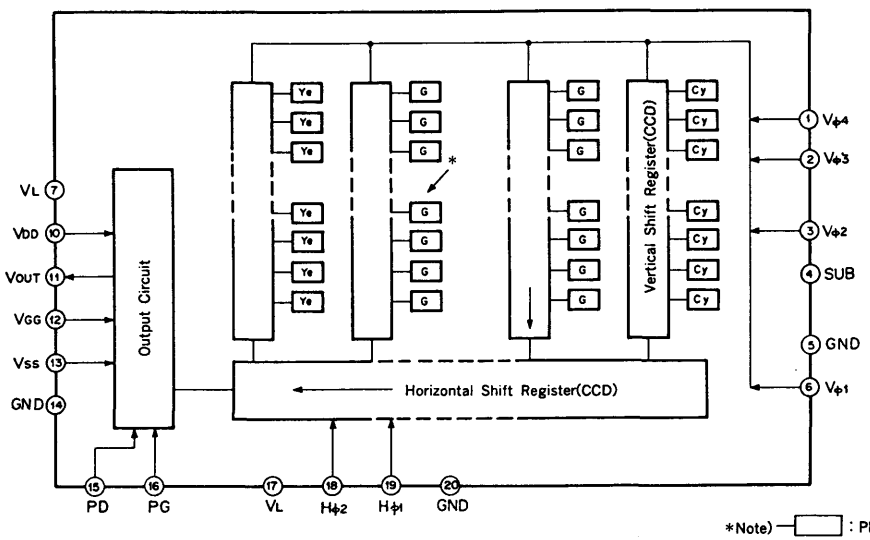
Fig. 1 Optical black configuration

Pin Configuration and Description (Top View)



No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate
3	Vφ2	Vertical register transfer clock	13	GSS	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	Vφ1	Vertical register transfer clock	16	PG	Output reset clock
7	VL	Protection transistor bias	17	VL	Protection transistor bias
8	NC		18	Hφ2	Horizontal register transfer clock
9	NC		19	Hφ1	Horizontal register transfer clock
10	VDD	Output amplifier drain supply	20	GND	GND

Imaging Device Function Block

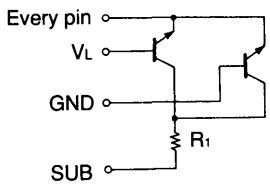


Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB-GND	-0.3 to +55	V	
V_{DD}, PD, V_{OUT}, V_{SS}-GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS}-SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - GND	-15 to +20	V	
Horizontal and vertical transfer clock inputs - SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	+15	V	Note 2
Potential difference between horizontal transfer clock inputs	+17	V	
$H\phi_1$, $H\phi_2$ - $V\phi_4$	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	
PG, V_{GG} - SUB	-55 to +10	V	Note 1
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L-V_L	-0.3 to +27	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This imaging device consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V.
The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5kΩ between Vss or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5 kΩ.

① V_{DD}, PD, V_{OUT} and Vss pins



② Pins other than ① (except V_L and GND)

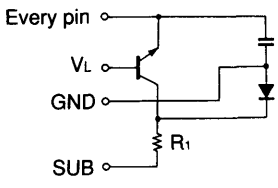


Fig. 2 Equivalent circuit

2. In case of clock width <10 μs and clock duty factor <0.1%, up to 27 V is guaranteed.

Bias Conditions

Item	Symbol	Min.	Typ.	Max	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5 %
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	-3		3	%	
Protection transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.

V_{SUB} code – Two digit indication

□ □
↑ ↑
Integral part Decimal part

The integral codes correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Actual values	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground Vss with a 390Ω resistance.
4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
   2) Current flowing to the ground when a voltage of 25 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 25 V to the SUB pin and ground pins other than those under test.
   3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
   4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.

Clock Voltage Conditions

Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.5		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-10.5			V	
Horizontal transfer clock voltage	V_{HHH}			5.2	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	

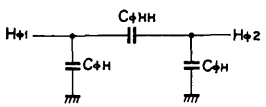
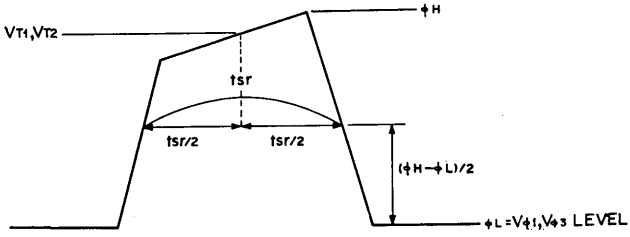


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_2$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".



2. Vertical clock voltage (Refer to Fig. 6)
T = 559 ns (with a horizontal driving frequency of 4 fsc)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).

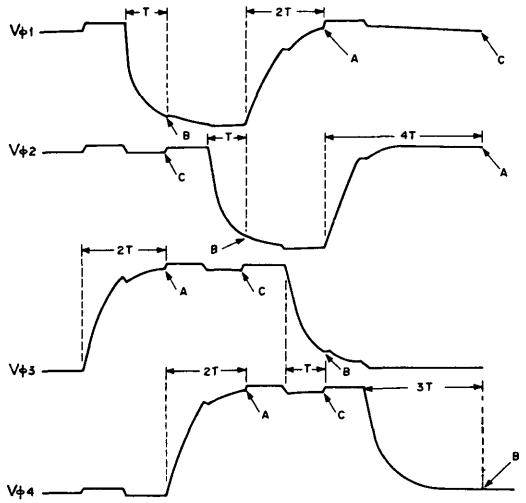


Fig. 6 Vertical transfer clock waveform
T = 559ns (with a horizontal driving frequency of 4 fsc)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".
   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
      And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

      The smaller of Δ21 and Δ12 is defined as the horizontal transfer clock amplitude "$V_{\phi H}$". The low level at that point is expressed as "V_{HL}".
   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

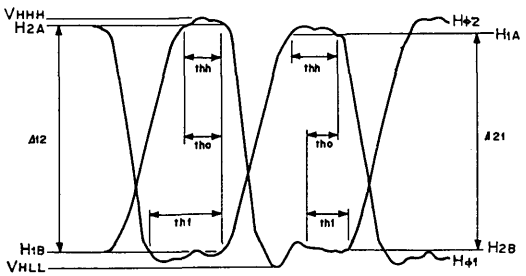


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

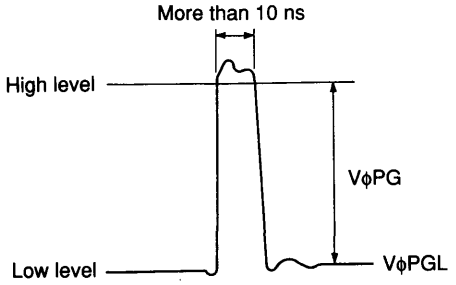


Fig. 8 Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as φL, and the substrate clock waveform maximum value as φH.
   2) The period where voltage level turns to (φH-φL)/2 is expressed as tsr. The difference between φL and voltage level at tsr/2 is defined as the substrate clock voltage VφSUB.

Driving Clock Waveform Conditions

1. Definition of ϕ_H (100%) and ϕ_L (0%)
   1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_2$) is applied.
   3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".
2. Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.32 MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
$H\phi_1$	18	33.7	10	8	ns	Imaging period
$H\phi_2$	18	33.7	10	8		
$H\phi_1$	4.9		0.01	0.01	µs	Parallel-serial converting period
$H\phi_2$		4.9	0.01	0.01		
ϕ_{PG}	12	53.7	2	2	ns	
$V\phi_1/V\phi_2$	61.6	1.6	0.1	0.1	µs	Imaging period
$V\phi_3/V\phi_4$	2.8	60.45	0.05	0.1		
$V\phi_T$	2.4		0.2	0.1		Reading period
$SUB\phi$	1.0		0.08	0.1	µs	Electron drained into substrate period

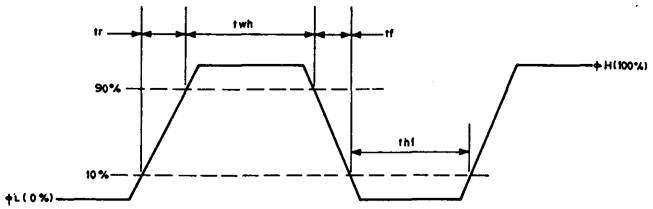


Fig. 9 Clock waveform

Imaging Characteristics

(See Fig. 10.)
Ta=25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	G	Sg	130	170		mV	1	
Sensitivity ratio	Ye	Ry	1.50	1.70	1.90		1	
	Cy	Rc	1.28	1.40	1.60		1	
Output saturation signal		Vsat	600			mV	2	Note
Blooming margin			1000			times	3	
Smear		Smr		0.007	0.015	%	4	Note
Video signal shading		Svg			25	%	5	
Uniformity in video signal channels		ΔSrg			10	%	6	
		ΔSdg			10	%	6	
Dark signal output		Vdt			2	mV	7	Ta=55°C
Dark signal shading		ΔVdt			1	mV	8	Ta=55°C
Flicker	Ye	Fy			5	%	9	
	G	Fg			5	%	9	
	Cy	Fc			5	%	9	

Note) Saturation signal and blooming margin are guaranteed only when the substrate voltage has been set to the voltage indicated on the back of the imaging device.

Test Methods

Conditions

(1) The conditions required to drive the device through the following tests are covered by the bias conditions and the clock voltage conditions. The test circuit shown in Fig. 11 is used for evaluating and testing the characteristics.

(2) Blemish are excluded from the following tests and the signal output is based on the optical black level unless otherwise specified test the value obtained at the output test point becomes the test value.

Definition of the standard imaging conditions

(1) Standard imaging condition I: Shoot the PTB-100 pattern box (luminance 706 Nit, Color temperature 3200°K) with no pattern, using a FUJINON H6 × 12.5D (F1.4) lens at F5.6. Use the CM-500S (1.0mmt) filter to cut off infrared rays.

(2) Standard imaging condition II: Shoot a light source (color temperature 3200°K) which provides a uniform brightness within 2% over the whole screen.
For infrared cut-off filter, use the CM-500S (1.0mmt)

1. Set to standard imaging condition I and test signal voltages (Sy, Sg, Sc) of Ye, G, Cy channels at the center of the screen.

   $Ry = Sy/Sg \qquad Rg=Sc/sg$

2. Set to standard imaging condition II and adjust the light intensity applied to Ye channel to about ten times the intensity obtained at a signal voltage of 200 mV. Then obtain the minimum value of the signal voltages at channels Ye, G and Cy respectively over the whole screen.

3. Set to standard imaging condition II and adjust the hight intensity applied to Ye channel to about 1000 times the intensity obtained at a signal voltage of 200 mV. Check that neither blooming is generated nor the vertical register saturated.

4. Set to standard imaging condition II and adjust the light intensity so that the signal voltage of G channel (V_{SG}) becomes 200 mV. Then, turn V_T off and obtain the maximum value of the signal voltage "V_{SM}" after stopping the horizontal resistor 50H at the effective pixels without depending Ye, G, Cy channels.

   $$Smr = \frac{V_{SM}}{V_{SG}} \times \frac{1}{50} \times \frac{1}{10} \times 100(\%)$$

   (Converted into 1/10V system)

5. Set to standard imaging condition II and test the signal voltage of G channel to obtain maximum (V_G max) and minimum (V_G min) values.
   The light intensity is adjusted so that the average value of the signal voltage (V_G average) becomes about 200 mV.

   $$Syg = \frac{V_G \text{ max} - V_G \text{ min}}{V_G \text{ average}} \times 100(\%)$$

6. Following test 5, test the signal voltage of each channel. Calculate the output gains of the red and blue signals (Ar and Ab) from the mean values of the signal voltages of Ye, G and Cy channels ($V_Y$mean, $V_G$mean, $V_C$mean). Then arrange the mean value of the red and bule signal voltage (VRmean and VBmean) so that they become equal to "VGmean". Then measure the differences between the G channel signal voltage (VG) and the R channel as well as B channel signal voltage (VR as well as VB) to obtain the maximum and minimum values.

$$Ar = \frac{VYmean - VGmean}{VGmean}$$

$$Ab = \frac{VCmean - VGmean}{VGmean}$$

$$VR = (VY - VG)/Ar \qquad VB = (VC - VG)/Ab$$

$$\Delta Srg = \frac{(VR-VG)max\ (VR-VG)min}{VGmean} \times 100(\%)$$

$$\Delta Sbg = \frac{(VB-VG)max - (VB-VG)min}{VGmean} \times 100(\%)$$

7. Measure the mean voltage of the dark current signal based on the horizontal free-transfer level in a light-shaded condition with an ambient temperature of 55°C.

8. Following measurement 7, test the dark current signal voltage to obtain the maximum (Vdmax) and minimum (Vdmin) values. Spot defects are ignored in this test.

$$\Delta Vdt = (Vdmax - Vdmin)$$

9. Set to standard imaging condition II and test the signal voltage difference "Vdr" between the fields of each channel. The light intensity is adjusted so that the average value of the G channel signal output (VG average) becomes about 200mV.
The average values of Ye and Cy channels are expressed as "VY average" and "VC average", respectively.

$$Fi = \frac{Vdri}{Vi\ average} \times 1000(\%) \qquad i = Y, G, C$$

Electrical Characteristics Test Circuit

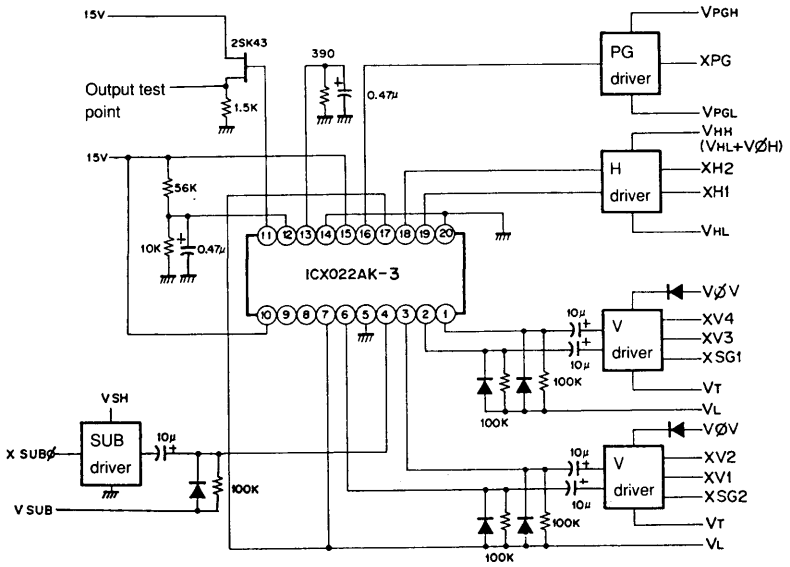
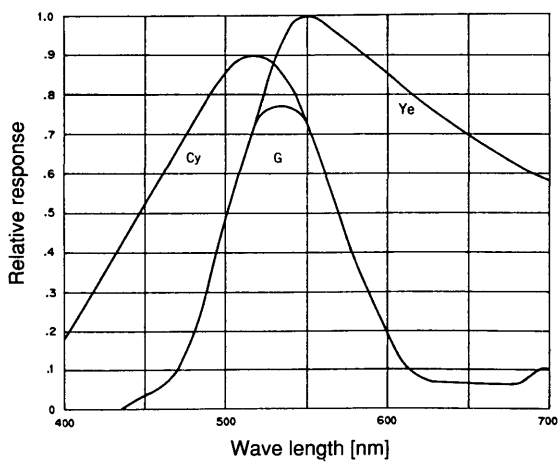
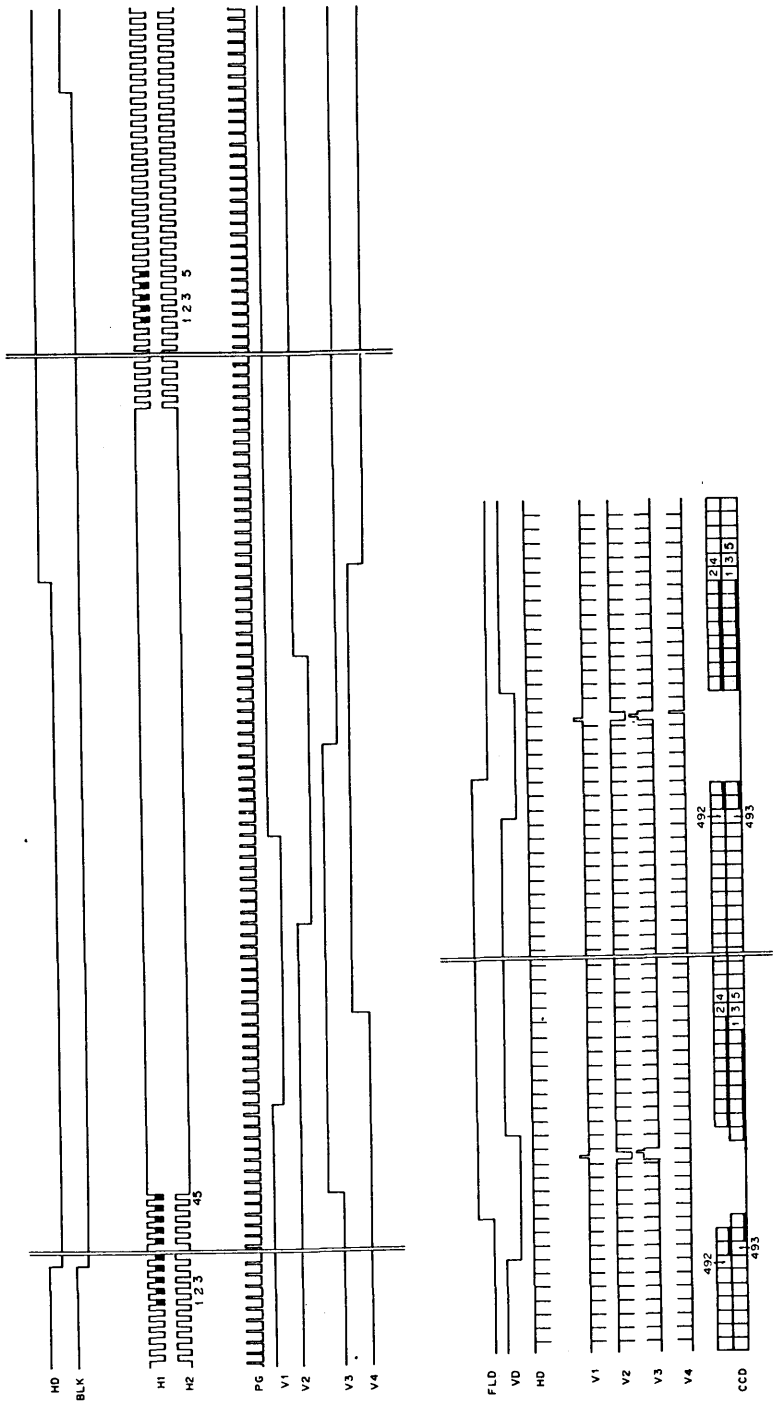


Fig.10

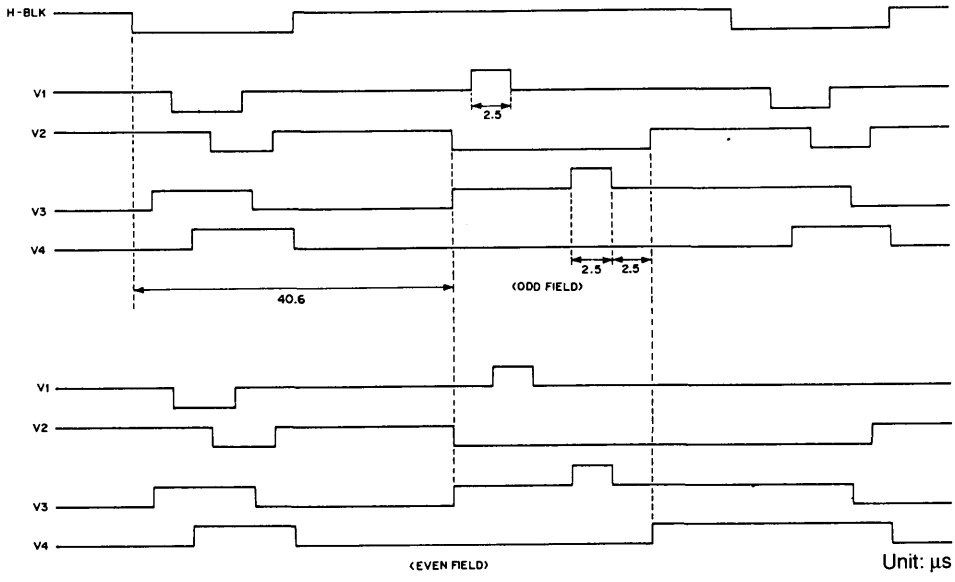
Spectrum Sensitivity Characteristics (Typical example, excluding illuminant characteristics)



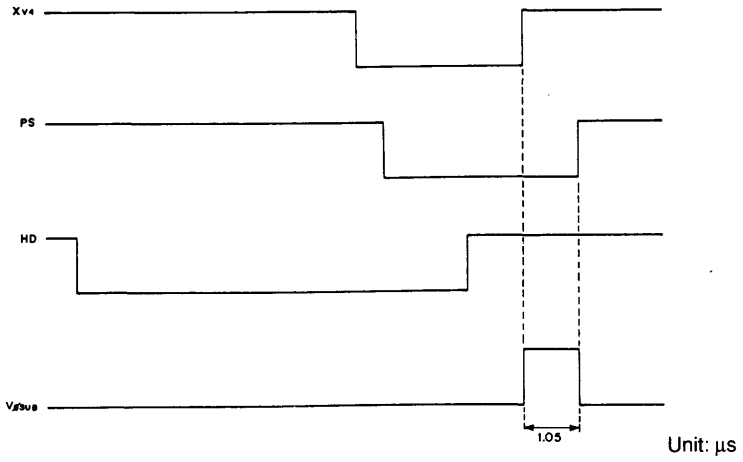
Driving Pulse Timing Chart (NTSC)



Sensor Read clock Timing Chart



Charge Drain Clock Timing Chart



Handling Instructions

1. On electric screening
   To prevent damage to the CCD image sensor by static electricity, handle as follows.
   a) Either handle the device with bare hands, or use antistatic gloves and clothes. Conductive shoes are also required.
   b) Use a ground lead when directly touching the device.
   c) Cover the floor and working table with a conductive mat or equivalent to avoid static electricity.
   d) Discharge using ionized air is recommended.
   e) To ship the mounted boards, use cartons with antistatic properties.

2. On soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder-dipping of DIP in a mounting furnace may break glass. Use a grounded 30 W soldering iron a each pin for less than 2 seconds. When adjusting or removing soldered parts, let the CCD cool sufficiently.
   c) Do not use any solder-aspirating equipment to remove the imaging device. Should an electric solder-aspiration device be used, use only a device of the zero-cross type control system and be sure to ground the controller.

3. On contamination
   a) Keep the operation room clean (Class 1000 will be expected).
   b) Do not touch the glass surface avoid contact with foreign objects. Blow off any dust the surface with a blower. (Ionized air is recommended to blow off any object sticking through static electricity.)
   c) Wipe off grass spots with an applicator moistened with ethanol. Be careful not to scratch the surface.
   d) To eliminate contamination, store the device in an exclusive case. During transportation minimize the difference in temperatures between locations to avoid moisture condensation.
   e) When a protection tape has been affixed for shipment, remove it just before use after applying appropriate antistatic measures. Do not reuse the removed tape.

4. Do not subject the device to light sources for extended periods. If a color element is subjected to strong light ray for an extended period, the color filter will be discolored. (Store the device in a dark place.)

5. Usage or storage of the device in high temperature or high humidity may seriously affect the performance.

6. The CCD image sensor is a high-precision optical part, that should not be subjected to mechanical shocks.

7. System data write complete ROM (address for Blemish compensation included)
   A number of System data write complete ROM equal to the number of ICX022AK-3's is attached. ROM's with blemish compensation address written bear a serial No. sticker. Use in pair with ICX022AK-3 bearing the same serial No.

Interline-type CCD Image Sensor

Description

ICX024AK-3 is an interline-type CCD image sensor designed for color video cameras.

Effective picture elements number 756 horizontally and 581 vertically.

Complementary color filters Ye, G and Cy are vertical stripe filters of high resolution and high sensitivity.

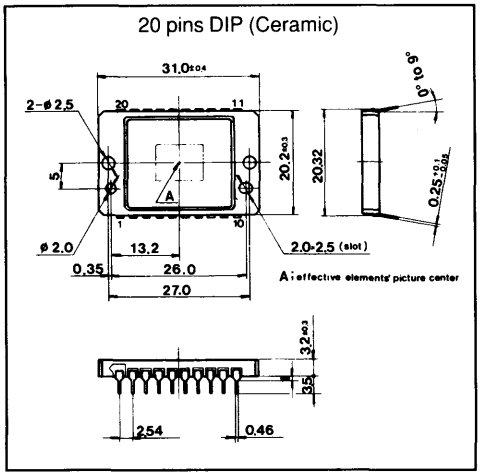
This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

Element Structure

- Interline type CCD image sensor
- Number of effective pixels: 756 (H) x 581 (V)
- 2/3 inch optical format (Effective sensing area: diagonal 10.49 mm)
- Color filters (on-chip): Ye,G,Cy vertical stripe filters
- Field integration read out system
- Electronic shutter function
- Anti-blooming function
- Chip size: 10.0 mm(H) x 8.2 mm(V)
- Unit Cell size: 11.0 mm(H) x 11.0 mm(V)
- Effective optical black
  - Horizontal: Front 5 pixels
    Back 55 pixels
  - Vertical: Front 19 pixels
    Back 6 pixels
- Dummy bits: horizontal 22-bits, vertical 1-bit (even fields only)

Package Outline

Unit: mm



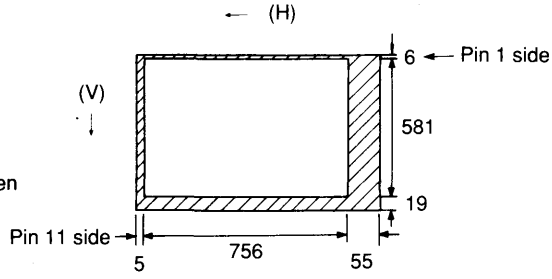
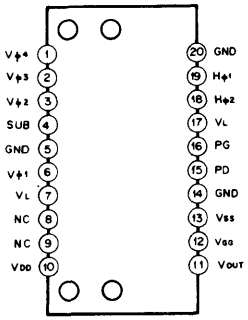


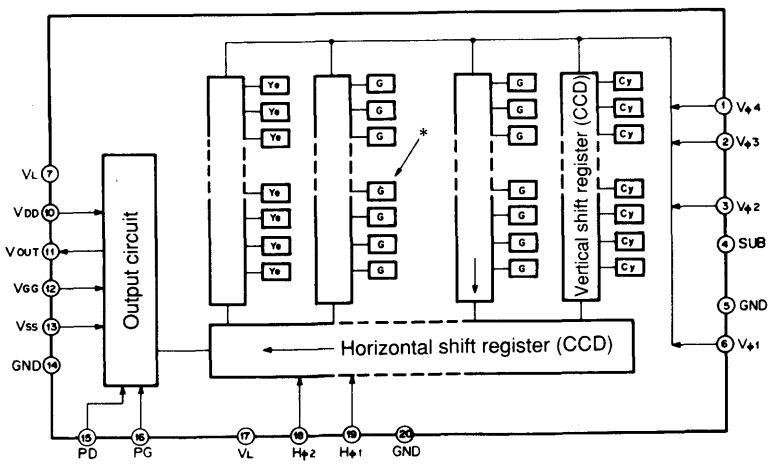
Fig. 1 Optical black configuration

Pin Configuration and Description
(Top View)



No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	V_{OUT}	Signal output
2	Vφ3	Vertical register transfer clock	12	V_{GG}	Output amplifier gate
3	Vφ2	Vertical register transfer clock	13	V_{SS}	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	Vφ1	Vertical register transfer clock	16	PG	Output reset clock
7	V_L	Protective transistor bias	17	V_L	Protective transistor bias
8	NC		18	Hφ2	Horizontal register transfer clock
9	NC		19	Hφ1	Horizontal register transfer clock
10	V_{DD}	Supply voltage	20	GND	GND

Imaging Device Function Block



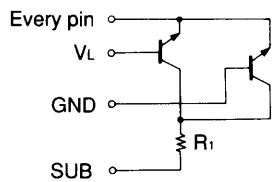
*Note) : Photo sensor

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB - GND	−0.3 to +55	V	
V_{DD}, PD, V_{OUT}, V_{SS} - GND	−0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS} - SUB	−55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - GND	−15 to +20	V	
Horizontal and vertical transfer clock inputs - SUB	−65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	15	V	Note 2
Potential difference between horizontal transfer clock inputs	17	V	
$H\phi_1$, $H\phi_2$ - $V\phi_4$	−17 to +17	V	
PG, V_{GG} - GND	−10 to +15	V	
PG, V_{GG} - SUB	−55 to +10	V	Note 1
V_L - SUB	−65 to +0.3	V	
Pins other than GND, SUB and V_L - V_L	−0.3 to +27	V	
Storage temperature	−30 to +80	°C	
Operation guarantee ambient temperature	−10 to +55	°C	

Note) 1. This imaging device consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V. The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5 kΩ between V_{SS} or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5 Ω.

1) V_{DD}, PD, V_{OUT} and V_{SS} pins



2) Pins other than 1) (except V_L and GND)

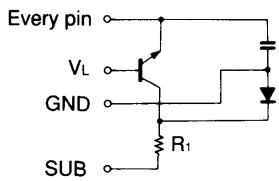


Fig. 2 Equivalent circuit

2. In case of clock width <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Electrical Characteristics

Bias conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5%
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	-3		3	%	
Protection transistor bias	V_L	To be the vertical transfer clock low-level clamp bias				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.
V_{SUB} code - Two digit indication

□ □
↑ ↑
Integral part Decimal part

The integral code correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Numerical value	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground V_{SS} with a 390 Ω resistance

4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
2) Current flowing to the ground when a voltage of 20 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 20 V to the SUB pins and ground pins other than those under test.
3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.

5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.

Clock Voltage Conditions

Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0	5.0	15.0	V	Note 1
Vertical transfer clock voltage	V_{VMM}			1.3	V	Note 2
	V_{VM}	-0.5		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-10.5			V	
Horizontal transfer clock voltage	V_{MMH}			5.2	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	

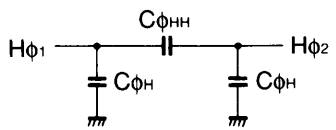


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_2$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes (ϕ_H – ϕ_L)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at Vo1) and "V_{T3}" (at Vo3). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

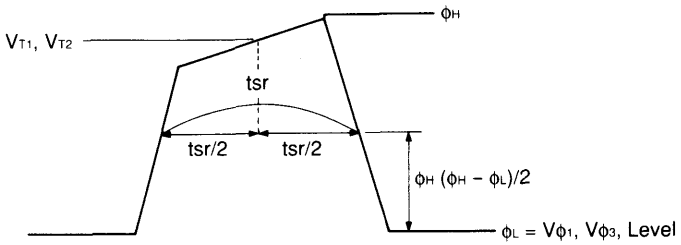


Fig. 5 Read clock waveform

2. Vertical clock voltage (Refer to Fig. 6)

T = 564 ns (with a horizontal driving frequency of 14.19MHz)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ Level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ Level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ Level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum from these values is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}".
"V_{VHH}" expresses the maximum level except in the period where read clock Vr is protruding (in $V\phi_1$ and $V\phi_3$ only).

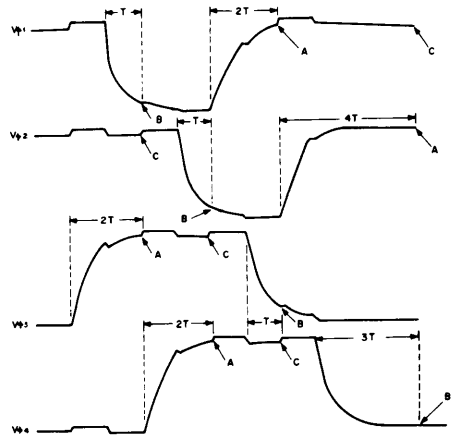


Fig. 6 Vertical transfer clock waveform
T = 564ns (with a horizontal driving frequency of 14.1875MHz)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clock s "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".

   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
   And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

      The smaller of Δ21 and Δ12 is defined as the horizontal transfer clock amplitude "$V\phi_H$". The low level at that point is expressed as "V_{HL}".

   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

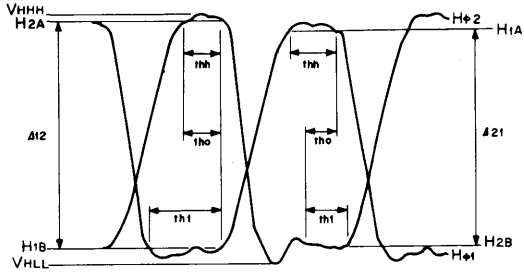


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

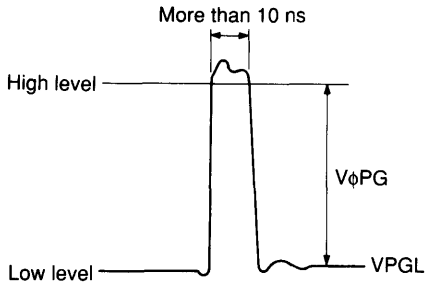


Fig. 8 Waveform of PG clock

5. Basic clock voltage
   1) Basic voltage is expressed as ϕ_L and the maximum value of the basic clock waveform as ϕ_H.
   2) The period during which voltage level reaches (ϕ_H – ϕ_L) is expressed as tsr. The difference of voltage level with φL at tsr/2 is defined as basic clock voltage Vφ SUB.

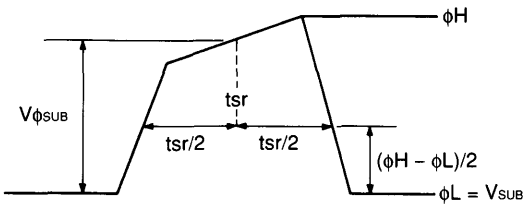


Fig. 9 Basic clock waveform

Driving Clock Waveform Conditions

1) Definition of ϕ_H (100%) and ϕ_L (0%)
   (1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock (PGφ) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   (2) For the read clock (Vr), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (Vr) of the vertical transfer clocks ($V\phi_1$, $V\phi_2$) is protruding.
   (3) For the substrate clock (SUBφ), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".

2) Standard driving clock conditions (Typ.)
Horizontal drive frequency: 14.1875MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
Hφ1	18	33.7	10	8	ns	Imaging period
Hφ2	18	33.7	10	8		
Hφ1	4.9		0.01	0.01	µs	Parallel-serial converting period
Hφ2		4.9	0.01	0.01		
φPG	12	53.7	2	2	ns	
Vφ1/Vφ2	61.6	1.6	0.1	0.1	µs	Imaging period Reading period
Vφ3/Vφ4	2.8	60.45	0.05	0.1		
VφT	2.4		0.2	0.1		Reading period
SUBφ	1.0		0.08	0.1	µs	Electron sweep-off period

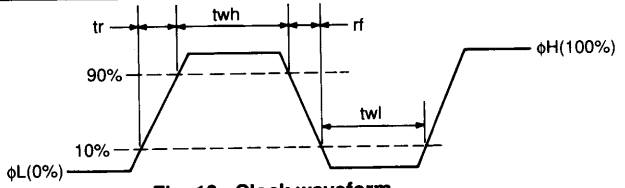


Fig. 10 Clock waveform

Imaging Characteristics

(For the testing circuit, see Fig. 10.)
Ta=25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	G	Sg	120	160		mV	1	
Sensitivity ratio	Ye	Ry	1.50	1.70	1.90		1	
	Cy	Rc	1.28	1.40	1.60		1	
Output saturation signal		Vsat	500			mV	2	Note
Blooming margin			800			times	3	Note
Smear		Smr		0.07	0.015		4	
Video signal shading		Svg			25	%	5	
Uniformity in video signal channels		ΔSrg			10	%	6	
		ΔSbg			10	%	6	
Dark signal output		Vdt			2	mV	7	Ta=55°C
Dark signal shading		ΔVdt			1	mV	8	Ta=55°C
Flicker	Ye	Fy			5	%	9	
	G	Fg			5	%	9	
	Gy	Fc			5	%	9	

Note) Saturation signal and blooming margin are guaranteed only when the substrate voltage has been set to the voltage indicated on the back of the imaging device.

Test Methods

Conditions

1) The conditions required to drive the device through the following tests are covered by the bias conditions and the clock voltage conditions. The test circuit shown in Fig. 11 is used for evaluating and testing the characteristics.
2) Flaws are excluded from the following tests and the signal output is based on the optical back level unless otherwise specified. The value obtained at the output test point becomes the test value.

Standard imaging conditions

1) Shoot the PTB-100 pattern box (luminance 706 Nit, color temperature 3200°K) with no pattern, using a FUJINON H6 × 12.5D (F1.4) lens at F5.6. Use the CM-500S (1.0 mmt) filter to cut off infrared rays.
2) Shoot a light source (color temperature 3200°K) which provides a uniform brightness within 2% over the whole screen.
   For infrared cut-off filter, use the CM-500S (1.0 mmt).

1. Set to standard imaging condition 1) and test signal voltages (Sy, Sg, Sc) of Ye, G, Cy channels at the center of the screen.
   Ry = Sy / Sg
   Rc = Sc / Sg

2. Set to standard imaging condition 2) and adjust the light intensity applied to Ye channel to about eight times the intensity obtained at a signal voltage of 200 mV. Then obtain the minimum value of the signal voltage at channels Ye, G and Cy respectively over the whole screen.

3. Set to imaging condition 2) and adjust the light intensity applied to channel Ye to about 800 times the intensity obtained at a signal voltage of 200 mV. At that time make sure there is no blooming and the vertical resistor is not saturated.

4. Set to standard imaging condition 2) and adjust the light intensity so that the signal voltage of G channel (V_{SG}) becomes 200 mV. Then, turn Vr off and obtain the maximum value of the signal voltage "V_{SM}" after stopping the horizontal resistor 50 H at the effective picture element without depending Ye, G, Cy channels.

$$Smr = \frac{V_{SM}}{V_{SY}} \times \frac{1}{50} \times \frac{1}{10} \times 100\ (\%)$$

   (Converted into 1/10 V system)

5. Set to standard imaging condition 2) and test the signal voltage of G channel to obtain maximum (V_G max) and minimum (V_G min) values.
   The light intensity is adjusted so that the average value of the signal voltage (V_G average) becomes about 200 mV.

$$Syg = \frac{V_G max - V_G min}{V_G average} \times 100\ (\%)$$

6. Following test 5, test the signal voltage of each channel. Calculate the output gains of the red and blue signals (Ar and Ab) from the mean values of the signal voltages of Ye, G and Cy channels (VYmean, VGmean, VCmean). Then arrange the mean value of the red and blue signal voltage (VRmean and VBmean) so that they become equal to "VGmean". Then measure the differences between the G channel signal voltage (VG) and the R channel as well as B channel signal voltage (VR as well as VB) to obtain the maximum and minimum values.

$$Ar = \frac{VYmean - VGmean}{VGmean}$$

$$Ab = \frac{VCmean - VGmean}{VGmean}$$

$$VR = (VY - VG)/Ar \qquad VB = (VC - VG)/Ab$$

$$\Delta Srg = \frac{(VR - VG)max - (VR - VG)min}{VGmean} \times 100(\%)$$

$$\Delta Sbg = \frac{(VB - VG)max - (VB - VG)min}{VGmean} \times 100(\%)$$

7. Measure the mean voltage of the dark current signal based on the horizontal free-transfer level in light-shaded condition with an ambient temperature of 55°C.

8. Following measurement 7, test the dark current signal voltage to obtain the maximum (V dmax) and minimum (V dmin) values. Spot defects are ignored in this test.

$$\Delta Vdt = (Vdmax - Vdmin)$$

9. Set to standard imaging condition 2) and test the signal voltage difference "Vdr" between the fields of each channel. The light intensity is adjusted so that the average value of the G channel signal output (VG average) becomes about 200 mV.
The average values of Ye and Cy channels are expressed as "VY average" and "VC average", respectively.

$$Fi = \frac{Vdri}{Vi\ average} \times 100\ (\%)$$

$$i = Y, G, C$$

Electrical Characteristics Test Circuit

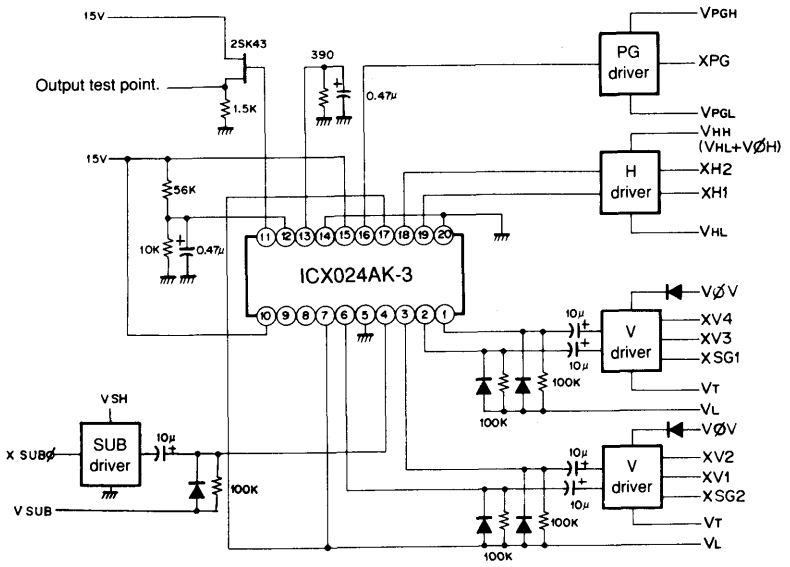
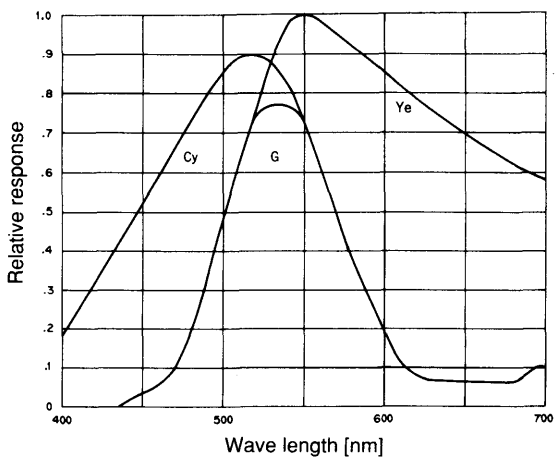
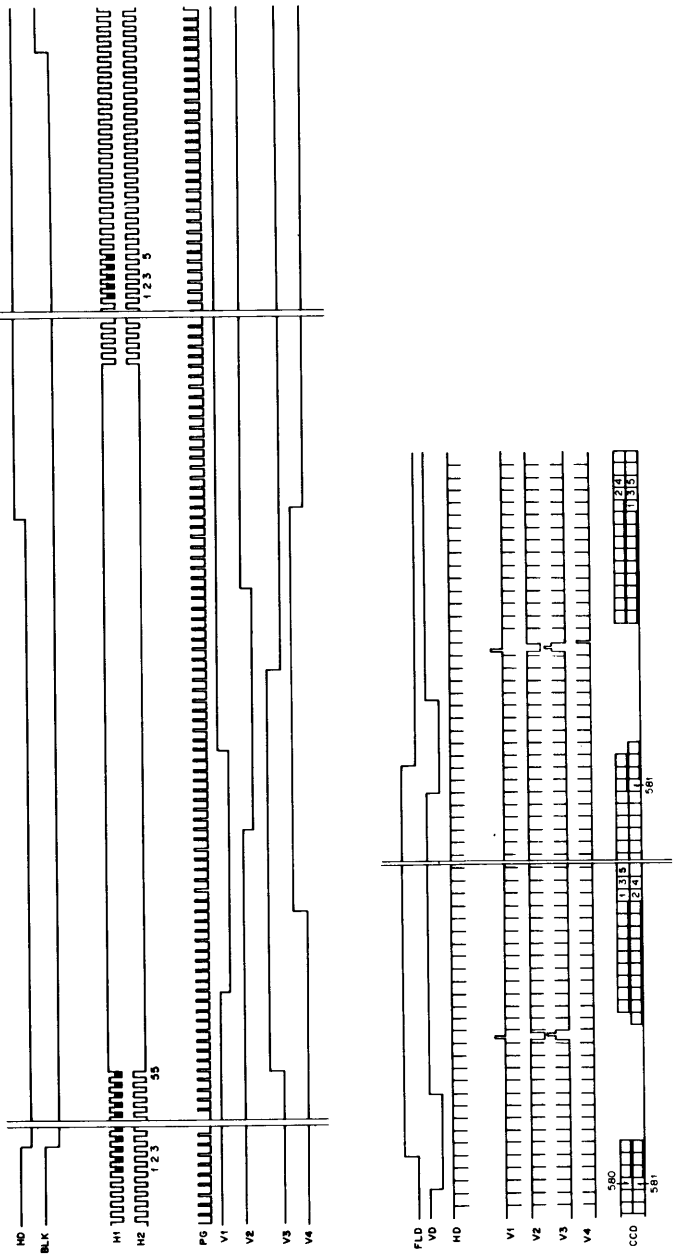


Fig. 11

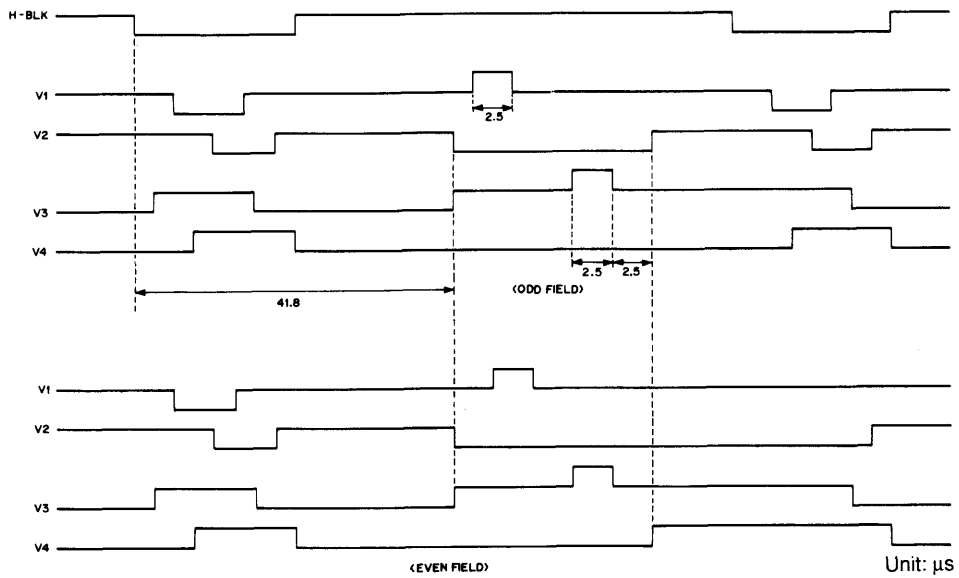
Spectrum Sensitivity Characteristics (Typical example, excluding illuminant characteristics)



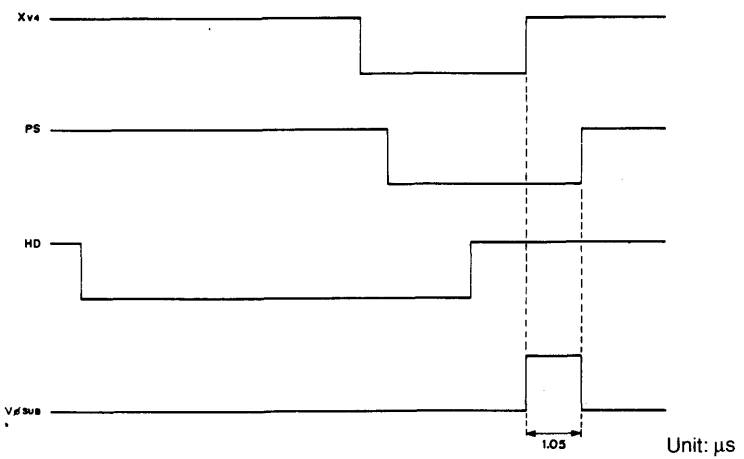
Driving Pulse Timing Chart (CCIR)



Sensor Read clock Timing Chart



Charge Drain Clock Timing Chart



Handling Instructions

1. On electric screening
   To prevent damage to the CCD image sensor by static electricity, handle as follows.
   a) Either handle the device with bare hands, or use antistatic gloves and clothes. Conductive shoes are also required.
   b) Use a ground lead when directly touching the device.
   c) Cover the floor and working table with a conductive mat or equivalent to avoid static electricity.
   d) Discharge using ionized air is recommended.
   e) To ship the mounted boards, use cartons with antistatic properties.

2. On soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder-dipping in a mounting furnace may break glass. Use a grounded 30 W soldering iron a each pin for less than 2 seconds. When adjusting or removing soldered parts, let the CCD cool sufficiently.
   c) Do not use any solder-aspirating equipment to remove the imaging device. Should an electric solder-aspiration device be used, use only a device of the zero-cross type control system and be sure to ground the controller.

3. On contamination
   a) Keep the operation room clean (Class 1000 will be expected).
   b) Do not touch the glass surface avoid contact with foreign objects. Blow off any dust the surface with a blower. (Ionized air is recommended to blow off any object sticking through static electricity.)
   c) Wipe off grass spots with an applicator moistened with ethanol. Be careful not to scratch the surface.
   d) To eliminate contamination, store the device in an exclusive case. During transportation minimize the difference in temperatures between locations to avoid moisture condensation.
   e) When a protection tape has been affixed for shipment, remove it just before use after applying appropriate antistatic measures. Do no reuse the removed tape.

4. Do not subject the device to light sources for extended periods. If a color element is subjected to strong light ray for an extended period, the color filter will be discolored. (Store the device in a dark place.)

5. Usage or storage of the device in high temperature or high humidity may seriously affect the performance.

6. The CCD image sensor is a high-precision optical part, that should not be subjected to mechanical shocks.

7. System data write complete ROM (with flow compensation address included)
   System data write complete ROM in equal quantity as ICX024AK-3 is attached.
   Analog those ROM with address for flow compensation have serial No. stuck on.
   Use in conjunction with ICX024AK-3 pairing the same serial No..

CCD Imaging Blocks for Color Camera

Description

IU022AK-30A/40A and IU024AK-30A/40A are solid state imaging blocks developed for color video cameras. They incorporate an image correction optical filter (Optical crystal low pass filter, infrared cut filter) indispensable for solid state imaging devices.
These blocks can easily be attached to the rear of a lens or the mount of an interchangeable lens to provide a lightweight, compact imaging system.

Pin Configuration (Top View)

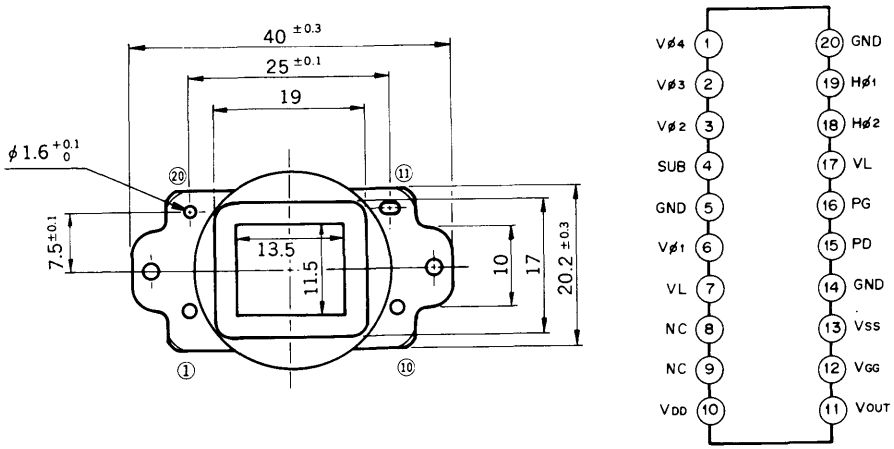


Fig. 1

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V_{\phi 4}$	Vertical register transfer clock input	11	V_{OUT}	Signal output
2	$V_{\phi 3}$	Vertical register transfer clock input	12	V_{GG}	Output amplifier gate bias
3	$V_{\phi 2}$	Vertical register transfer clock input	13	V_{SS}	Output amplifier source bias
4	SUB	Substrate	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	$V_{\phi 1}$	Vertical register transfer clock input	16	PG	Output reset clock input
7	VL	Protected transistor bias	17	VL	Protected transistor bias
8	NC	Non connection	18	$H_{\phi 2}$	Horizontal register transfer clock input
9	NC	Non connection	19	$H_{\phi 1}$	Horizontal register transfer clock input
10	V_{DD}	Supply voltage	20	GND	GND

80830-HP

Package Outline (Unit : mm)

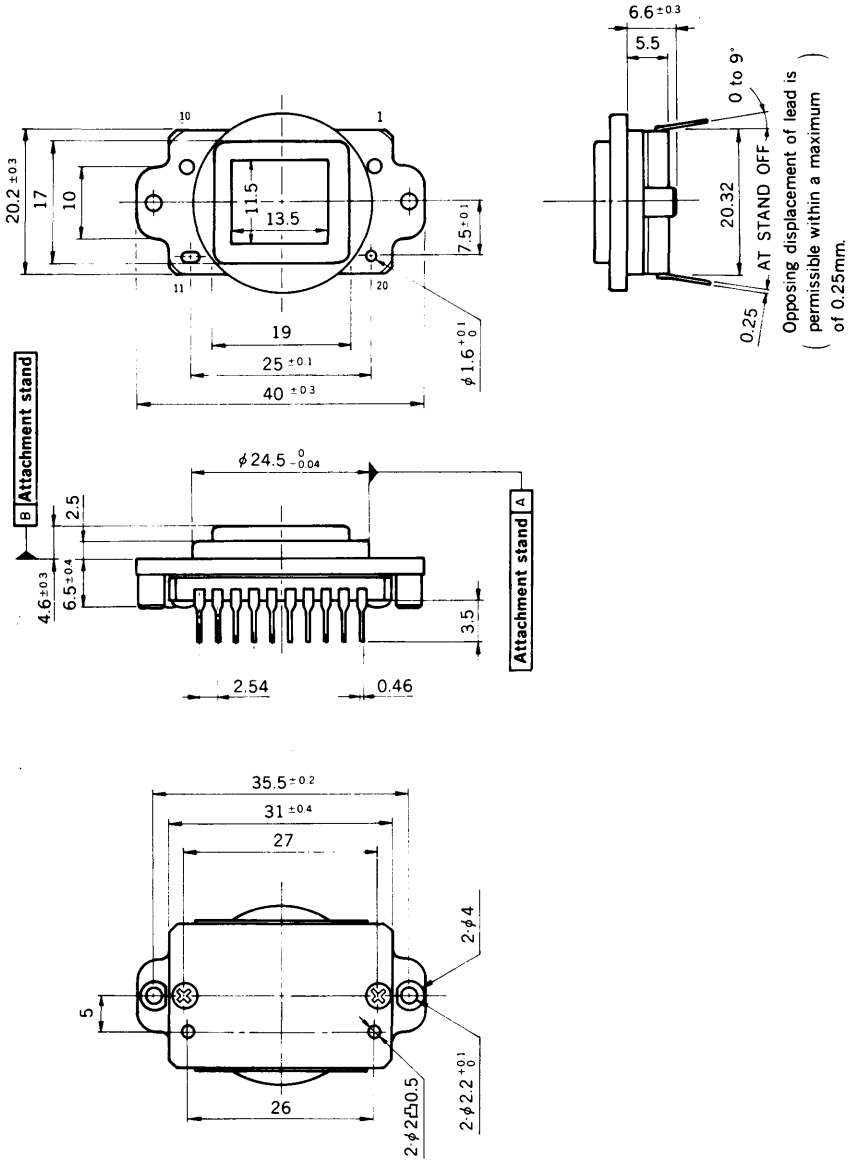


Fig. 2

Configuration and Optical Characteristics

Item	Ratings	Unit	Remark
Appearance, size, attachment.	See the Package Outline (Fig. 2)		
Optical axis	Within the ϕ11.1 circle with the Ref. A center are the effective elements.	mm	Fig. 2 Standard location A
Image rotation	Within ±1	deg	ϕ1.6 spot
Back focus	1.74±0.3	mm	(In AIR) Fig. 2 Standard surface B
Tilt	60	μm	Fig. 2 Standard surface B
Optical thickness	6.6	mm	BK-7 equivalent (including optical filter assembly and optical parts of CCD)
Optical filter	Four-layer laminated type		
Spectral sensitivity characteristics	See Fig. 3		
Weight	14	g	

Note) See the specifications of ICX022AK-3/4 and ICX024K-3/4 for imaging characteristics, electrical characteristics and absolute maximum ratings.

Spectral sensitivity characteristics example

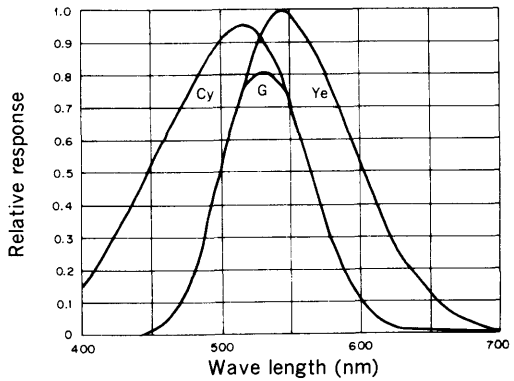


Fig. 3

Environmental Characteristics

Item	Condition	Requirements
Vibration	7G, 10 to 30Hz, 300sec sweep, each 15min for x, y, z directions	The above structure satisfies optical characteristics.
Impact	80G, in 6directions	
Low temperature durability	−30°C, 240 hours	
High temperature durability	80°C, 240 hours	
Heat cycle	−30°C to 25°C to 80°C 30min to 5min to 30min 10cycles	
High temperature and high humidity durability	60°C, 95%, 240hours	

Interline-type CCD Solid Image Sensor

Description

ICX022AN-3 is an interline-type CCD solid imaging device designed for color video cameras. Effective pixels number 768 horizontally and 493 vertically.

HAD (Hole Accumulated Diode) sensors are employed as photosensor elements to ensure much reduced dark current.

Color filters incorporated Ye, G, Mg and Cy are mosaic filters of high resolution and high sensitivity.

The device employs the field integration system to obtain a high resolution.

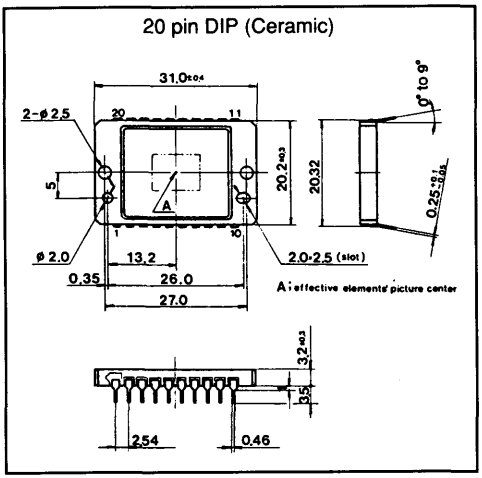
Electric charges are swept out of the substrate, so the sensor has electronic shutter capability with variable charge storage time.

Features

- Image size: 2/3 inches (8.8 mmH × 6.6 mmV)
- Effective pixels: 768H × 493V
- Effective optical black
  Horizontal: Front 5 pixels
  Back 45 pixels
  Vertical: Front 16 pixels
  Back 4 pixels
- High resolution
- High sensitivity
- Low noise
- Low smear
- Low dark current
- Electronic shutter
- Low antiblooming
- No graphic distortion, no microphonic noise
- γ characteristics: 1

Package Outline

Unit: mm



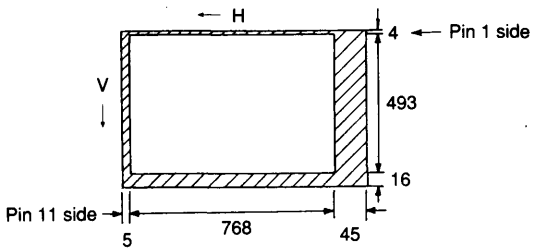


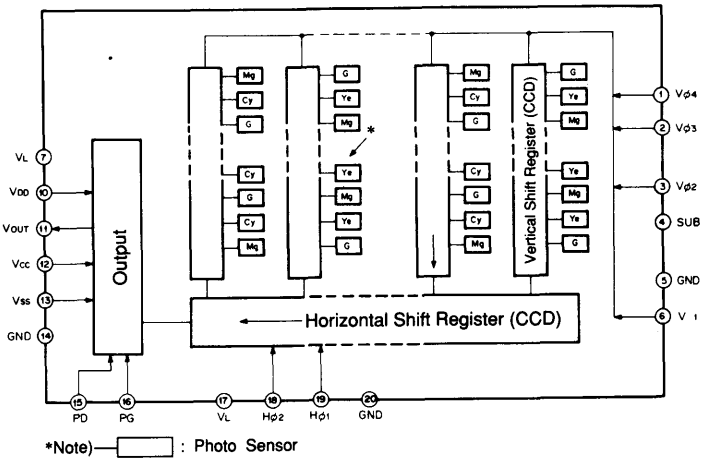
Fig. 1 Optical black configuration

Device Structure

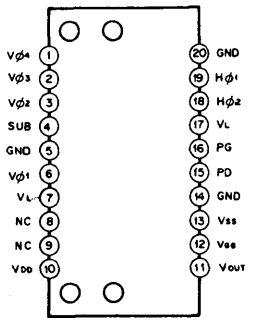
- Interline type CCD image sensor
- Chip size: 10.0 mmH × 8.2 mmV
- Unit cell size: 11.0 μm (H) × 13.0 μm (V)
- Dummy bits: Horizontal 22-bits, vertical 1-bit (Even fields only)
- HAD (Hole Accumulated Diode) sensor
- High sensitivity output amplifier
- Ye, Cy, Mg, G on chip type complementary color mosaic filter
- N type substrate P-well structure

E88Z38-YA

Imaging Device Function Block



Pin Configuration and Description (Top View)



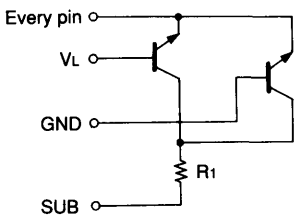
No.	Symbol	Description	No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	11	V_{OUT}	Signal output
2	$V\phi_3$	Vertical register transfer clock	12	V_{GG}	Output amplifier gate
3	$V\phi_2$	Vertical register transfer clock	13	V_{SS}	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	$V\phi_1$	Vertical register transfer clock	16	PG	Output reset clock
7	V_L	Protection transistor bias	17	V_L	Protection transistor bias
8	NC		18	$H\phi_2$	Horizontal register transfer clock
9	NC		19	$H\phi_1$	Horizontal register transfer clock
10	V_{DD}	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB-GND	-0.3 to +55	V	
V_{DD}, PD, V_{OUT}, V_{SS}-GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS}-SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - GND	-15 to +20	V	
Horizontal and vertical transfer clock inputs - SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	+15	V	Note 2
Potential difference between horizontal transfer clock inputs	+17	V	
$H\phi_1$, $H\phi_2$ - $V\phi_4$	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	
PG, V_{GG} - SUB	-55 to +10	V	Note 1
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L-V_L	-0.3 to +28	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This imaging device consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V.
The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5kΩ between Vss or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5 kΩ.

① V_{DD}, PD, V_{OUT} and Vss pins



② Pins other than ① (except V_L and GND)

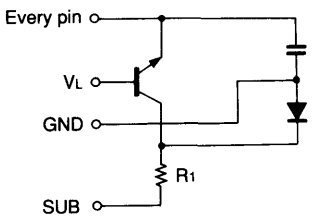


Fig. 2 Equivalent circuit

2. In case of clock width <10 μs and clock duty factor <0.1%, up to 27 V is guaranteed.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5 %
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	-3		3	%	
Protection transistor bias	V_L	-12	-11	Note 6	V	

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.

V_{SUB} code – Two digit indication

The integral codes correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Actual values	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground Vss with a 390Ω resistance.
4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
   2) Current flowing to the ground when a voltage of 25 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 25 V to the SUB pin and ground pins other than those under test.
   3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
   4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.
6. Vertical transfer clock low level clamp bias

Clock Voltage Conditions
Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.3		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-11.0			V	
Horizontal transfer clock voltage	V_{HHH}			5.5	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	

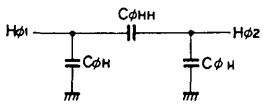


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_2$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

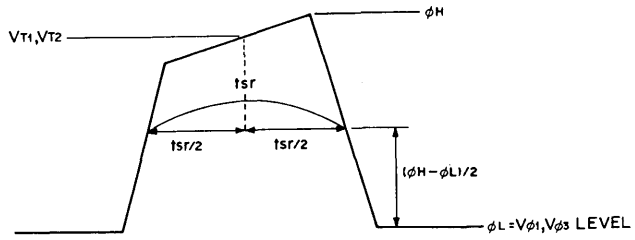


Fig. 5 Read clock waveform

2. Vertical clock voltage (Refer to Fig. 6)
T = 559 ns (with a horizontal driving frequency of 14.32 MHz)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).

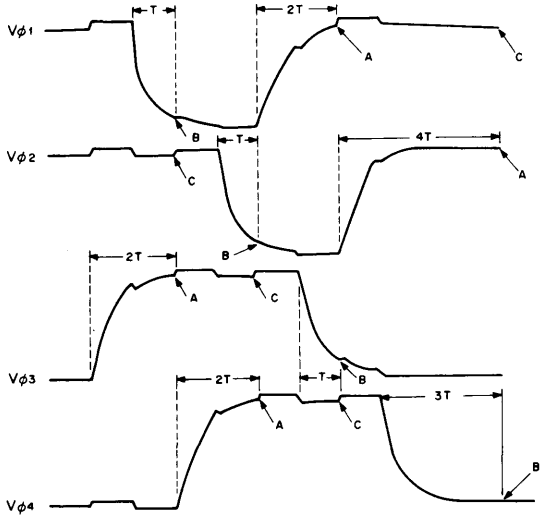


Fig. 6 Vertical transfer clock waveform
T = 559ns (with a horizontal driving frequency of 4 fsc)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".
   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
   And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

      The smaller of Δ21 and Δ12 is defined as the horizontal transfer clock amplitude "$V\phi_H$". The low level at that point is expressed as "V_{HL}".
   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

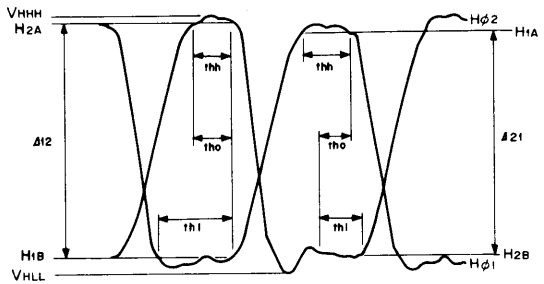


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

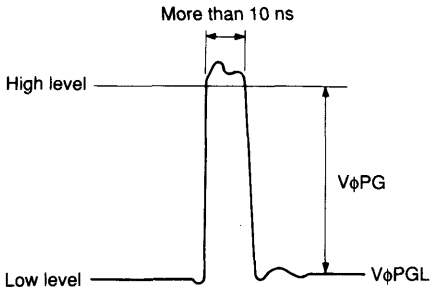


Fig. 8 Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as φL, and the substrate clock waveform maximum value as φH.
   2) The period where voltage level turns to (φH-φL)/2 is expressed as tsr. The difference between φL and voltage level at tsr/2 is defined as the substrate clock voltage VφSUB.

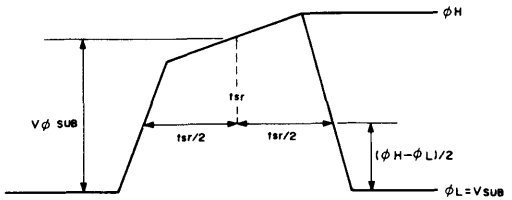


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1. Definition of ϕ_H (100%) and ϕ_L (0%)
   1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock ($PG\phi$) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_2$) is applied.
   3) For the substrate clock ($SUB\phi$), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".

2. Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.32 MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
Hφ1	18	33.7	10	8	ns	Imaging period
Hφ2	18	33.7	10	8		
Hφ1	4.9		0.01	0.01	µs	Parallel-serial converting period
Hφ2		4.9	0.01	0.01		
φPG	12	53.7	2	2	ns	
Vφ1/Vφ2	61.6	1.6	0.1	0.1	µs	Imaging period
Vφ3/Vφ4	2.8	60.45	0.05	0.1		
VφT	2.4		0.2	0.1		Reading period
SUBφ	1.0		0.08	0.1	µs	Electron drained into substrate period

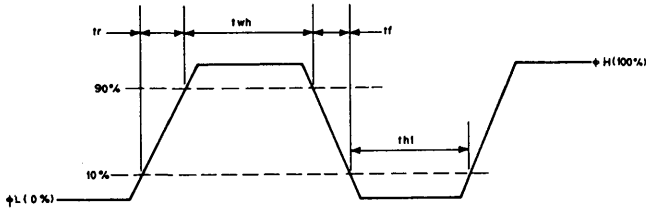
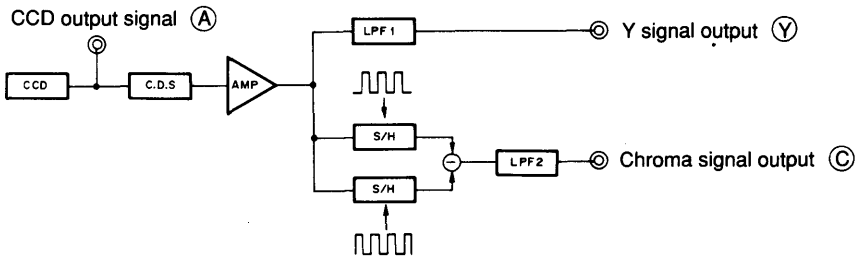


Fig. 10 Clock waveform

Imaging Characteristics (See Fig. 10.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sy	150	200		mV	1	
Output saturation signal	Ysat	600			mV	2	Ta=55°C
Smear	SM		0.007	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone ϕ, I
				25	%	5	Zone ϕ to II
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
R-Y	Fcr			5	%	9	
B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			3.0	%	10	
G	Lcg			3.0	%	10	
B	Lcb			3.0	%	10	
W	Lcw			3.0	%	10	
Lag	ΔYlag			0.5	%	11	

Test Circuit



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

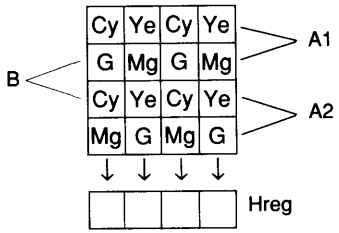
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through Horizontal register (H reg.) at line A1 are



Color Coding Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200°K Halogen source), at F5.6 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200°K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=200mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=200mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=200mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200mA. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = | (Crmax - Crmin)/Y_A | \times 100\ (\%)$$
$$\Delta Sb = | (Cbmax - Cbmin)/Y_A | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Ydmax.) and Min. (Ydmin.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$$Fy = (\Delta Yf/Y_A) \times 100\ (\%)$$

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

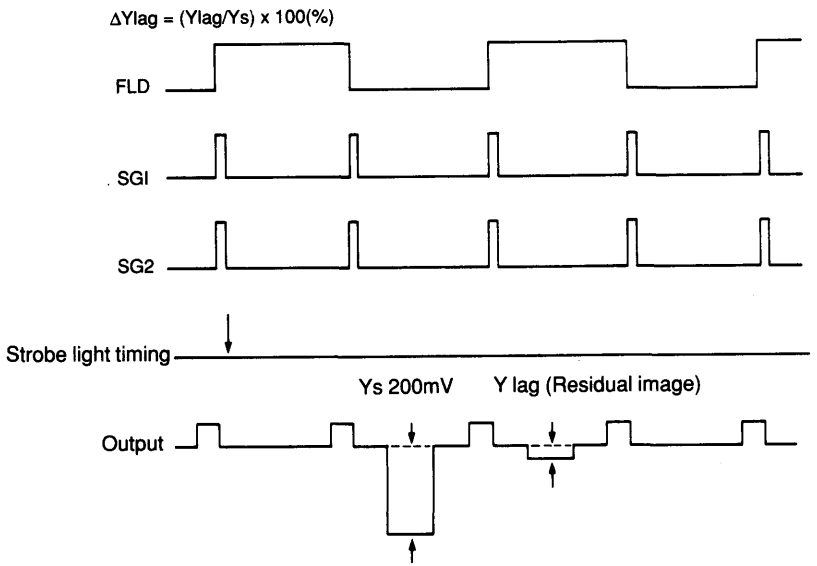
$$Fci = (\Delta Ci/C_{Ai}) \times 100\ (\%) \quad (i = r, b)$$

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

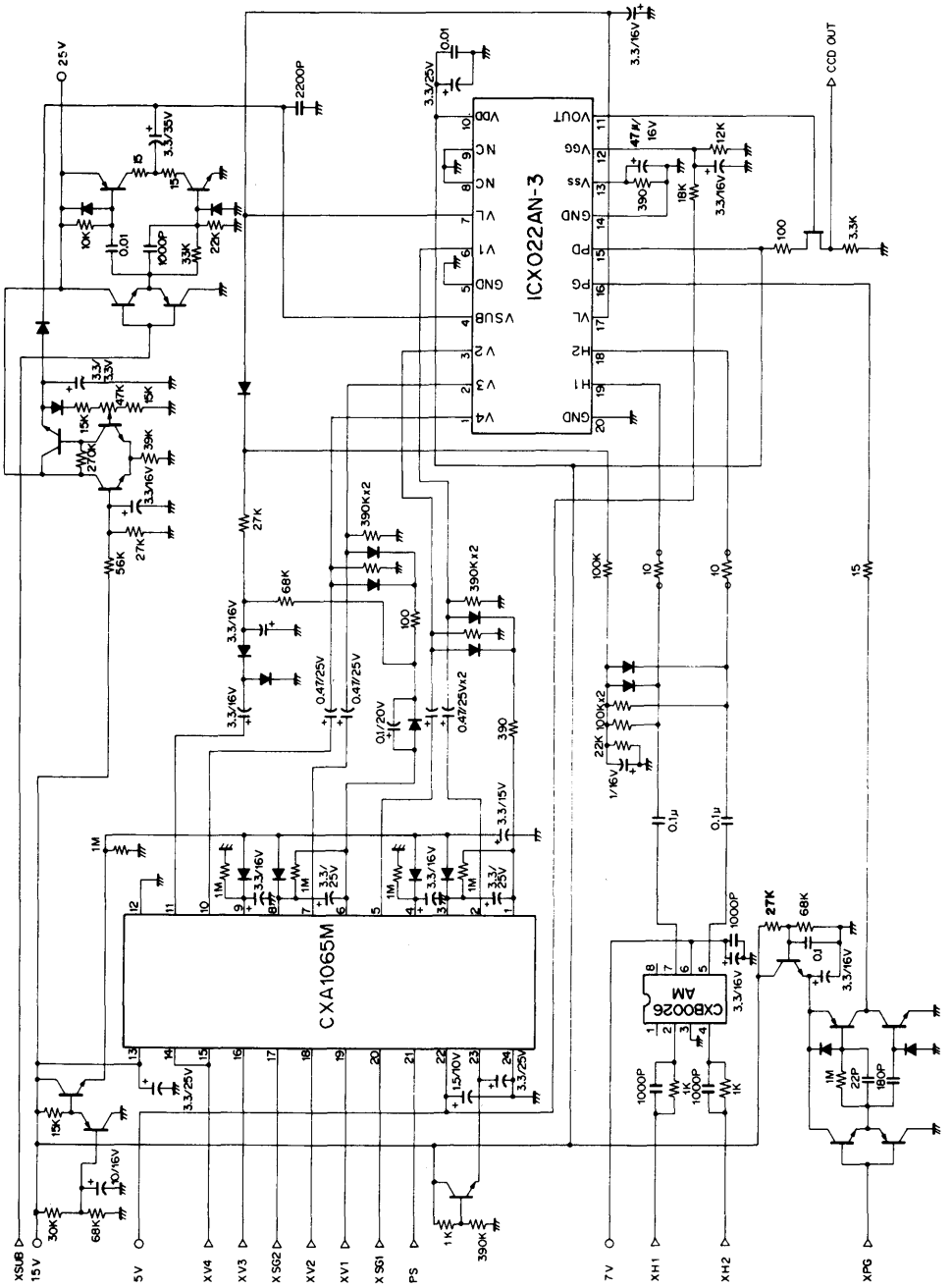
$$Lci = (\Delta Yli/Y_A) \times 100\ (\%) \quad (i = w, r, g, b)$$

11) Light a stroboscopic tube with the following timing and test the residual image.

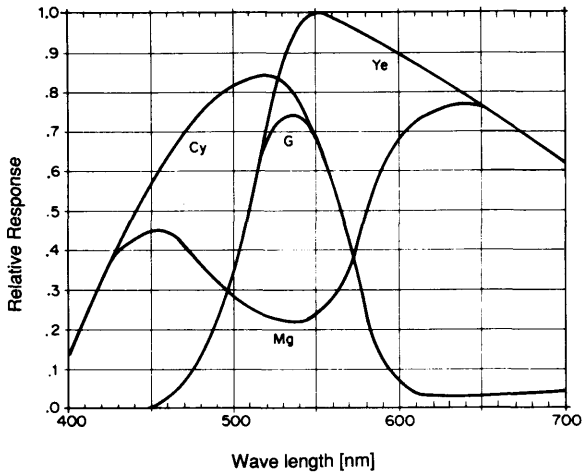
$$\Delta Ylag = (Ylag/Ys) \times 100\ (\%)$$



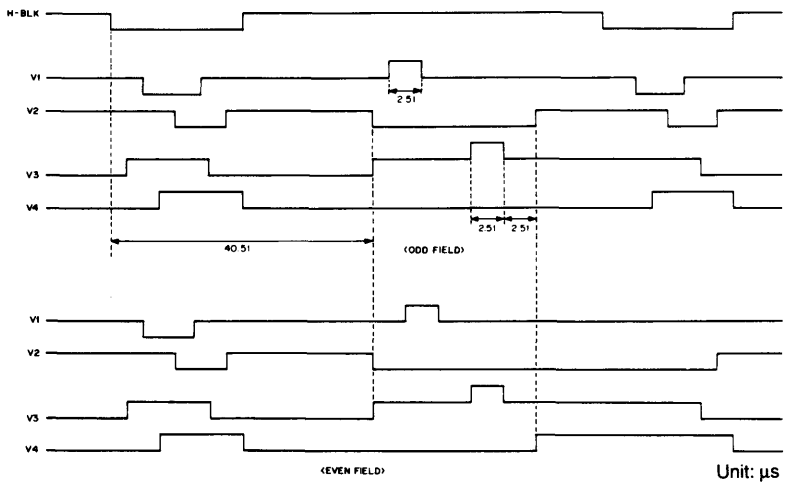
Drive Circuit



Spectral Sensitivity Characteristics (Excluding light source characteristics)
Fujinon lens H6 × 12.5R

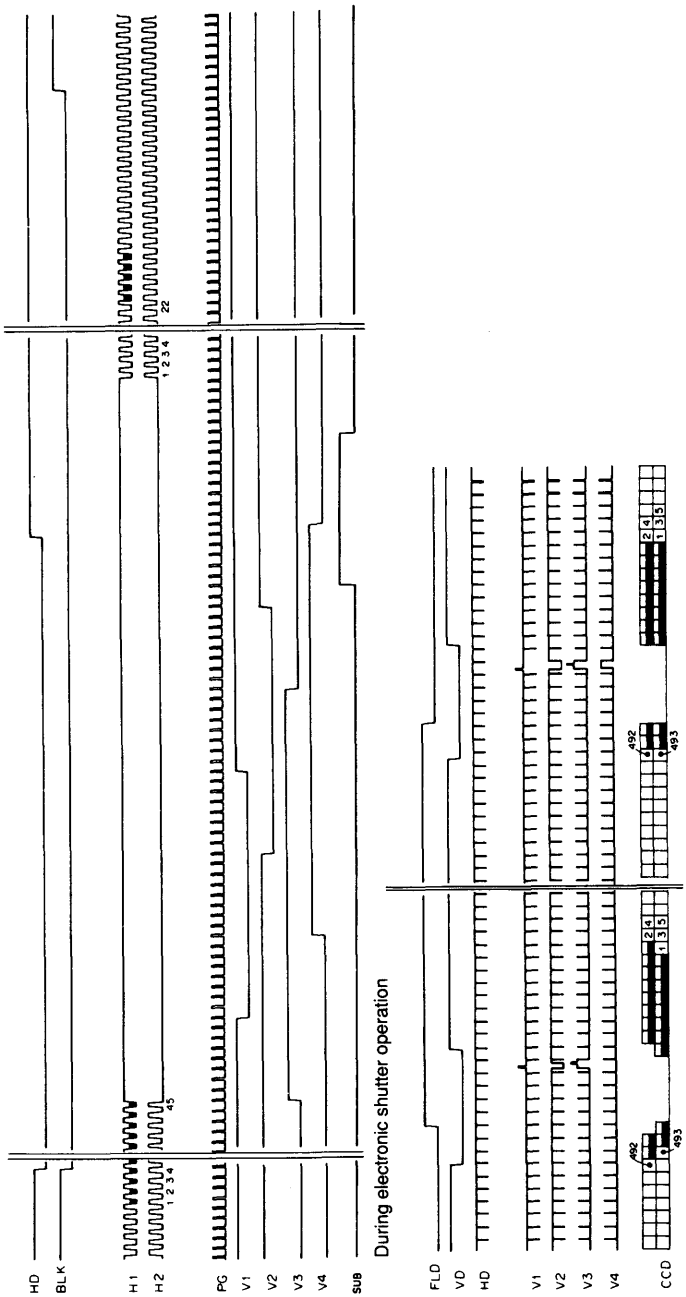


Using read out clock timing chart



Unit: µs

Drive Pulse Timing Chart



Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor. Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect there is no ROM or serial number.

Interline-type CCD Solid Image Sensor

Description

ICX024AN-3 is an interline-type CCD solid imaging device designed for color video cameras.
Effective pixels number 756 horizontally and 581 vertically.

HAD (Hole Accumulated Diode) sensors are employed as photosensor elements to ensure much reduced dark current.

Color filters incorporated Ye, G, Mg and Cy are mosaic filters of high resolution and high sensitivity.

The device employs the field integration system to obtain a high resolution.

Electric charges are swept out of the substrate, so the sensor has electronic shutter capability with variable charge storage time.

Features

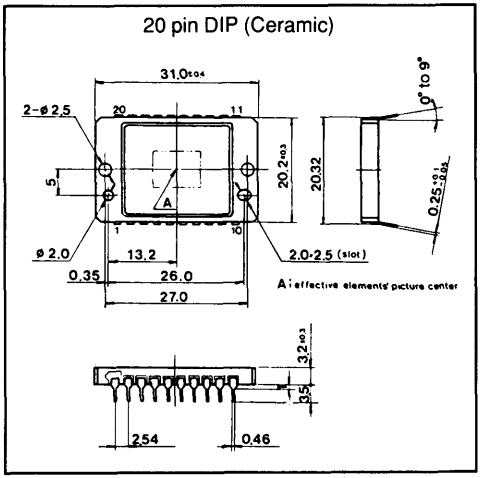
- Image size: 2/3 inches (8.8 mmH × 6.6 mmV)
- Effective pixels: 756H × 581V
- Effective optical black
  Horizontal: Front 5 pixels
  Back 55 pixels
  Vertical: Front 19 pixels
  Back 6 pixels
- High resolution
- High sensitivity
- Low noise
- Low smear
- Low dark current
- Electronic shutter
- Low antiblooming
- No graphic distortion, no microphonic noise
- γ characteristics: 1

Device Structure

- Interline type CCD image sensor
- Chip size: 10.0 mmH × 8.2 mmV
- Unit cell size: 11.0 μm (H) × 11.0 μm (V)
- Dummy bits: Horizontal 22-bits, vertical 1-bit
  (Even fields only)
- HAD (Hole Accumulated Diode) sensor
- High sensitivity output amplifier
- Ye, Cy, Mg, G on chip type complementary color mosaic filter
- N type substrate P-well structure

Package Outline

Unit: mm



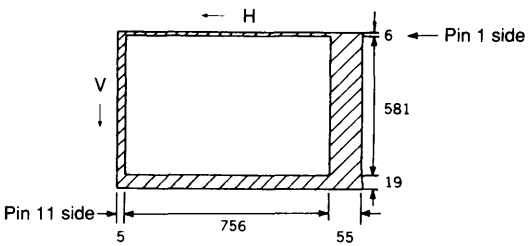
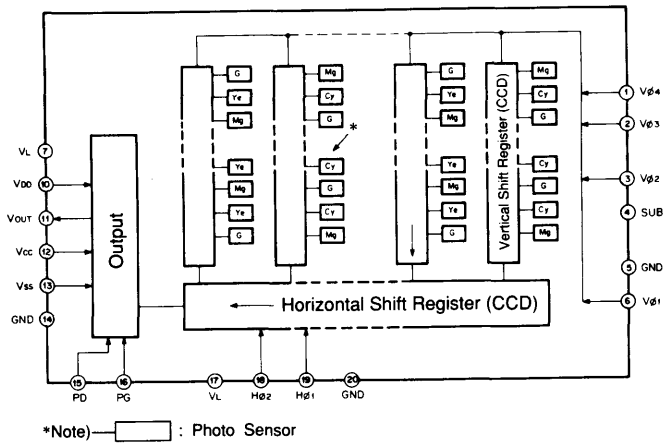


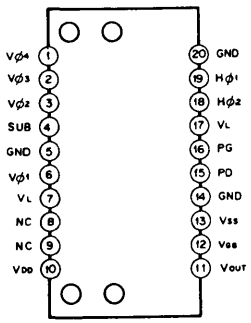
Fig. 1 Optical black configuration

E89143-YA

Imaging Device Function Block



Pin Configuration and Description (Top View)



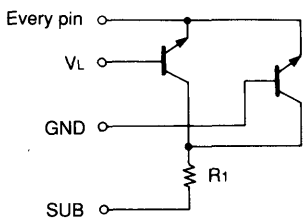
No.	Symbol	Description	No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	11	V_{OUT}	Signal output
2	$V\phi_3$	Vertical register transfer clock	12	V_{GG}	Output amplifier gate
3	$V\phi_2$	Vertical register transfer clock	13	V_{SS}	Output amplifier source
4	SUB	Substrate (OFD) bias	14	GND	GND
5	GND	GND	15	PD	Pre-charge drain bias
6	$V\phi_1$	Vertical register transfer clock	16	PG	Output reset clock
7	V_L	Protection transistor bias	17	V_L	Protection transistor bias
8	NC		18	$H\phi_2$	Horizontal register transfer clock
9	NC		19	$H\phi_1$	Horizontal register transfer clock
10	V_{DD}	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

Item	Ratings	Unit	Remarks
SUB-GND	-0.3 to +55	V	
V_{DD}, PD, V_{OUT}, V_{SS}-GND	-0.3 to +20	V	
V_{DD}, PD, V_{OUT}, V_{SS}-SUB	-55 to +10	V	Note 1
Horizontal and vertical transfer clock inputs - GND	-15 to +20	V	
Horizontal and vertical transfer clock inputs - SUB	-65 to +10	V	Note 1
Potential difference between vertical transfer clock inputs	+15	V	Note 2
Potential difference between horizontal transfer clock inputs	+17	V	
$H\phi_1$, $H\phi_2$ - $V\phi_4$	-17 to +17	V	
PG, V_{GG} - GND	-10 to +15	V	
PG, V_{GG} - SUB	-55 to +10	V	Note 1
V_L - SUB	-65 to +0.3	V	
Pins other than GND, SUB and V_L-V_L	-0.3 to +28	V	
Storage temperature	-30 to +80	°C	
Operation guarantee ambient temperature	-10 to +55	°C	

Note) 1. This imaging device consists of an N substrate P-Well structure where a protection transistor is connected to each pin accordingly. If a voltage exceeding 10 V is applied to pins other than V_L against the SUB pin, a punch through current will flow. Since a series resistance R_L is located between each pin and SUB, the device will withstand destruction through any rush voltage over 10 V.
The series resistance R_L must be more than 1 kΩ between Vp-p and SUB, more than 500 Ω between V_{OUT} and SUB and more than 5kΩ between Vss or PD and SUB. The series resistance between other pins (except V_L and GND) and SUB must be more than 5 kΩ.

① V_{DD}, PD, V_{OUT} and V_{SS} pins



② Pins other than ① (except V_L and GND)

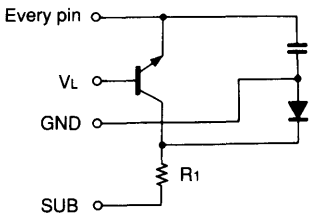


Fig. 2 Equivalent circuit

2. In case of clock width <10 µs and clock duty factor <0.1%, up to 27 V is guaranteed.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage of output circuit	V_{DD}	14.55	15.0	15.45	V	
	V_{PD}	14.55	15.0	15.45	V	Note 1
	V_{GG}	1.6	2.0	2.4	V	
	V_{SS}	Ground with a 390 Ω resistance				±5 %
Substrate voltage adjustable range	V_{SUB}	9		19	V	Note 2
Regulation range after substrate voltage adjustment	V_{SUB}	-3		3	%	
Protection transistor bias	V_L	-12	-11	Note 6	V	

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output circuit current	I_{DD}		5.0		mA	Note 3
Input current	I_{IN1}			1	μA	Note 4
	I_{IN2}			10	μA	Note 5

Note) 1. V_{PD} and V_{DD} must have the same voltage.

2. Indication of the substrate voltage (V_{SUB}) set value:
The set value is indicated on the rear of the imaging device by a code. Adjust to obtain the indicated voltage at the SUB pin.

V_{SUB} code – Two digit indication

The integral codes correspond to the following actual values:

Integral codes	9	A	B	C	D	E	F	G	H	I	J
Actual values	9	10	11	12	13	14	15	16	17	18	19

EX.) F5 → 15.5 (V)

3. Ground Vss with a 390Ω resistance.
4. 1) Current flowing to the ground when a voltage of 20 V is applied to V_{DD}, PD, V_{OUT}, V_{SS} and SUB pins. Test ground all the pins other than those under test.
   2) Current flowing to the ground when a voltage of 25 V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins in the order. Apply pin a voltage of 25 V to the SUB pin and ground pins other than those under test.
   3) Current flowing to the ground when a voltage of 15 V is applied to PG and V_{GG} pins in the order. Apply a voltage of 15 V to the SUB pin and ground pins other than those under test.
   4) Current flowing to the ground when V_L pin is grounded, GND and SUB pins are open and a voltage of 27 V is applied to other pins.
5. Current flowing to the ground when a voltage of 55 V is applied to the SUB pin. In this case ground pins other than those under test.
6. Vertical transfer clock low level clamp bias

Clock Voltage Conditions

Clock voltage

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Read clock voltage	V_{VT}	13.0		15.0	V	Note 1
Vertical transfer clock voltage	V_{VHH}			1.3	V	Note 2
	V_{VH}	-0.3		0.7	V	
	$V_{\phi V}$	8.0			V	
	V_{VLL}	-11.0			V	
Horizontal transfer clock voltage	V_{HHH}			5.5	V	Note 3
	V_{HL}	-3.0		-1.7	V	
	$V_{\phi H}$	5.2		8.0	V	
	V_{HLL}	-3.0			V	
Output reset clock voltage	V_{PGL}		0		V	Note 4
	$V_{\phi PG}$	7.0		13.0	V	
Substrate clock voltage	$V_{\phi SUB}$	23.0		27.0	V	Note 5

Clock capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Vertical transfer clock - GND	$C_{\phi V}$		5000		pF	
Capacitance between vertical transfer clocks	$C_{\phi VV}$		1500		pF	
Horizontal transfer clock - GND	$C_{\phi H}$		180		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Output reset clock - GND	$C_{\phi PG}$		10		pF	
Substrate clock - GND	$C_{\phi SUB}$		500		pF	

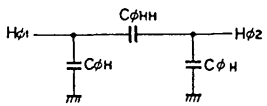


Fig. 4 Equivalent circuit of horizontal transfer clock capacitance

Note) 1. Read clock voltage

1) The symbol "ϕ_L" expresses the voltage level while the read clock "V_T" of the vertical transfer clocks ("$V\phi_1$" and "$V\phi_2$") is set. The maximum value in the read clock waveform is expressed as "ϕ_H".
2) The period in which the voltage level becomes ($\phi_H - \phi_L$)/2 is expressed as "tsr". The voltage levels at "tsr/2" are expressed as "V_{T1}" (at $V\phi_1$) and "V_{T3}" (at $V\phi_3$). The smaller of "V_{T1}" and "V_{T3}" is defined as the read clock voltage "V_{VT}".

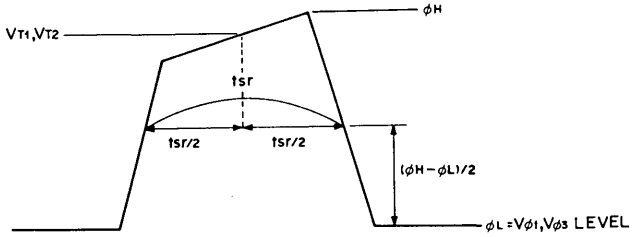


Fig. 5 Read clock waveform

2. Vertical clock voltage (Refer to Fig. 6)
T = 564 ns (with a horizontal driving frequency of 14.19 MHz)

1) Definition of the vertical transfer clock amplitude

Level 2T after the rising edge of "$V\phi_3$" is expressed as "V_{3A}".
Level T after the falling edge of "$V\phi_1$" is expressed as "V_{1B}".
Level 2T after the rising edge of "$V\phi_4$" is expressed as "V_{4A}".
Level T after the falling edge of "$V\phi_2$" is expressed as "V_{2B}".
Level 2T after the rising edge of "$V\phi_1$" is expressed as "V_{1A}".
Level T after the falling edge of "$V\phi_3$" is expressed as "V_{3B}".
Level 4T after the rising edge of "$V\phi_2$" is expressed as "V_{2A}".
Level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{4B}".

$V\phi_2$ level T after the falling edge of "$V\phi_1$" is expressed as "V_{2C}".
$V\phi_3$ level T after the falling edge of "$V\phi_2$" is expressed as "V_{3C}".
$V\phi_4$ level T after the falling edge of "$V\phi_3$" is expressed as "V_{4C}".
$V\phi_1$ level 3T after the falling edge of "$V\phi_4$" is expressed as "V_{1C}".

$\Delta 31 = (V_{3A} + V_{2C}) / 2 - V_{1B}$
$\Delta 42 = (V_{4A} + V_{3C}) / 2 - V_{2B}$
$\Delta 13 = (V_{1A} + V_{4C}) / 2 - V_{3B}$
$\Delta 24 = (V_{2A} + V_{1C}) / 2 - V_{4B}$

The minimum value of these is defined as the vertical transfer clock amplitude "$V\phi_V$".

2) The maximum value from V_{1A}, V_{2A}, V_{3A}, and V_{4A}, is defined as the high level V_{VH} of the clock.
3) The minimum level in a waveform which includes the vertical clock coupling is expressed as "V_{VLL}". "V_{VHH}" expresses the maximum level except in the period where read clock V_T is applied (in $V\phi_1$ and $V\phi_3$ only).

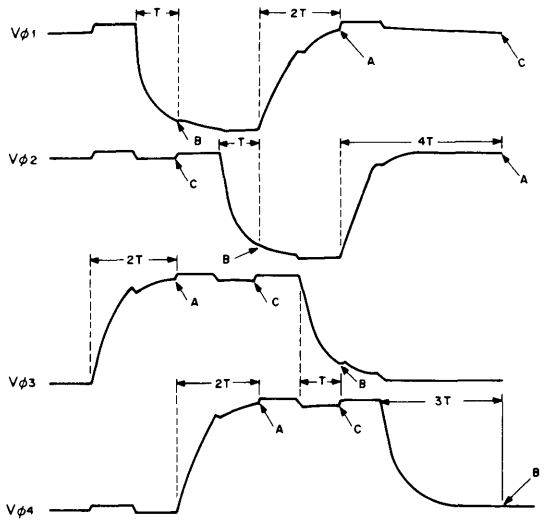


Fig. 6 Vertical transfer clock waveform
T = 564ns (with a horizontal driving frequency of 14.19 MHz)

3. Horizontal transfer clock voltage
   1) For the horizontal transfer clocks "Hφ1" and "Hφ2", the low-level period is expressed as "thl" and the high-level period is expressed as "thh". The symbol "tho" expresses the overlap period of "thl" and "thh".
   2) The low level at which "thl", "thh" and "tho" satisfy the following time duration is expressed as "H_{1B}" and "H_{2B}".
      And the high level is expressed as "H_{1A}" and "H_{2A}"

      thl ≥ 10 ns, thh ≥ 10 ns, tho ≥ 5 ns

      $\Delta 21 = H_{1A} - H_{2B}$
      $\Delta 12 = H_{2A} - H_{1B}$

      The smaller of Δ21 and Δ12 is defined as the horizontal transfer clock amplitude "$V_{\phi H}$". The low level at that point is expressed as "V_{HL}".
   3) The minimum level in the waveform which contains the coupling of the horizontal transfer clocks "Hφ1" and "Hφ2" is expressed as "V_{HLL}" and the minimum level is expressed as "V_{HHH}".

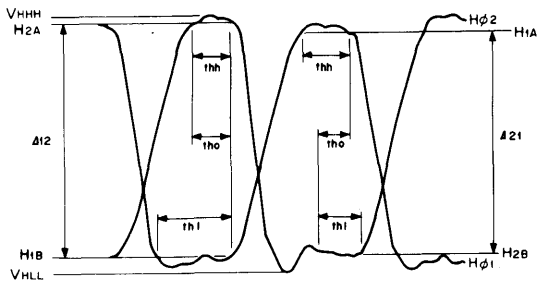


Fig. 7 Horizontal transfer clock waveform

4. Output reset clock voltage
   1) The low level of the output reset clock is to be the GND in the circuit.
   2) The amplitude of the output reset PG clock "$V\phi_{PG}$" is defined as the maximum value of the amplitude which provides a high level period over 10 ns.

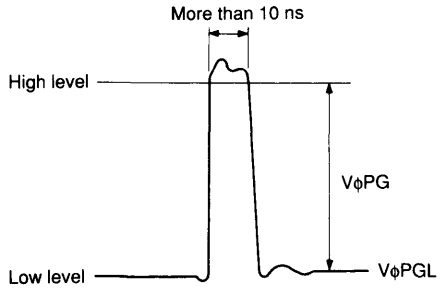


Fig. 8 Waveform of PG clock

5. Substrate clock voltage
   1) Substrate voltage is expressed as φL, and the substrate clock waveform maximum value as φH.
   2) The period where voltage level turns to (φH-φL)/2 is expressed as tsr. The difference between φL and voltage level at tsr/2 is defined as the substrate clock voltage VφSUB.

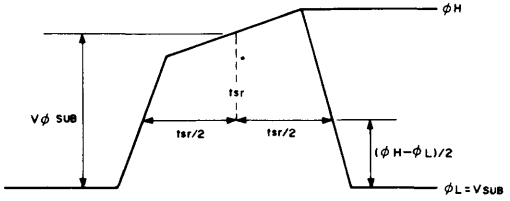


Fig. 9 Substrate clock waveform

Driving Clock Waveform Conditions

1. Definition of ϕ_H (100%) and ϕ_L (0%)
   1) For the horizontal transfer clocks ($H\phi_1$, $H\phi_2$), output reset clock (PGφ) and vertical transfer clocks ($V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$), the maximum value in the clock waveform which includes no coupling is expressed as "ϕ_H" and the minimum value is expressed as "ϕ_L".
   2) For the read clock (V_T), the maximum value in the clock waveform is expressed as "ϕ_H"."ϕ_L" expresses the voltage level while the read clock (V_T) of the vertical transfer clocks ($V\phi_1$, $V\phi_2$) is applied.
   3) For the substrate clock (SUBφ), the maximum value in the clock waveform is expressed as "ϕ_H" and the substrate voltage (V_{SUB}) as "ϕ_L".

2. Standard driving clock conditions (Typ.)

Horizontal drive frequency: 14.19 MHz

Clock (Symbol)	twh	twl	tr	tf	Unit	Remarks
Hφ1	18	33.7	10	8	ns	Imaging period
Hφ2	18	33.7	10	8		
Hφ1	4.9		0.01	0.01	µs	Parallel-serial converting period
Hφ2		4.9	0.01	0.01		
φPG	12	53.7	2	2	ns	
Vφ1/Vφ2	61.6	1.6	0.1	0.1	µs	Imaging period
Vφ3/Vφ4	2.8	60.45	0.05	0.1		
VφT	2.4		0.2	0.1		Reading period
SUBφ	1.0		0.08	0.1		Electron drained into substrate period

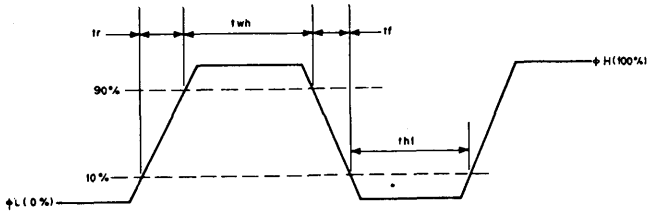


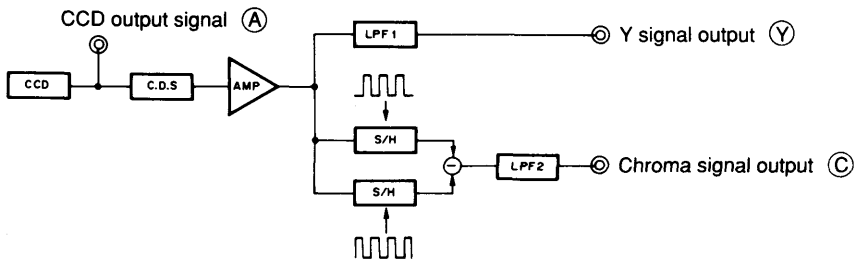
Fig. 10 Clock waveform

Imaging Characteristics

(See Fig. 10.)
Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Testing method	Remarks
Sensitivity	Sy	150	200		mV	1	
Output saturation signal	Ysat	500			mV	2	Ta=55°C
Smear	SM		0.007	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone ϕ, I
				25	%	5	Zone ϕ to II′
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
R-Y	Fcr			5	%	9	
B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			3.0	%	10	
G	Lcg			3.0	%	10	
B	Lcb			3.0	%	10	
W	Lcw			3.0	%	10	
Lag	ΔYlag			0.5	%	11	

Test Circuit



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

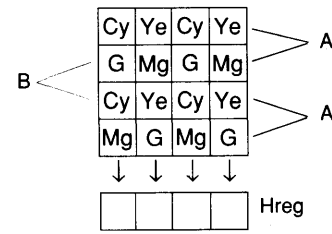
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through Horizontal register (H reg.) at line A1 are



Color Coding Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200°K Halogen source), at F5.6 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200°K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=200mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=200mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times 1/500 \times 1/10 \times 100\ (\%) \quad (1/10V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=200mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200mA. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Crmax - Crmin)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cbmax - Cbmin)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Ydmax.) and Min. (Ydmin.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 200 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$Fy = (\Delta Yf/Y_A) \times 100$ (%)

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

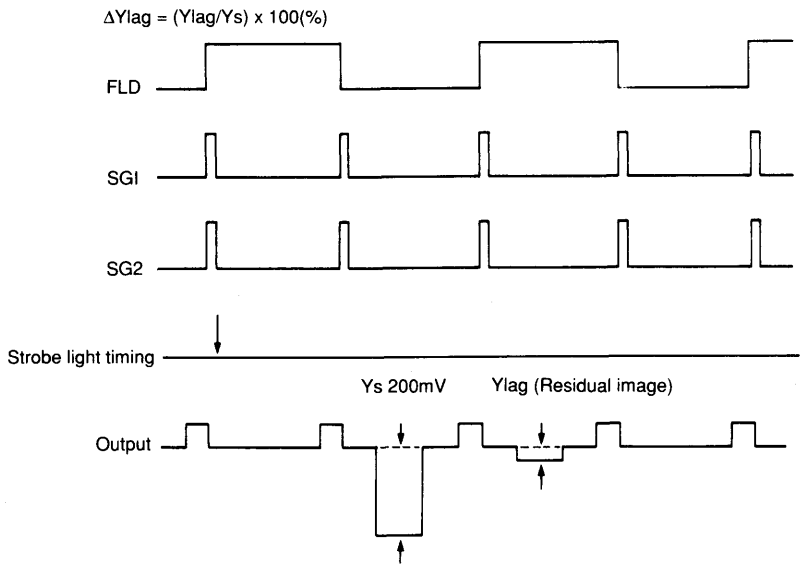
$Fci = (\Delta Ci/C_{Ai}) \times 100$ (%) (i = r, b)

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the C signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

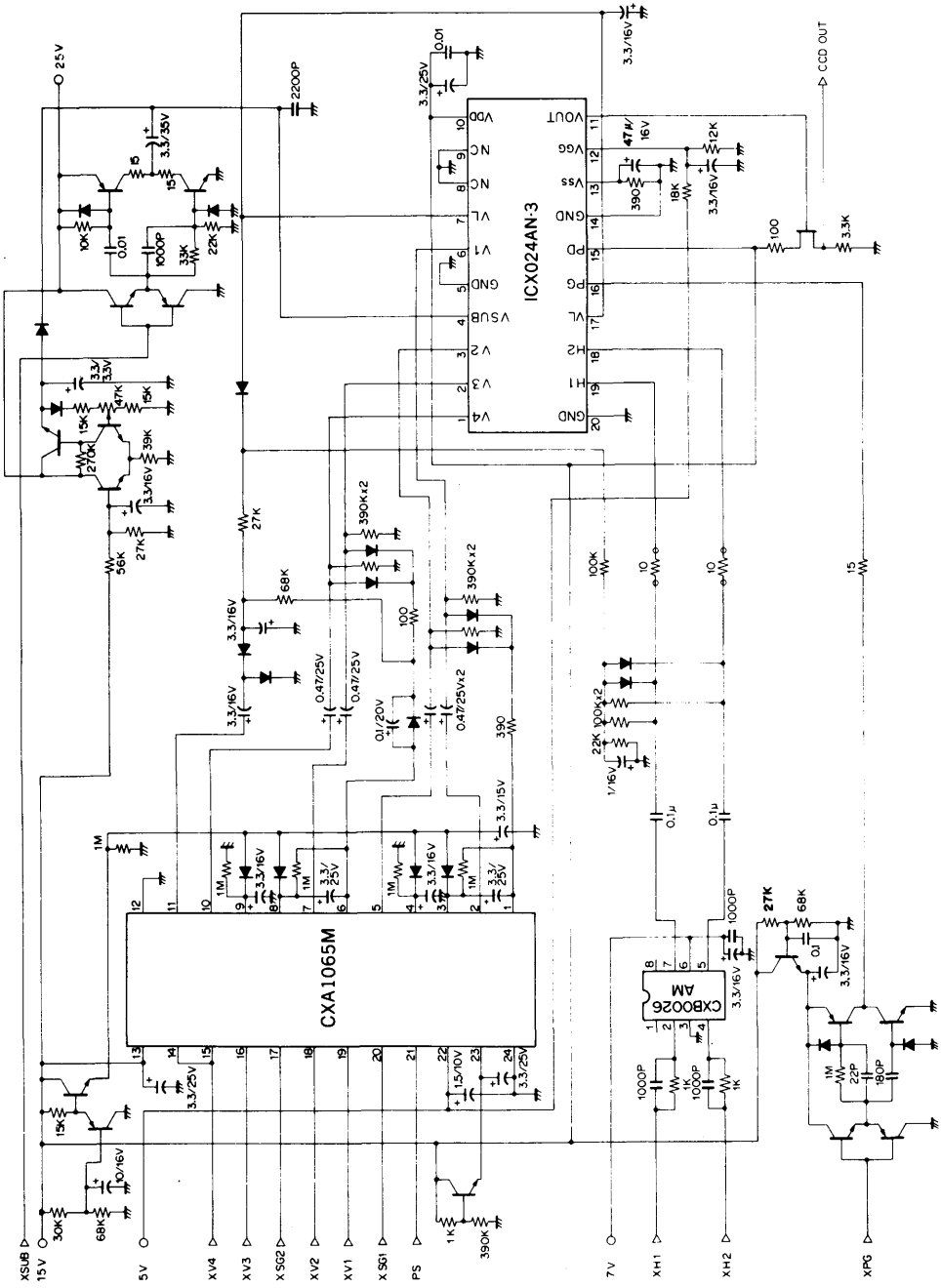
$Lci = (\Delta Yli/Y_A) \times 100$ (%) (i = w, r, g, b)

11) Light a stroboscopic tube with the following timing and test the residual image.

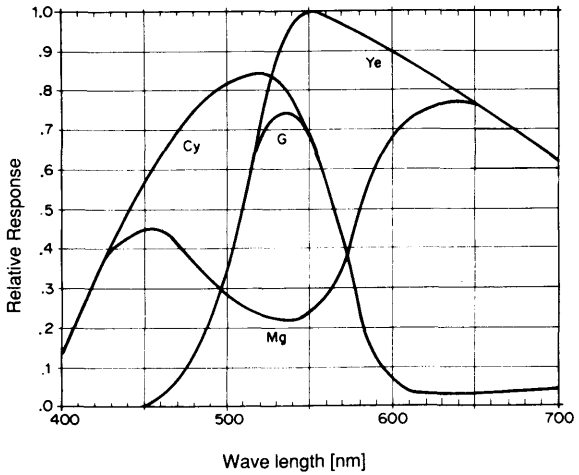
$\Delta Ylag = (Ylag/Ys) \times 100$ (%)



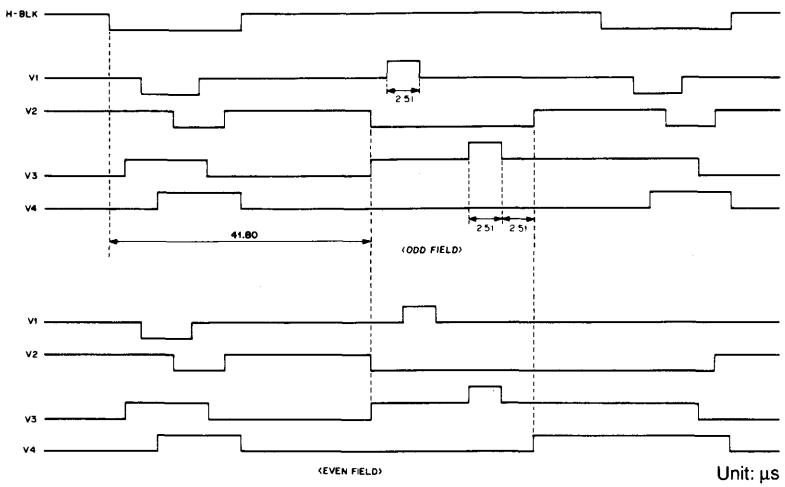
Drive Circuit



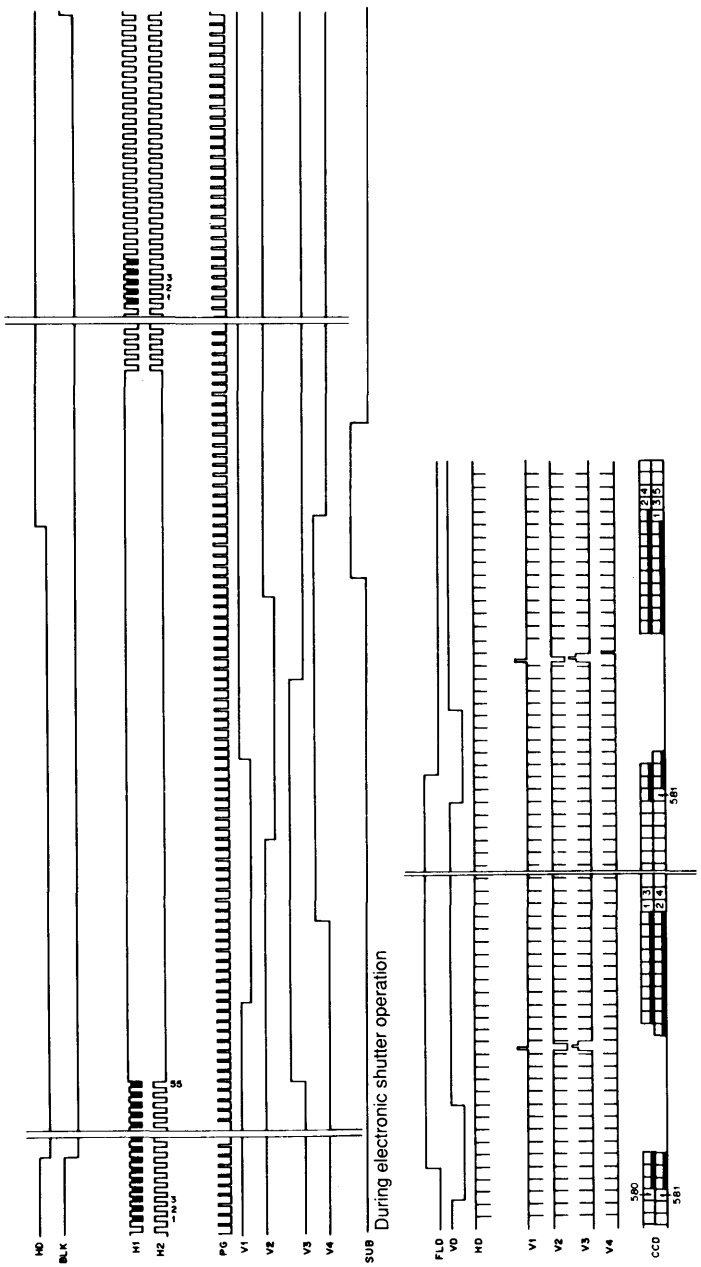
Spectral Sensitivity Characteristics (Excluding light source characteristics)
Fujinon lens H6 × 12.5R



Using read out clock timing chart



Drive Pulse Timing Chart (CCIR)



Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor. Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect there is no ROM or serial number.

SONY® ICX026BK

Solid-State Image Sensor for Color Camera

Description

ICX026BK is an interline transfer CCD solid-state imager suitable for NTSC 1/2 inch color video cameras. High sensitiveness is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole Accumulated Diode) sensors.

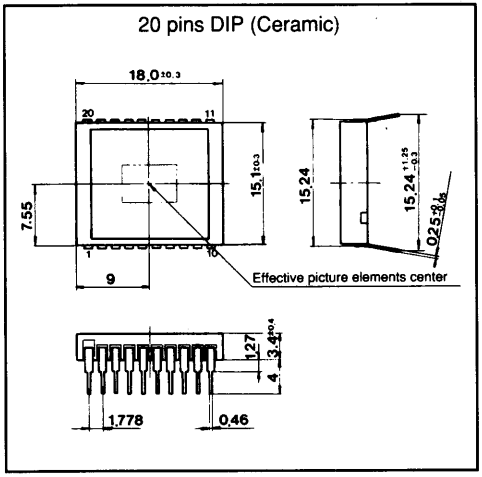
This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

Features

- High sensitivity (+6 dB compare with ICX026AK)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

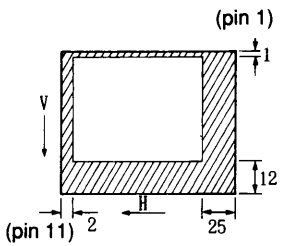
Package Outline

Unit: mm



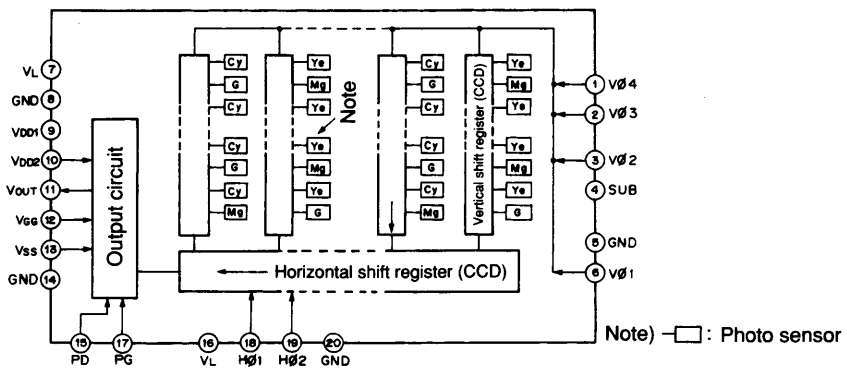
Device Structure

- Number of effective pixels 510 (H) × 492 (V)
- Number of total pixels 537 (H) × 505 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 μm (H) × 9.8 μm (V)
- Optical black
  - Horizontal (H) direction Front 2 pixels Rear 25 pixels
  - Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



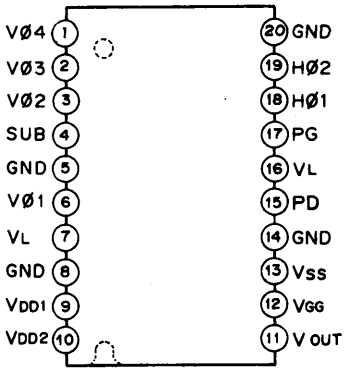
Optical black position (Top View)

Block Diagram



E89405-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	V_{OUT}	Signal output
2	Vφ3	Vertical register transfer clock	12	V_{GG}	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	V_L	Protective transistor bias
7	V_L	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	V_{DD1}	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	V_{DD2}	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	–0.3 to +55	V
• Supply voltage	V_{DD1}, V_{DD2}, PD, V_{OUT}, Vss, – GND	–0.3 to +18	V
	V_{DD1}, V_{DD2}, PD, V_{OUT}, Vss, – SUB	–55 to +10	V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	–15 to +20	V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	–65 to +10	V
• Voltage difference between vertical clock input pins		+15	V *(Max.)
• Voltage difference between horizontal clock input pins		+17	V (Max.)
• Hφ1, Hφ2, – Vφ4,		–17 to +17	V
• PG, V_{GG} – GND		–10 to +15	V
• PG, V_{GG} – SUB		–55 to +10	V
• V_L – SUB		–65 to +0.3	V
• Beside GND, SUB, V_L – V_L		–0.3 to +30	V
• Storage temperature		–30 to +80	°C
• Operating temperature		–10 to +55	°C

***Note)** +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display

□ □
↑ ↑
Integral part Decimal part

The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, V_{SS} and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

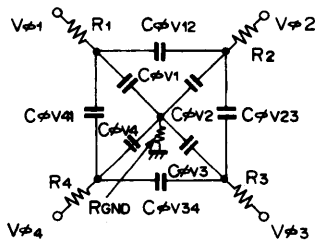
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	–0.2	0	0.2	V	1,2,3,6	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	–9.6	–9.0	–8.3	V	1,2,3,6	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	–0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	–0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	–0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	–0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0		34.0	V	4	*5

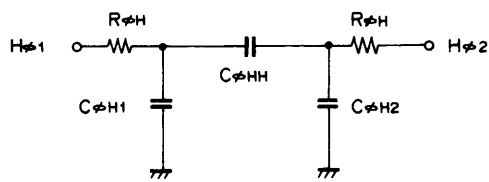
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		750		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

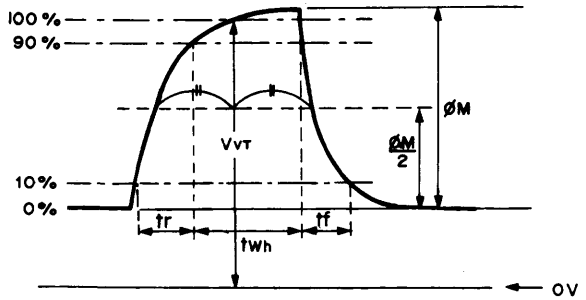


Fig.1

2. Vertical transfer clock waveform

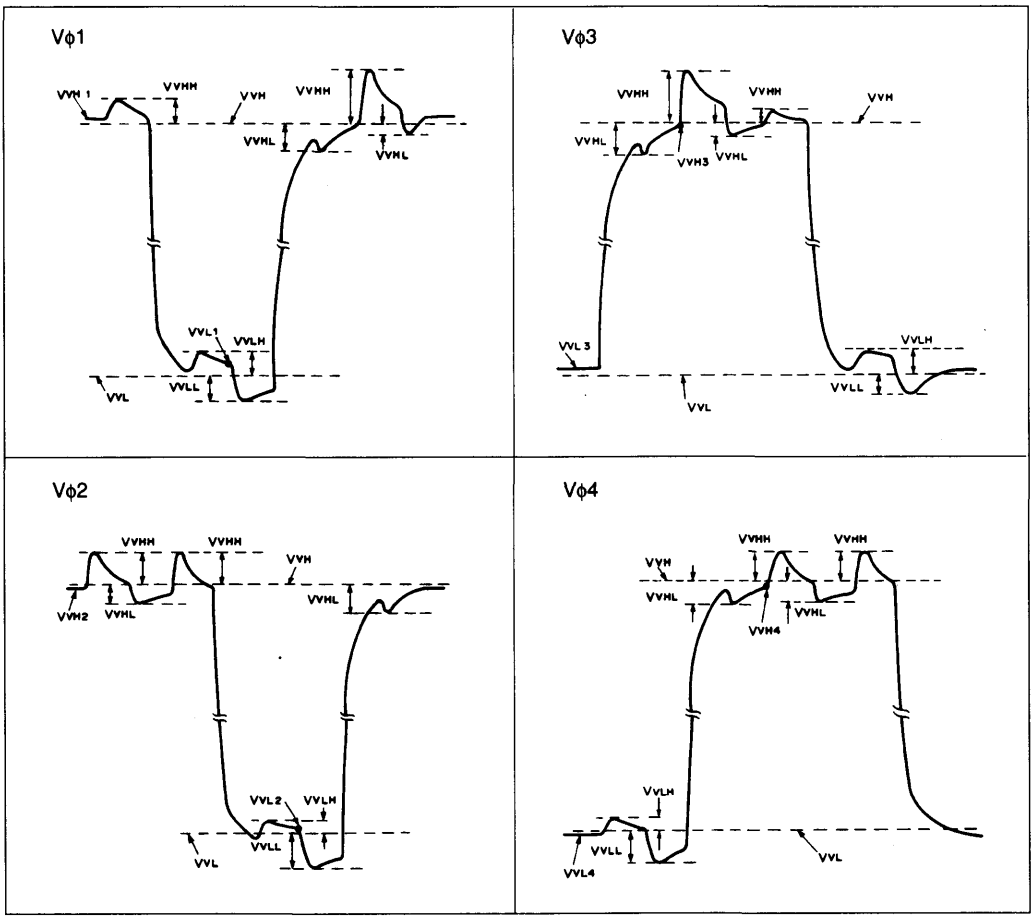


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

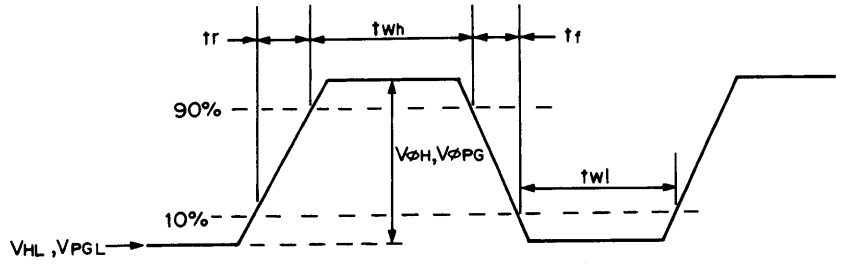


Fig. 3

4. Substrate clock waveform

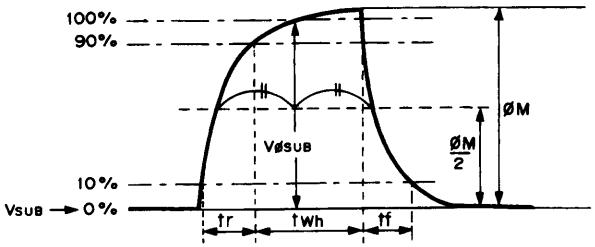


Fig. 4

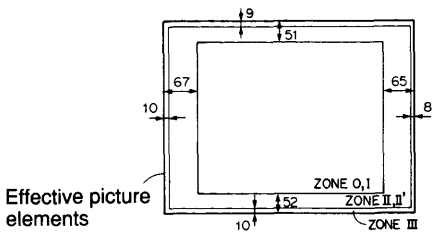
Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	$V\phi_1, V\phi_2, V\phi_3, V\phi_4$									0.45	0.015		0.25	µs	*
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.01		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.01		µs	During parallel serial conversion.
Precharge gate clock	ϕ_{PG}	15	17		75	81			4			3		ns	
Substrate clock	ϕ_{SUB}	1.5	2.1							0.5			0.5	µs	During charge drain.

***Note)** When vertical transfer clock driver CXD1250 is in use.

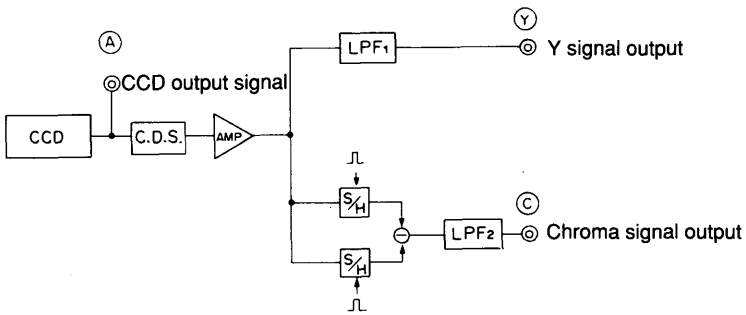
Operating Characteristics Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	260	340		mV	1	Ta=55°C
Saturation signal	Ysat	500			mV	2	
Smear	SM		0.005	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zone0, I
				25	%	5	Zone0 to II'
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
Flicker R-Y	Fcr			5	%	9	
Flicker B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			4	%	10	
Horizontal stripes G	Lcg			4	%	10	
Horizontal stripes B	Lcb			4	%	10	
Horizontal stripes W	Lcw			4	%	10	
Lag	ΔYlag			0.5	%	11	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

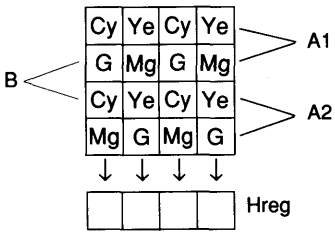
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are



Color Coating Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200°K Halogen source), at F5.6 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200°K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=150mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=150mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Crmax - Crmin)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cbmax - Cbmin)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Yd max.) and Min. (Yd min.) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$Fy = (\Delta Yf/Y_A) \times 100$ (%)

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

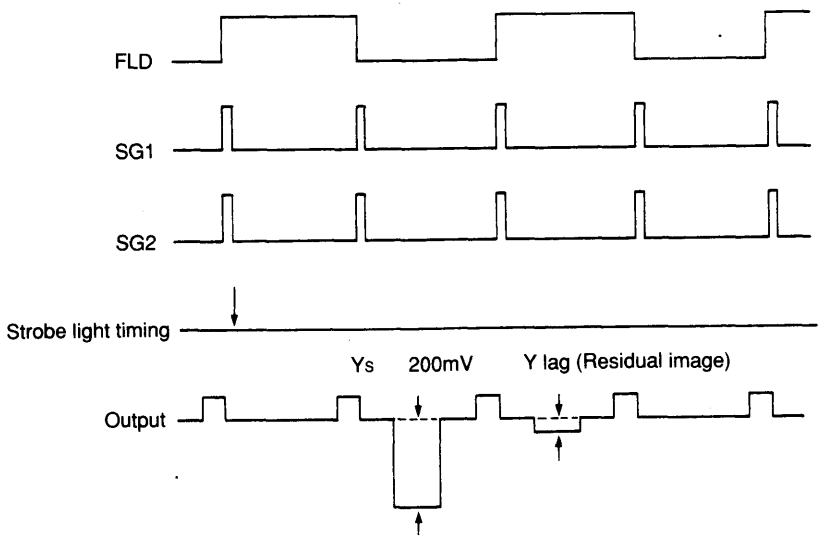
$Fci = (\Delta Ci/C_{Ai}) \times 100$ (%) (i = r, b)

10) Set to standard imaging condition II. Insert W, R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

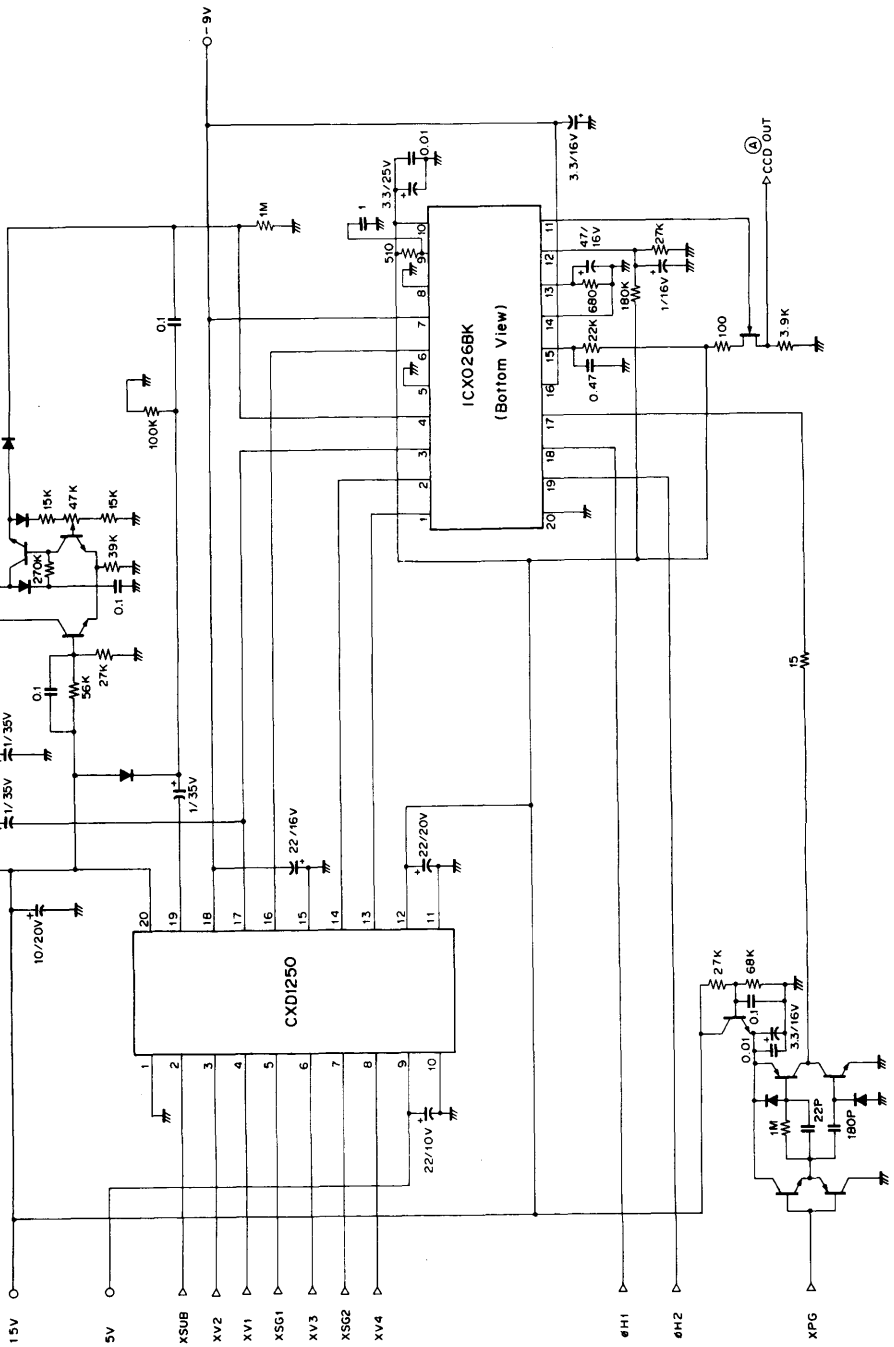
$Lci = (\Delta Yli/Y_A) \times 100$ (%) (i = w, r, g, b)

11) Light a stroboscopic tube with the following timing and test the residual image.

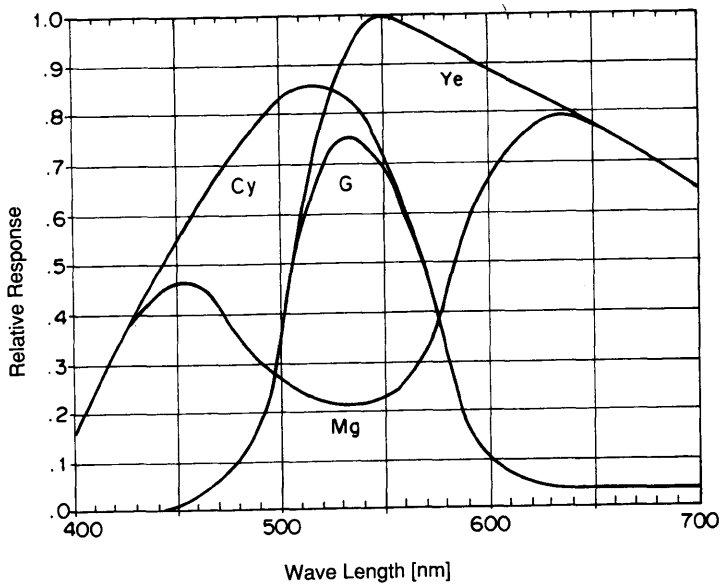
$\Delta Ylag = (Ylag/Ys) \times 100$ (%)



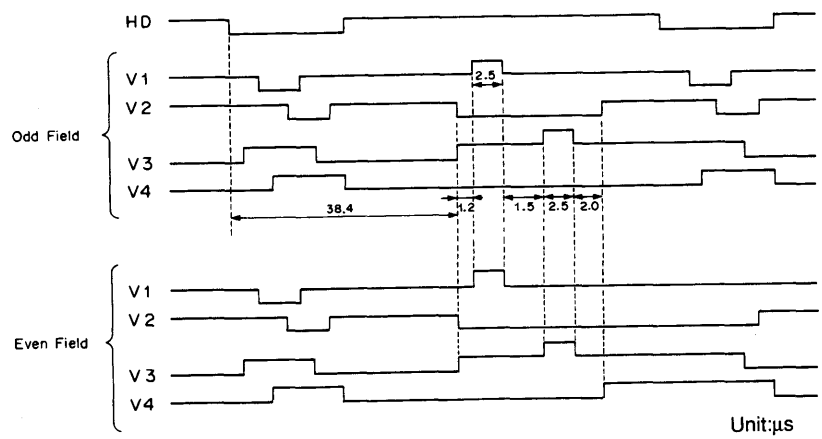
Drive Circuit



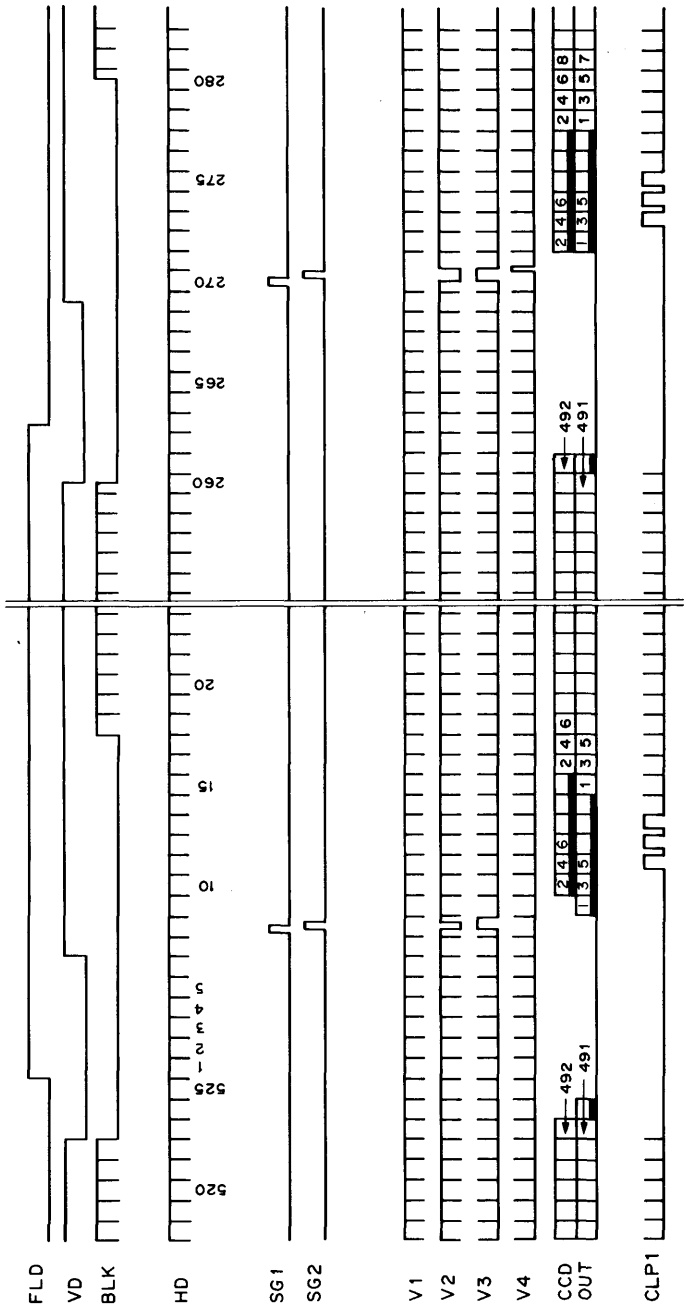
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



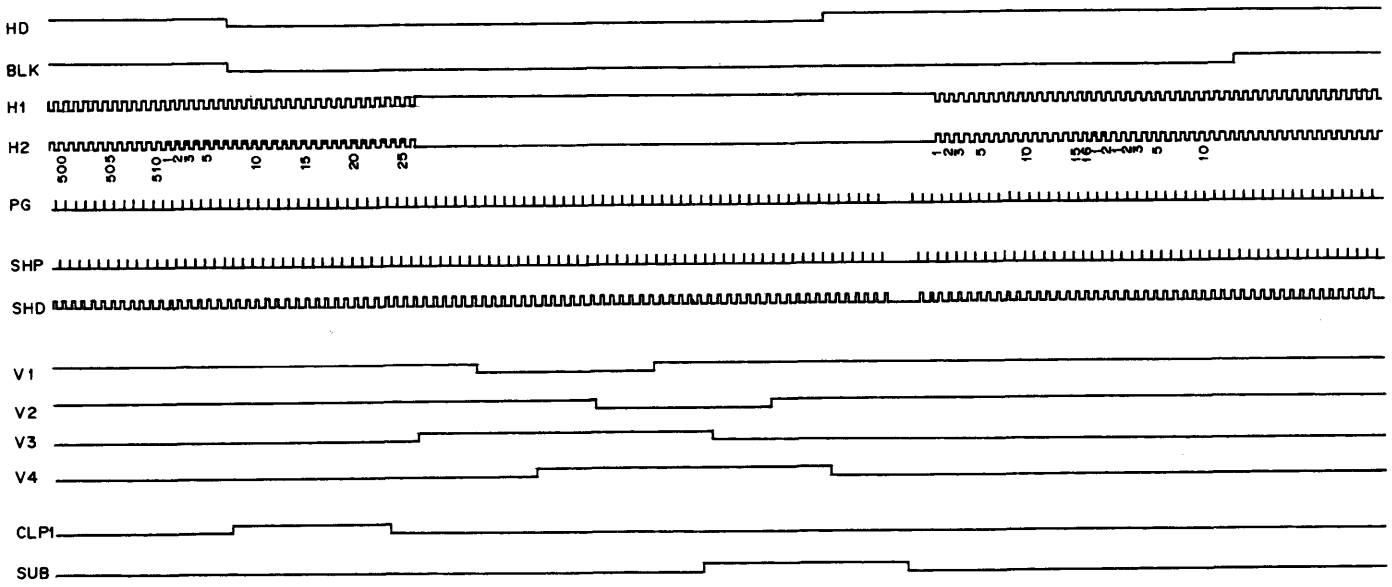
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

Solid-State Image Sensor for Color Camera

Description

ICX027BK is an interline transfer CCD solid-state imager suitable for PAL 1/2 inch color video cameras. High sensitiveness is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole Accumulated Diode) sensors.

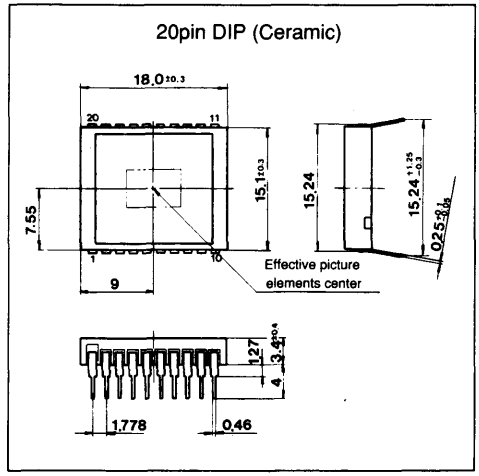
This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

Features

- High sensitivity (+6 dB compare with ICX027AK)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

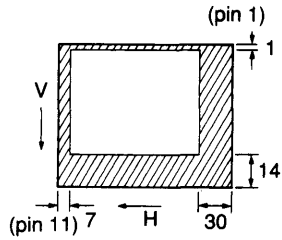
Package Outline

Unit: mm



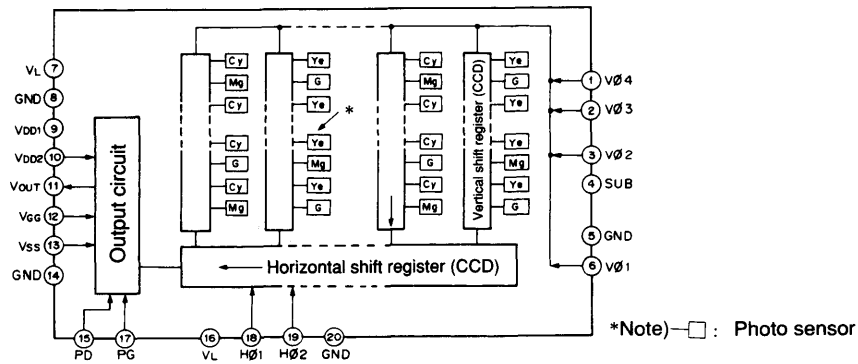
Device Structure

- Number of effective pixels 500 (H) × 582 (V)
- Number of total pixels 537 (H) × 597 (V)
- Interline transfer CCD image sensor
- Chip size 7.84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 μm (H) × 8.3 μm (V)
- Optical black
  - Horizontal (H) direction Front 7 pixels Rear 30 pixels
  - Vertical (V) direction Front 14 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

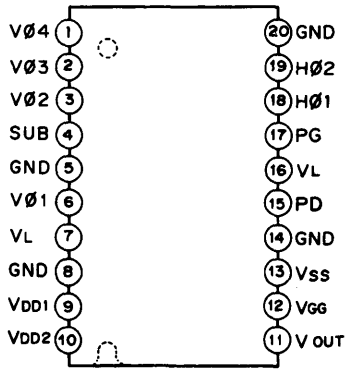
Block Diagram



*Note)—□ : Photo sensor

E89406-YA

Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	11	VOUT	Signal output
2	Vφ3	Vertical register transfer clock	12	VGG	Output amplifier gate bias
3	Vφ2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	Vφ1	Vertical register transfer clock	16	VL	Protective transistor bias
7	VL	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	Hφ1	Horizontal register transfer clock
9	VDD1	Output amplifier drain supply	19	Hφ2	Horizontal register transfer clock
10	VDD2	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	−0.3 to +55 V
• Supply voltage	VDD1, VDD2, PD, VOUT, Vss, – GND	−0.3 to +18 V
	VDD1, VDD2, PD, VOUT, Vss, – SUB	−55 to +10 V
• Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – GND	−15 to +20 V
	Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, Hφ2 – SUB	−65 to +10 V
• Voltage difference between vertical clock input pins		15 V* (Max.)
• Voltage difference between horizontal clock input pins		17 V (Max.)
• Hφ1, Hφ2, – Vφ4,		−17 to +17 V
• PG, VGG – GND		−10 to +15 V
• PG, VGG – SUB		−55 to +10 V
• VL – SUB		−65 to +0.3 V
• Beside GND, SUB, VL – VL		−0.3 to +30 V
• Storage temperature		−30 to +80°C
• Operating temperature		−10 to +55°C

***Note)** +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1}, V_{DD2}	14.55	15.0	15.45	V	V_{DD1} = V_{DD2}
Precharge drain voltage	V_{PD}	14.55	15.0	15.45	V	V_{PD} = V_{DD1} = V_{DD2}
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	I_{DD} = I_{DD1} + I_{DD2}
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1. Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display □ □

↑ Integral part ↑ Decimal part

The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical Value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, Vss and SUB pin. However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins Vφ1, Vφ2, Vφ3, Vφ4, Hφ1, and Hφ2. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4. 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

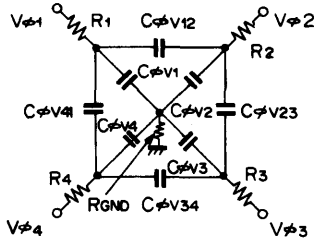
Clock Voltage Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	No.	Remarks
Read out clock voltage	V_{VT}	14.3	15.0	15.7	V	2,6	*1
Vertical transfer clock voltage *2	V_{VH1},V_{VH2},V_{VH3},V_{VH4}	−0.2	0	0.2	V	1,2,3,6	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VL1},V_{VL2},V_{VL3},V_{VL4}	−9.6	−9.0	−8.3	V	1,2,3,6	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V_{\phi V}$	8.1	9.0	9.8	V	1,2,3,6	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.2	V	3,6	
	$V_{VH3} - V_{VH}$	−0.4		0.1	V	2,3,6	
	$V_{VH4} - V_{VH}$	−0.4		0.1	V	1,3,6	
	V_{VHH}			0.8	V	1,2,3,6	High level coupling
	V_{VHL}			1.0	V	1,2,3,6	High level coupling
	V_{VLH}			0.8	V	1,2,3,6	Low level coupling
	V_{VLL}			0.8	V	1,2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.7	5.0	5.3	V	18,19	*3
	V_{HL}	−0.05	0	0.05	V	18,19	
Precharge gate clock voltage	$V_{\phi PG}$	8.0		11.5	V	17	*4
	V_{PGL}	−0.1	0	0.1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23.0		34.0	V	4	*5

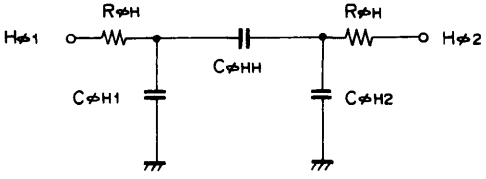
Note) *1. See Fig. 1.
*2. See Fig. 2.
*3. See Fig. 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1400		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		900		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1,R_2,R_3,R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		10		Ω	



Vertical transfer clock equivalent circuit



Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

1. Read out clock waveform

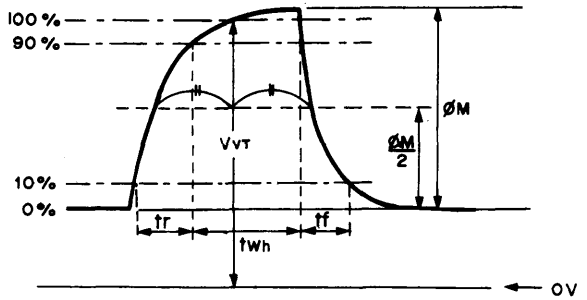


Fig.1

2. Vertical transfer clock waveform

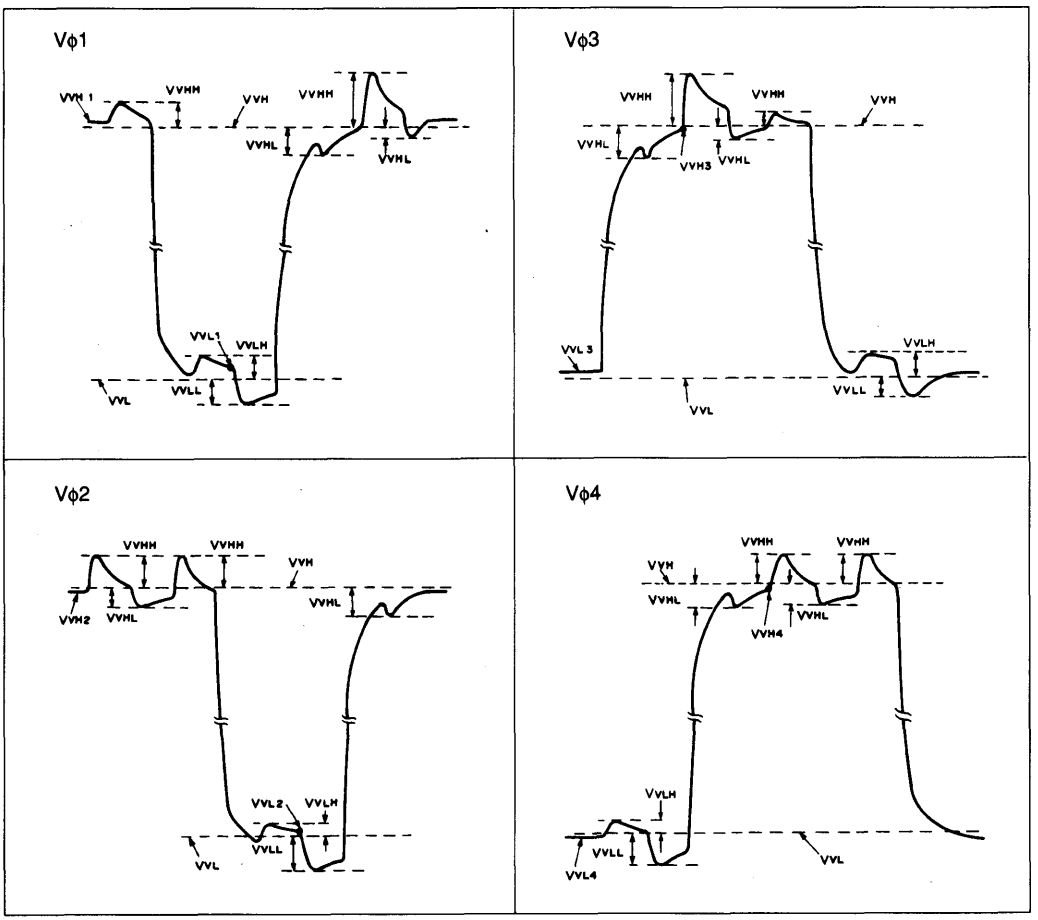


Fig.2

3. Horizontal transfer clock waveform/Precharge gate clock waveform

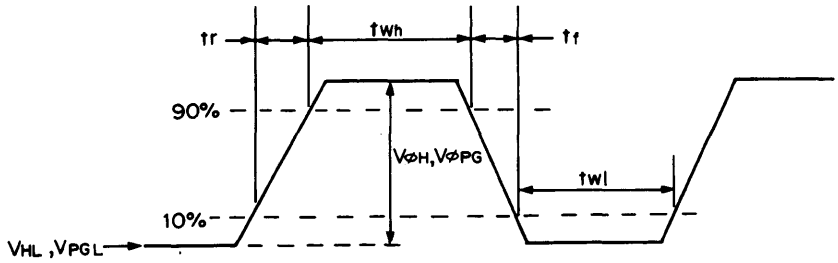


Fig. 3

4. Substrate clock waveform

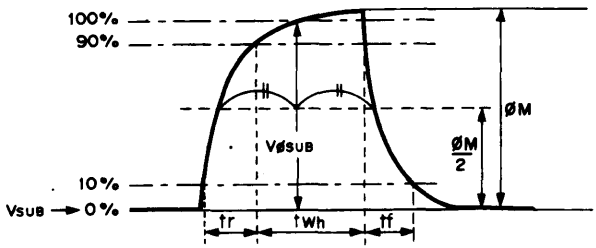


Fig. 4

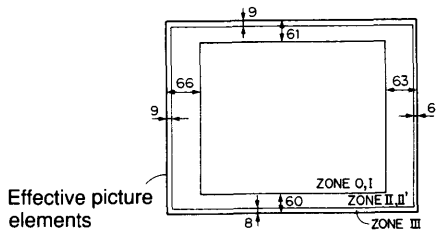
Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	1.5	1.85							0.5			0.5	µs	During read out
Vertical transfer clock	$V\phi_1, V\phi_2, V\phi_3, V\phi_4$									0.45	0.015		0.25	µs	*
Horizontal transfer clock	$H\phi$	38	42		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.01		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.01		µs	During parallel serial conversion.
Precharge gate clock	ϕ_{PG}	15	17		76	82			4			3		ns	
Substrate clock	ϕ_{SUB}	1.5	2.1							0.5			0.5	µs	During charge drain.

***Note)** When vertical transfer clock driver CXD1250 is in use.

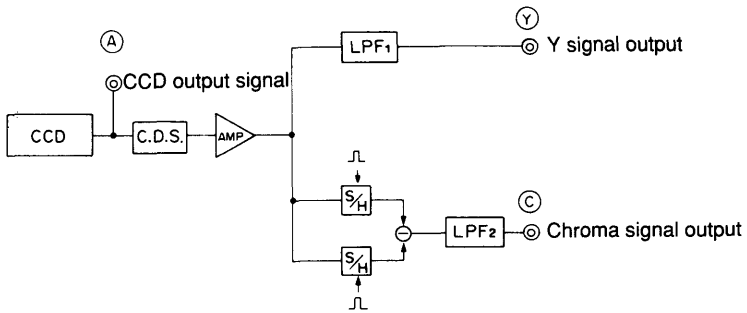
Operating Characteristics Ta = 25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	320		mV	1	
Saturation signal	Ysat	450			mV	2	Ta=55°C
Smear	SM		0.005	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SHy			20	%	5	Zon0, I
				25	%	5	Zone0 to II'
Uniformity between signal channels	ΔSr			10	%	6	
	ΔSb			10	%	6	
Dark signal	Ydt			2	mV	7	Ta=55°C
Dark signal shading	ΔYdt			1	mV	8	Ta=55°C
Flicker Y	Fy			2	%	9	
Flicker R-Y	Fcr			5	%	9	
Flicker B-Y	Fcb			5	%	9	
Horizontal stripes R	Lcr			4	%	10	
Horizontal stripes G	Lcg			4	%	10	
Horizontal stripes B	Lcb			4	%	10	
Horizontal stripes W	Lcw			4	%	10	
Lag	ΔYlag			0.5	%	11	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

Test Method

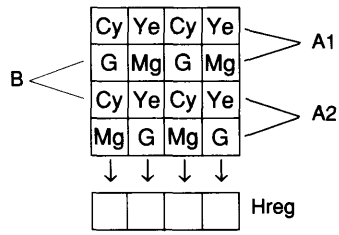
Test conditions

1) Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

2) Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OPB) is set as the reference for the signal output which is taken as the Y signal output or the Chroma signal output of the testing system.

Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals.

CFA of this imager is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The readout line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are



Color Coating Diagram

[G+Cy], [Mg+Ye], [G+Cy], [Mg+Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows:

$$Y = \{(G+Cy) + (Mg+Ye)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg+Ye) - (G+Cy)\}$$
$$= \{2R-G\}$$

Next, the signals through H reg. at line A2 are

[Mg+Cy], [G+Ye], [Mg+Cy], [G+Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G+Ye) + (Mg+Cy)\} \times 1/2$$
$$= 1/2\ \{2B+3G+2R\}$$

$$-(B-Y) = \{(G+Ye) - (Mg+Cy)\}$$
$$= -\{2B-G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R–Y and –(B–Y) on alternate lines.
It is the same for B field.

Definition of Standard Imaging Conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 Nit, 3200°K Halogen source), at F5.6 with a typical test lens, and CM-500S (1.0 mmt) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200°K and CM-500S (1.0 mmt) as IR cut filter. The light intensity is adjusted in accordance with the average value of Y signals (Y_A) indicated in each item.

1) Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2) Set to imaging condition II. Adjust light intensity to 10 times when Y signal output average value Y_A=150mV. Then test Y signal Min. Value.

3) Set to imaging condition II. Adjust light intensity to 500 times when Y signal output average value Y_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value Y_{SM} of Ysignal output.

$$SM = (Y_{SM}/Y_A) \times {}^1/_{500} \times {}^1/_{10} \times 100\ (\%) \quad ({}^1/_{10}V)$$

4) Set to imaging condition II. Adjust light intensity to 1000 times when Y signal output average value Y_A=150mV. Then check that there is no blooming.

5) Video signal shading SHy
Set to standard imaging condition II. Test Y signal Max. (Y max.) and Min. (Y min.) values. Adjust light intensity to obtain a Y signal output average value (Y_A) of about 150mV.

$$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

6) Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150mV. Test the Max. (Cr max. and Cb max.) and Min. (Cr min. and Cb min.) values of C signals from R-Y and B-Y channels.

$$\Delta Sr = |\ (Crmax - Crmin)/Y_A\ | \times 100\ (\%)$$
$$\Delta Sb = |\ (Cbmax - Cbmin)/Y_A\ | \times 100\ (\%)$$

7) Test the average Y signal voltage when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference.

8) Following 7, test Max. (Yd max) and Min. (Yd min) values of Y signal output. Only keep spot defects out of this range.

$$\Delta Ydt = Ydmax - Ydmin$$

9) ① Fy
Set to standard imaging condition II. Adjust light intensity to obtain a Y signal output average value (Y_A) of 150 mV. Test the Y signal difference (ΔYf) between even field and odd field.

$$Fy = (\Delta Yf/Y_A) \times 100\ (\%)$$

② Fcr, Fcb
Set to standard imaging condition II. Insert R and B filter respectively, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (C_{Ar}, C_{Ab}). At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

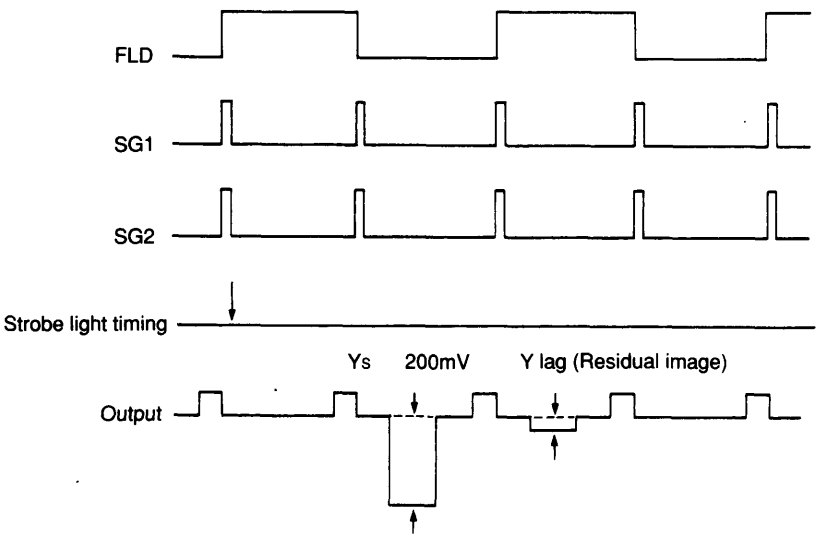
$$Fci = (\Delta Ci/C_{Ai}) \times 100\ (\%) \quad (i = r, b)$$

10) Set to standard imaging condition II. Insert W,R,G and B filters respectively and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field. At that time, adjust light intensity to obtain a Y signal output average value (Y_A) of 100 mV.

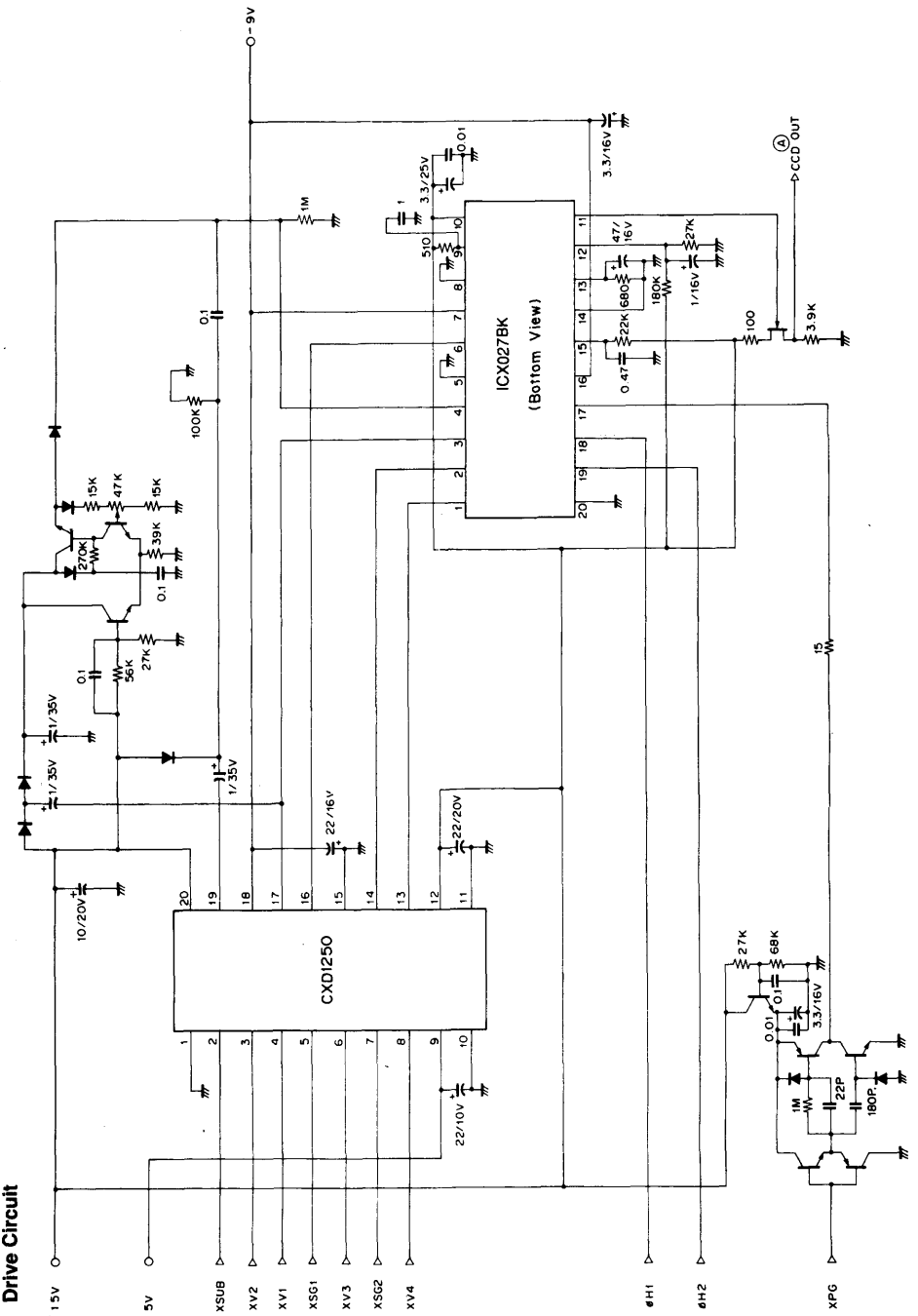
$$Lci = (\Delta Yli/Y_A) \times 100\ (\%) \quad (i = w, r, g, b)$$

11) Light a stroboscopic tube with the following timing and test the residual image.

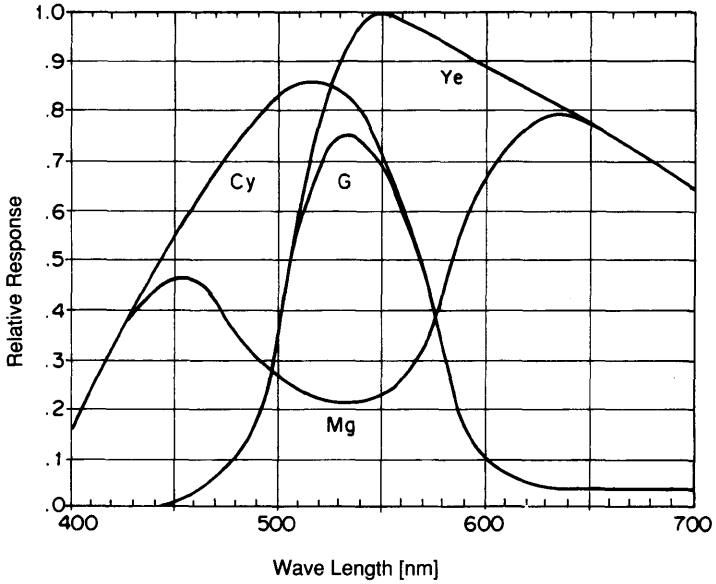
$$\Delta Ylag = (Ylag/Ys) \times 100\ (\%)$$



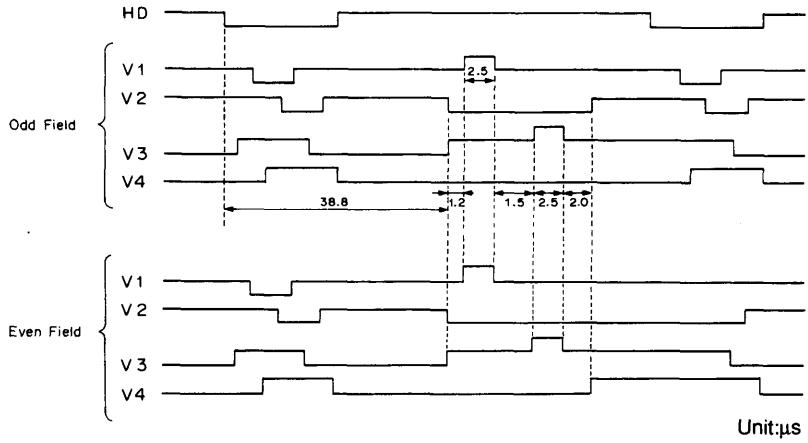
Drive Circuit



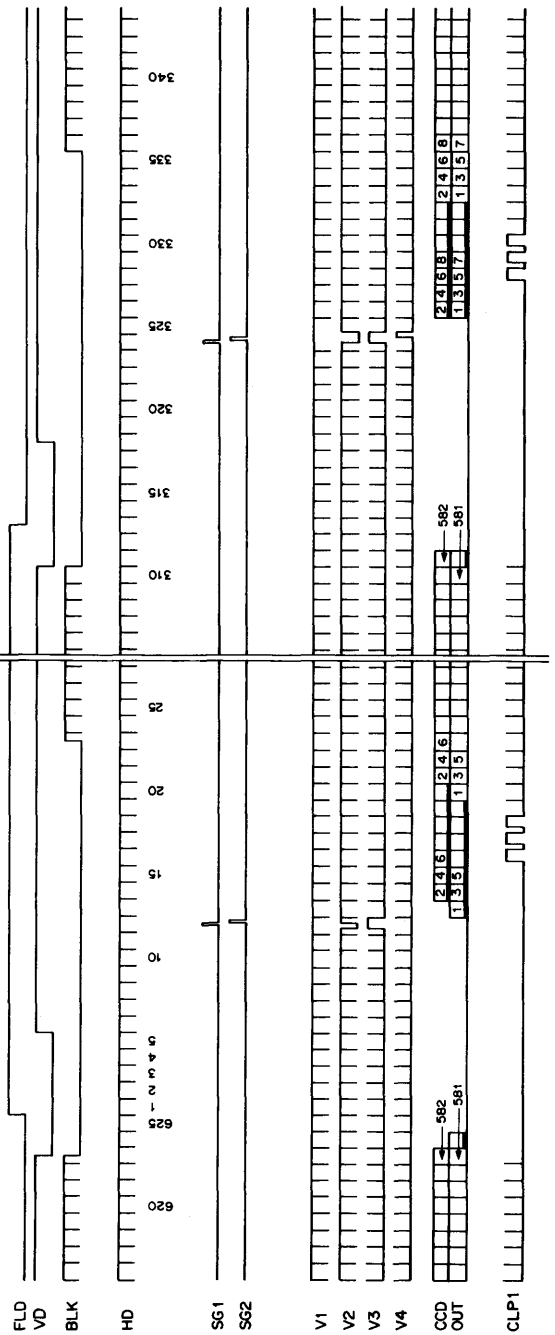
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



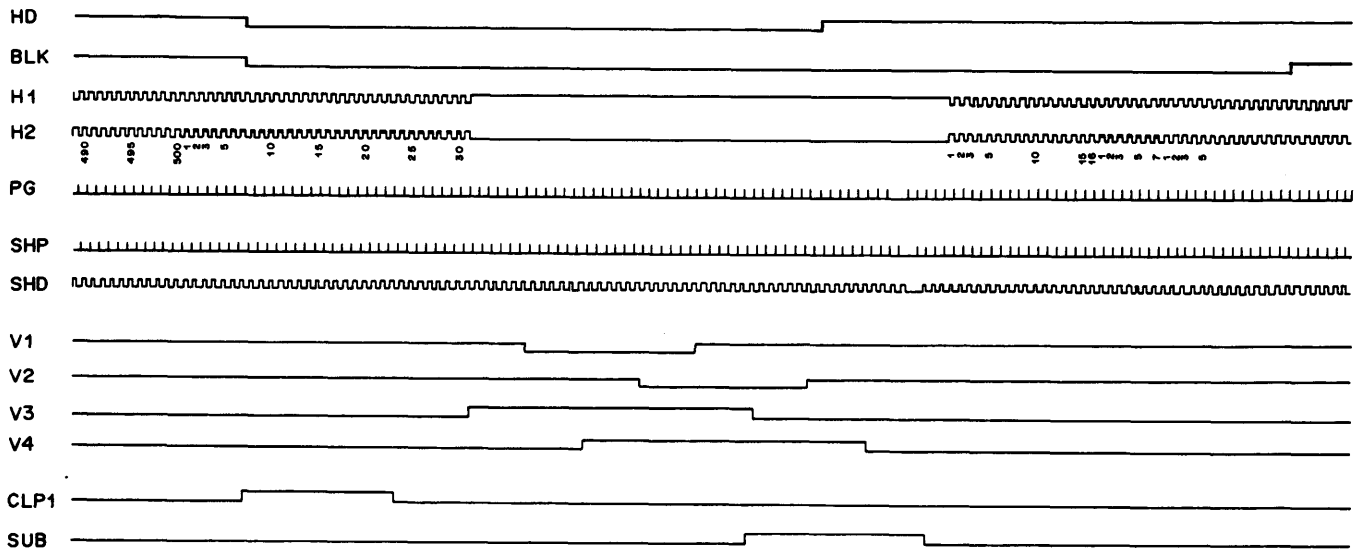
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



During electronic shutter operation

Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

Solid-State Image Sensor for Color Camera

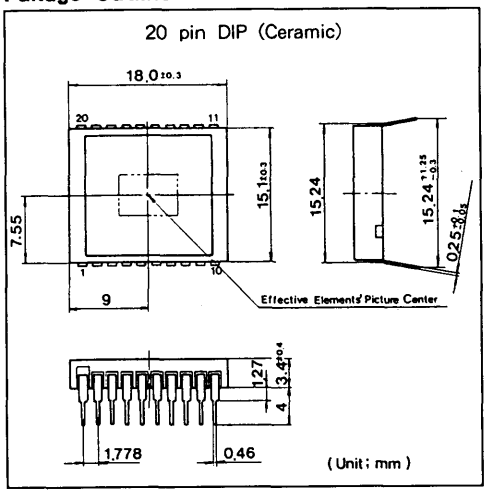
Description

ICX038AK is an interline transfer CCD solid-state imager suitable for NTSC 1/2 inch color video cameras. High sensitiveness is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

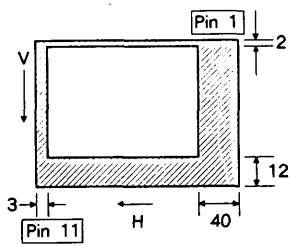
Pakage Outline

Unit : mm



Features

- High image, high sensitivity and low dark current
- Consecutive various speed shutter
  1/60sec.(Typ.), 1/100sec. to 1/10000sec.
- Low smear
- High antiblooming
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive



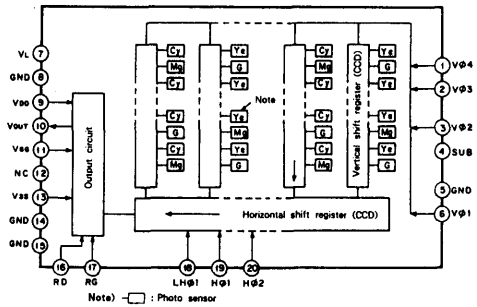
Optical black position (Top View)

Device Structure

- Optical size 1/2 inch format
- Number of effective pixels
  768 (H) × 494 (V) Approx. 380k pixels
- Number of total pixels
  811 (H) × 508 (V) Approx. 410k pixels
- Interline transfer CCD image sensor
- Chip size 7.95mm (H) × 6.45mm (V)
- Unit cell size 8.4 μm (H) × 9.8 μm (V)
- Optical black Horizontal (H) direction Front 3 pixels Rear 40 pixels
  Vertical (V) direction Front 12 pixels Rear 2 pixels
- Number of dummy bits Horizontal 22
  Vertical 1 (even field only)
- Substrate material silicon

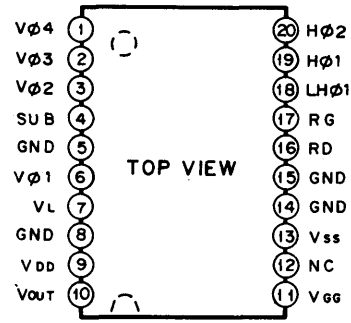
E89442 – ST

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	V ϕ 4	Vertical register transfer clock	11	V_{GG}	Output amplifier gate bias
2	V ϕ 3	Vertical register transfer clock	12	NC	
3	V ϕ 2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	GND	GND
6	V ϕ 1	Vertical register transfer clock	16	RD	Reset drain bias
7	V_L	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	LH ϕ 1	Horizontal register final stage transfer clock
9	V_{DD}	Output amplifier drain supply	19	H ϕ 1	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	H ϕ 2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		− 0.3 to + 55	V	
Supply voltage	V_{DD}, V_{RD}, V_{OUT}, Vss − GND	− 0.3 to + 18	V	
	V_{DD}, V_{RD}, V_{OUT}, Vss − SUB	− 55 to + 10	V	
Clock input voltage	V ϕ 1, V ϕ 2, V ϕ 3, V ϕ 4 − GND	− 15 to + 20	V	
	V ϕ 1, V ϕ 2, V ϕ 3, V ϕ 4 − SUB	to + 10	V	
Voltage difference between vertical clock input pins		to + 15	V	* (Max.)
Voltage difference between horizontal clock input pins		to + 17	V	
H ϕ 1, H ϕ 2 − V ϕ 4		− 17 to + 17	V	
LH ϕ 1, RG, V_{GG} − GND		− 10 to + 15	V	
LH ϕ 1, RG, V_{GG} − SUB		− 55 to + 10	V	
V_L − SUB		− 65 to + 0.3	V	
Beside GND, SUB-V_L		− 0.3 to + 30	V	
Storage temperature		− 30 to + 80	℃	
Operating temperature		− 10 to + 60	℃	

* **Note)** + 27V (Max.) when clock width < 10 μs, duty factor < 0.1 %.

Bias Conditions

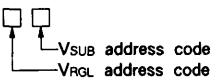
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 390 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0.5		5.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*3				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*** 2)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ±3%.

V_{SUB} code address − 1 digit display
V_{RGL} code address − 1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	0	1	2	3	4	5	6	7	8	9
Numerical value	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

< Example > "5L" → $V_{RGL} = 3.0V$
$V_{SUB} = 12.0V$

*** 3)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* **4)** 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss and SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V φ 1, V φ 2, V φ 3, V φ 4, H φ 1 and H φ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, LH φ 1 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

* **5)** Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

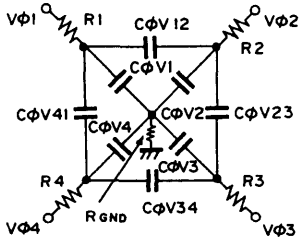
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	− 0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	− 0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	V φ V	8.3	9.0	9.65	V	2	V φ V = V_{VHn} − V_{VLn} (n = 1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.1	V	2	
	$V_{VH3} - V_{VH}$	− 0.25		0.1	V	2	
	$V_{VH4} - V_{VH}$	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V φ H	4.75	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	V_{LHH}	4.45	5.0	5.55	V	4	
	V_{LHL}	− 4.7	− 4.0	− 3.5	V	4	
	V φ LH	8.0	9.0	10.0	V	4	
Reset gate clock voltage	V φ RG	4.5	5.0	5.5	V	5	* 6
	$V_{RGLH} - V_{RGLL}$			0.8	V	5	Low level coupling
Substrate clock voltage	V φ SUB	23.0	24.0	25.0	V	6	

*6) No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

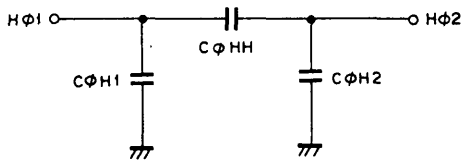
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	−0.2	0	0.2	V	5	
	$V_{\phi RG}$	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1800		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		2200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		450		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		270		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		62		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH}$		8		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		68		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	



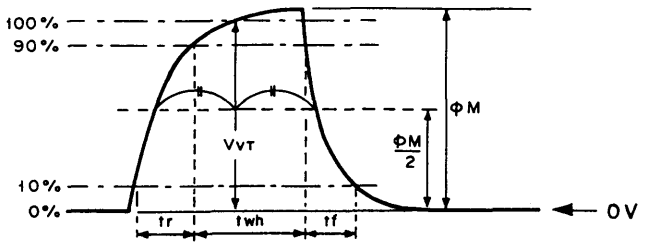
Vertical transfer clock equivalent circuit



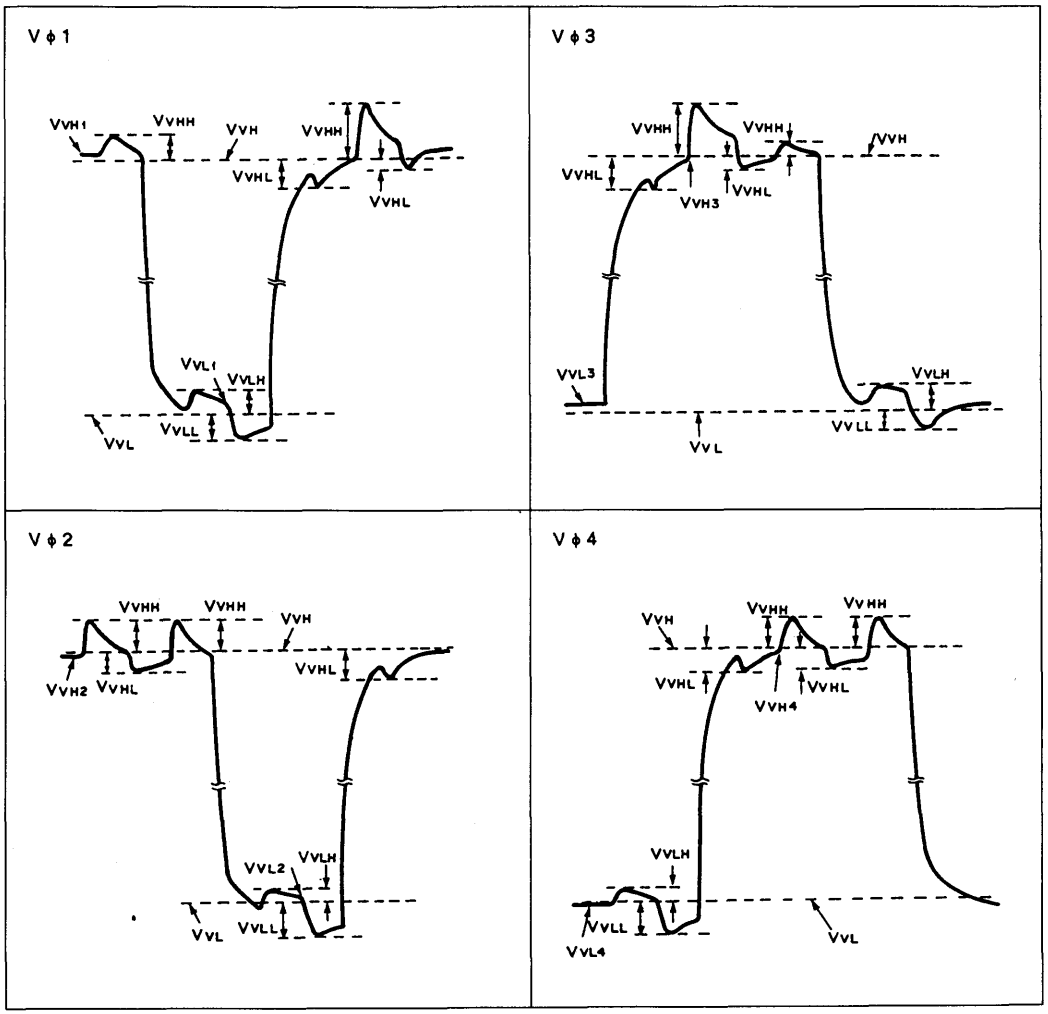
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

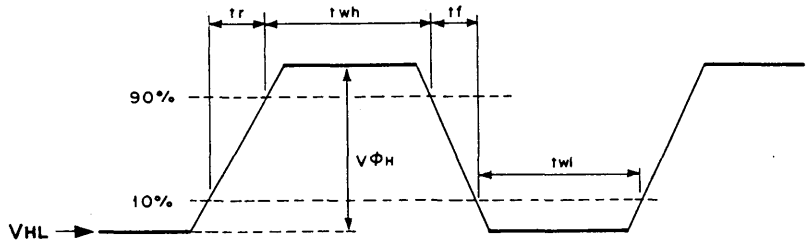
(1) Read out clock waveform



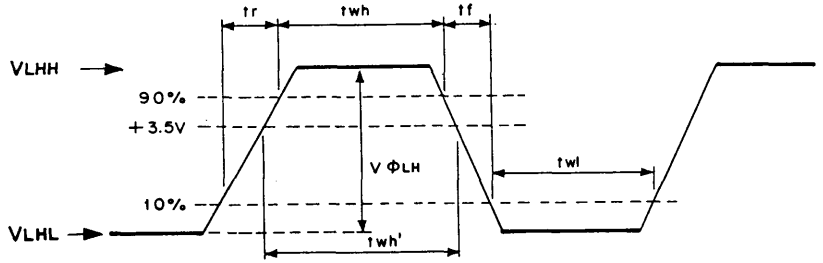
(2) Vertical transfer clock waveform



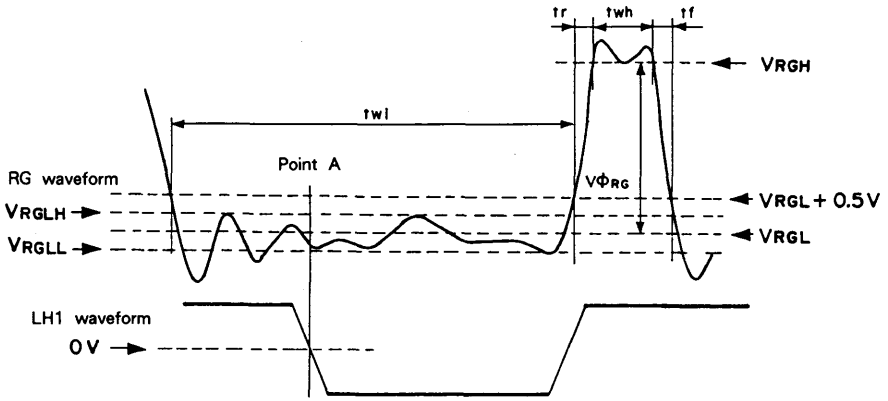
(3) Horizontal transfer clock waveform diagram



(4) Horizontal final stage transfer clock waveform diagram



(5) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

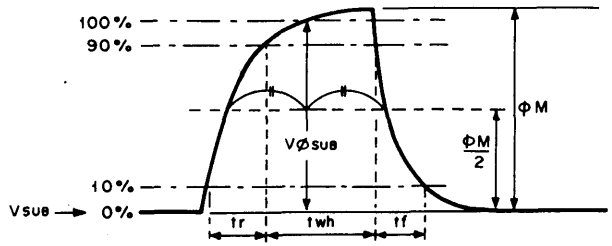
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

V_{RGH} is the minimum value for twh period.

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(6) Substrate clock waveform



Clock switching characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		μs	During read out
Vertical transfer clock	V φ 1, V φ 2, V φ 3, V φ 4										0.015		0.25	μs	* 7
Horizontal transfer clock	H φ		20			20			15	19	*8	15	19	ns	During imaging
Horizontal final stage clock	LH φ		24		22	27			10			9		ns	During imaging
Horizontal transfer /horizontal final stage clock	H φ 1, LH φ		5.38						0.01			0.01		μs	During parallel serial conversion.
Horizontal transfer clock	H φ 2					5.38			0.01			0.01		μs	
Reset gate clock	φ RG	11	13			51			3			3		ns	
Substrate clock	φ SUB	1.5	1.8							0.5			0.5	μs	During charge drain.

* **7)** When vertical transfer clock driver CXD1250 is in use.
* **8)** $tf \geqq tr - 2$ ns

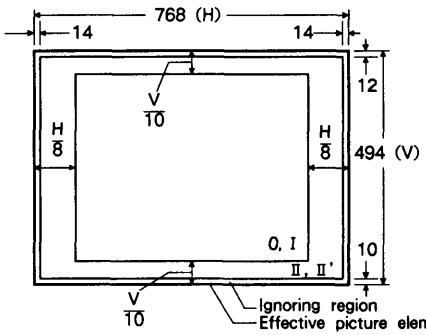
Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H φ	16	20		ns	*9
Horizontal transfer/ horizontal final stage clock	H φ 2, LH φ	15	20		ns	*10

* **9)** "two" is the overlap period of horizontal transfer clocks H φ 1 and H φ 2's twh and twl.
* **10)** "two" is the overlap period of horizontal transfer clock H φ 2's twl and horizontal final stage transfer clock LH φ's twh'

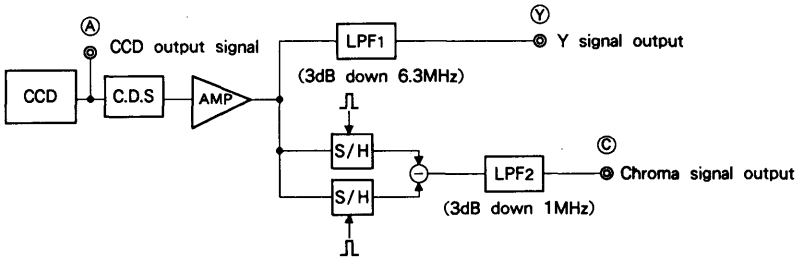
Operating Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	180	220		mV	1	
Saturation signal	Ysat	500			mV	2	Ta = 60°C
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SHy			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Uniformity between signal channels	Δ Sr			10	%	5	
	Δ Sb			10	%	5	
Dark signal	Ydt			2	mV	6	Ta = 60°C
Dark signal shading	Δ Ydt			1	mV	7	Ta = 60°C
Flicker Y	Fy			2	%	8	
Flicker R − Y	Fcr			5	%	8	
Flicker B − Y	Fcb			5	%	8	
Horizontal stripes R	Lcr			3	%	9	
Horizontal stripes G	Lcg			3	%	9	
Horizontal stripes B	Lcb			3	%	9	
Horizontal stripes W	Lcw			3	%	9	
Lag	Lag			0.5	%	10	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

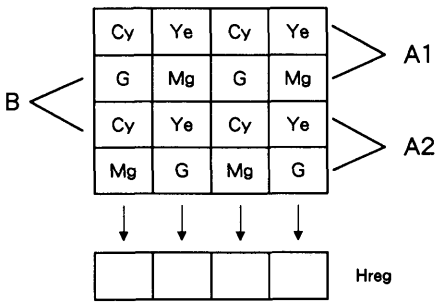
Image Sensor Characteristics Test Method

◎Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the Y signal output or the chroma signal output of the testing system.

◎ Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals



Color Coding Diagram

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The read out line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are [G + Cy], [Mg + Ye], [G + Cy], [Mg + Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows :

$$Y = \{(G + Cy) + (Mg + Ye)\} \times 1/2$$
$$= 1/2\ \{2B + 3G + 2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg + Ye) - (G + Cy)\}$$
$$= \{2R - G\}$$

Next, the signals through H reg. at line A2 are

[Mg + Cy], [G + Ye], [Mg + Cy], [G + Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G + Ye) + (Mg + Cy)\} \times 1/2$$
$$= 1/2\ \{2B + 3G + 2R\}$$
$$-(B - Y) = \{(G + Ye) - (Mg + Cy)\}$$
$$= -\{2B - G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R − Y and − (B − Y) on alternate lines.

It is the same for B field.

◎Definition of standard imaging conditions

① Standard imaging condition I : (As imaging device) Use a pattern box (luminance 706 Nit, color temperature 3200k Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (1.0mmt) as IR cut filter and image at F5.6. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Y signal output average value in this condition is called Y_A.

② Standard imaging condition II : Image a light source (color temperature of 3200k) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (1.0mmt) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of Y signal output average value (Y_A), then test Y signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of Y signal output average value (Y_A). Stop read out clock. When the charge drain executed by the electric shutter at the respective H blankings takes place, test the maximum value Y_{SM} of Y signal output.

   $$S_M = \frac{Y_{SM}}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A) with lens diaphragm at F5.6 to F8. Then test maximum (Ymax) and minimum (Ymin) values of Y signal.

   $$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

5. Video signal between channels uniformity
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then test maximum (Crmax, Cbmax) and minimum (Crmin, Cbmin) values of chroma signals from R − Y and B − Y channels.

   $$\Delta Sr = |(Crmax - Crmin)/Y_A| \times 100\ (\%)$$
   $$\Delta Sb = |(Cbmax - Cbmin)/Y_A| \times 100\ (\%)$$

6. Dark signal
   Test Y signal output average value Ydt when the device ambient temperature is at 60℃ and light is obstructed with horizontal idle transfer level as reference.

7. Dark signal shading
Following 6, test maximum (Ydmax) and minimum (Ydmin) values of dark signal output.

$\Delta Ydt = Ydmax - Ydmin$

8. Flicker
① Fy
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then test the Y signal difference (ΔYf) between even field and odd field.

$Fy = (\Delta Yf / Y_A) \times 100\ (\%)$

② Fcr, Fcb
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then insert R or B filter, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (CAr, CAb).

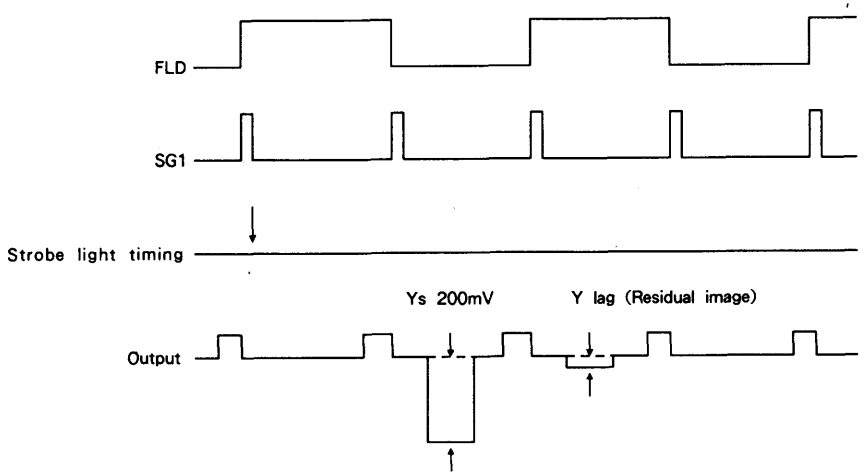
$Fci = (\Delta Ci / CAi) \times 100\ (\%)\ (i = r, b)$

9. Lateral stripe
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then insert R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field.

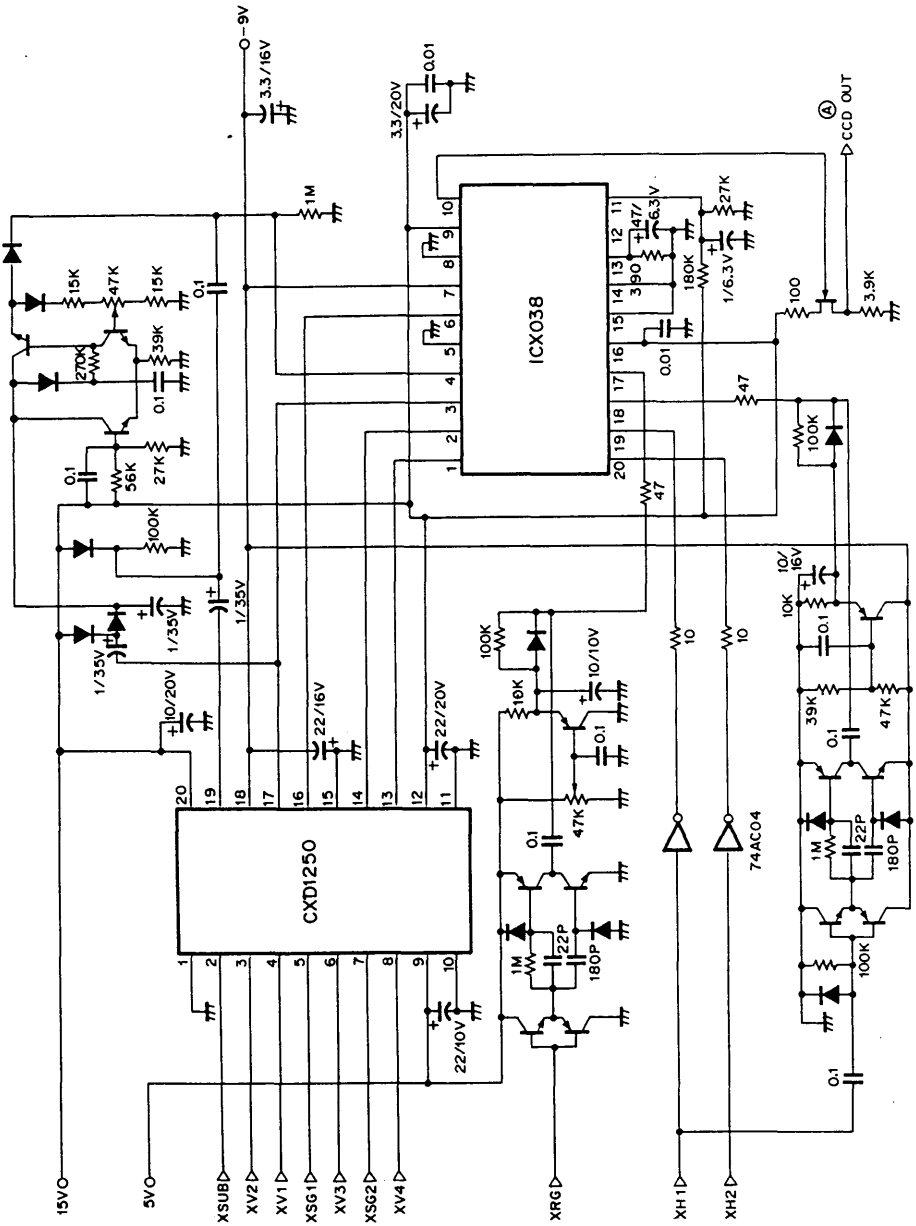
$Lci = (\Delta Yli / Y_A) \times 100\ (\%)\ (i = w, r, g, b)$

10. Residual image
Adjust Y signal output value (Ys) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Ylag).

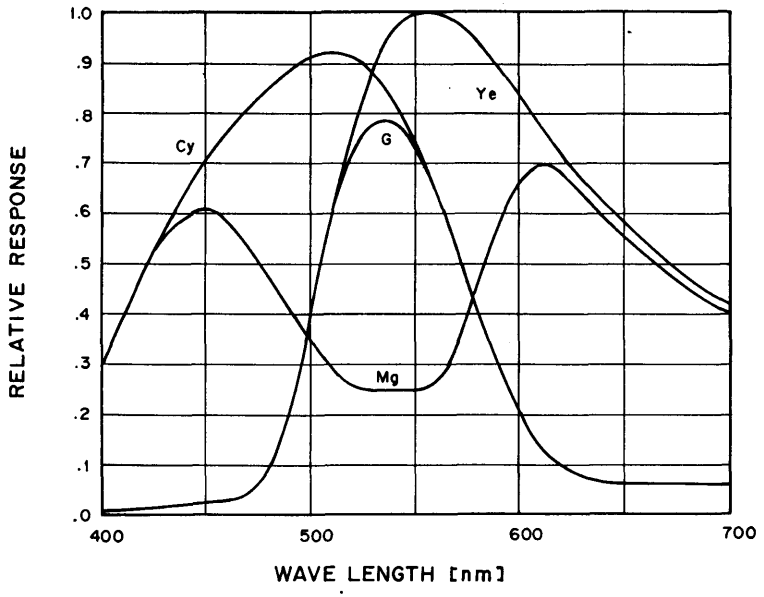
$Lag = (Ylag / Ys) \times 100\ (\%)$



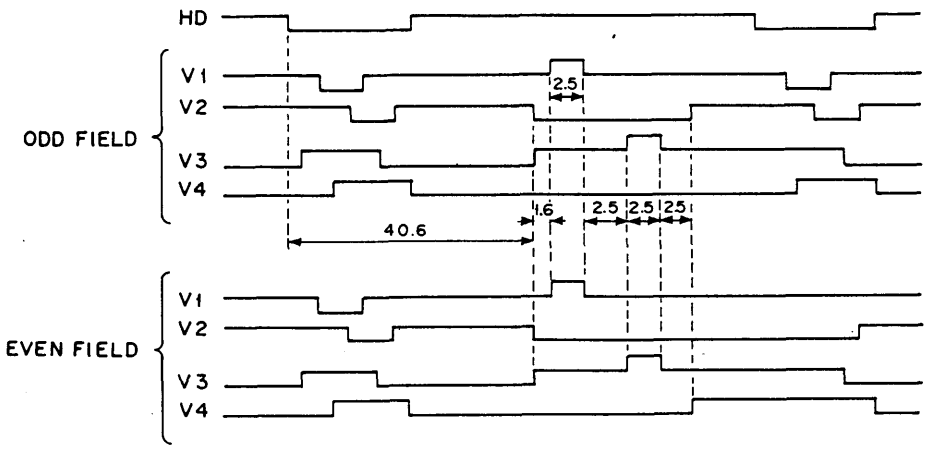
Drive Circuit



Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)

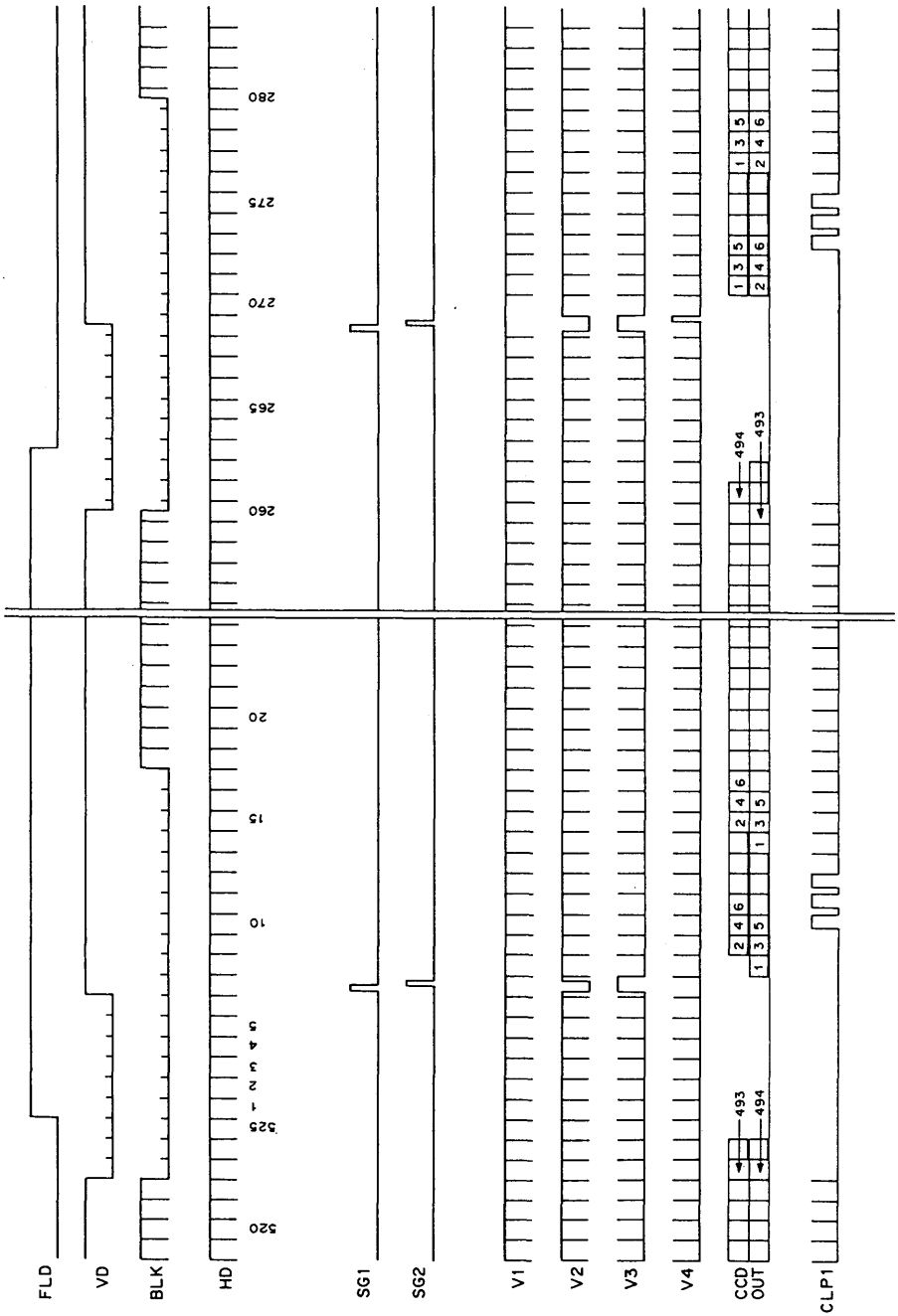


Using read out clock timing chart

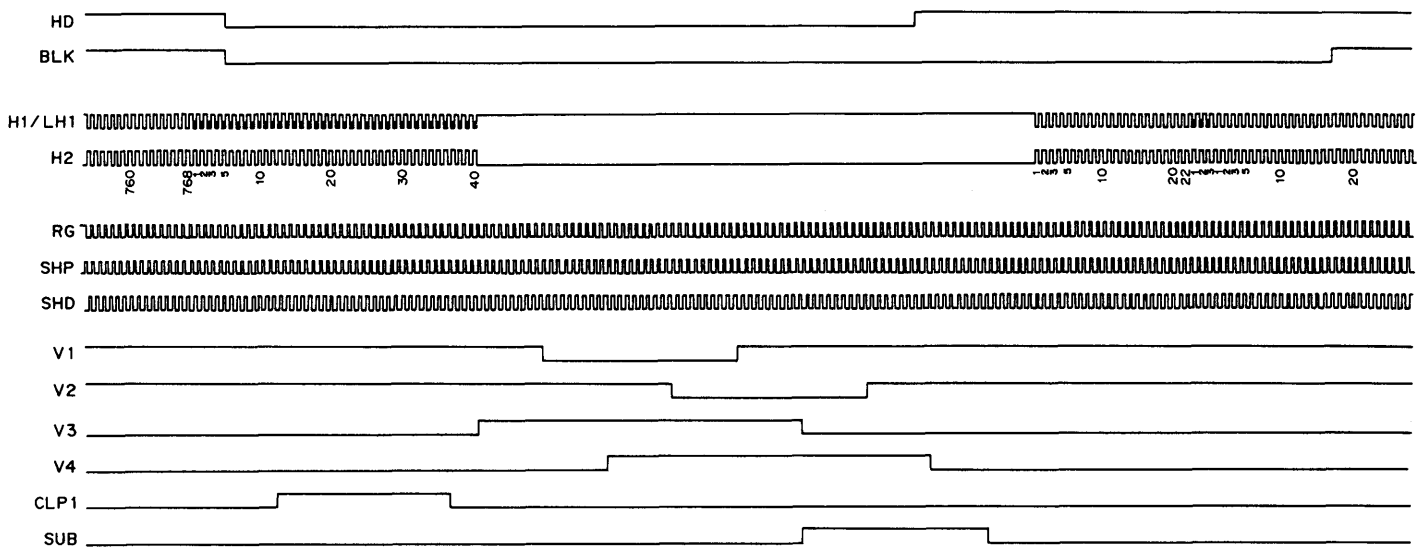


Unit : μs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80℃.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor.
Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect, there is no ROM or serial number.

SONY

ICX039AK

Solid-State Image Sensor for Color Camera

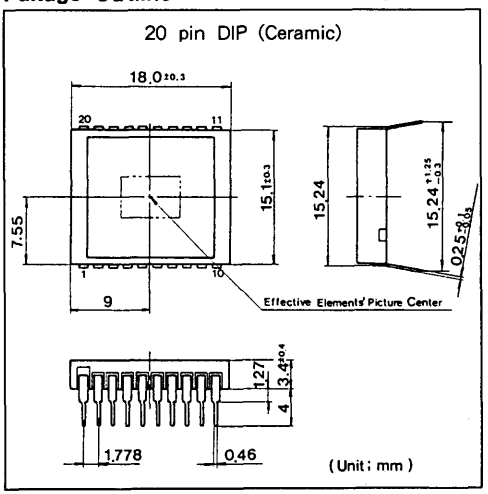
Description

ICX039AK is an interline transfer CCD solid-state imager suitable for PAL 1/2 inch color video cameras. High sensitiveness is achieved through the adoption of Ye, Cy, Mg and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors.

This chip features a field integration read out system and an electronic shutter with variable charge-storage time.

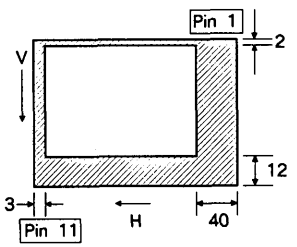
Pakage Outline

Unit : mm



Features

- High image, high sensitivity and low dark current
- Consecutive various speed shutter
  1/50sec.(Typ.), 1/100sec. to 1/10000sec.
- Low smear
- High antiblooming
- Ye, Cy, Mg, G on chip type complementary color mosaic filter.
- Horizontal register 5V drive
- Reset gate 5V drive



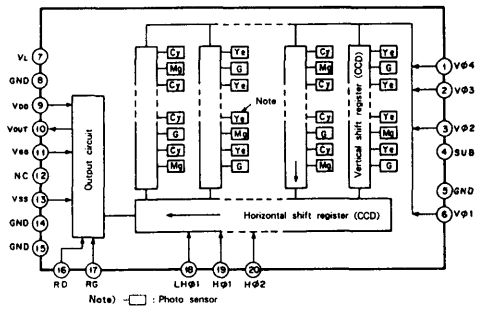
Optical black position (Top View)

Device Structure

- Optical size 1/2 inch format
- Number of effective pixels
  752 (H) × 582 (V) Approx. 440k pixels
- Number of total pixels
  795 (H) × 596 (V) Approx. 470k pixels
- Interline transfer CCD image sensor
- Chip size 7.95mm (H) × 6.45mm (V)
- Unit cell size 8.6 µm (H) × 8.3 µm (V)
- Optical black Horizontal (H) direction Front 3 pixels Rear 40 pixels
  Vertical (V) direction Front 12 pixels Rear 2 pixels
- Number of dummy bits Horizontal 22
  Vertical 1 (even field only)
- Substrate material silicon

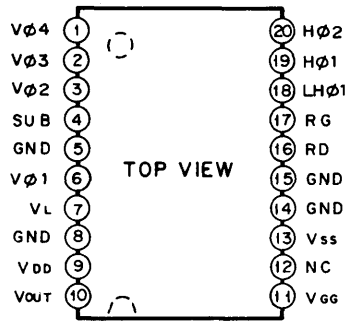
E89445 – ST

Block Diagram



Pin Configuration

(Top View)



Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	V φ 4	Vertical register transfer clock	11	V_{GG}	Output amplifier gate bias
2	V φ 3	Vertical register transfer clock	12	NC	
3	V φ 2	Vertical register transfer clock	13	Vss	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	GND	GND
6	V φ 1	Vertical register transfer clock	16	RD	Reset drain bias
7	V_L	Protective transistor bias	17	RG	Reset gate clock
8	GND	GND	18	LH φ 1	Horizontal register final stage transfer clock
9	V_{DD}	Output amplifier drain supply	19	H φ 1	Horizontal register transfer clock
10	V_{OUT}	Signal output	20	H φ 2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		− 0.3 to + 55	V	
Supply voltage	V_{DD}, V_{RD}, V_{OUT}, Vss − GND	− 0.3 to + 18	V	
	V_{DD}, V_{RD}, V_{OUT}, Vss − SUB	− 55 to + 10	V	
Clock input voltage	V φ 1, V φ 2, V φ 3, V φ 4 − GND	− 15 to + 20	V	
	V φ 1, V φ 2, V φ 3, V φ 4 − SUB	to + 10	V	
Voltage difference between vertical clock input pins		to + 15	V	* (Max.)
Voltage difference between horizontal clock input pins		to + 17	V	
H φ 1, H φ 2 − V φ 4		− 17 to + 17	V	
LH φ 1, RG, V_{GG} − GND		− 10 to + 15	V	
LH φ 1, RG, V_{GG} − SUB		− 55 to + 10	V	
V_L − SUB		− 65 to + 0.3	V	
Beside GND, SUB-V_L		− 0.3 to + 30	V	
Storage temperature		− 30 to + 80	℃	
Operating temperature		− 10 to + 60	℃	

* **Note)** + 27V (Max.) when clock width < 10 μs, duty factor < 0.1 %.

Bias Conditions

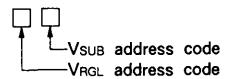
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 390 Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	0.5		5.0	V	*2 *6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*3				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

***2)** Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ±3%.

V_{SUB} code address − 1 digit display
V_{RGL} code address − 1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	0	1	2	3	4	5	6	7	8	9
Numerical value	0.5	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

< Example > "5L" → V_{RGL} = 3.0V
V_{SUB} = 12.0V

***3)** V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

* **4)** 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss and SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V φ 1, V φ 2, V φ 3, V φ 4, H φ 1 and H φ 2, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, LH φ 1 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

* **5)** Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

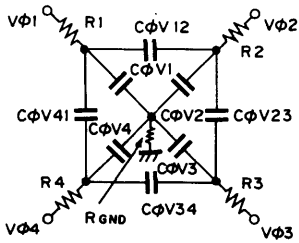
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	− 0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	− 0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	− 9.6	− 9.0	− 8.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	V φ V	8.3	9.0	9.65	V	2	V φ V = $V_{VHn} - V_{VLn}$ (n = 1 to 4)
	$\lvert V_{VH1} - V_{VH2} \rvert$			0.1	V	2	
	$V_{VH3} - V_{VH}$	− 0.25		0.1	V	2	
	$V_{VH4} - V_{VH}$	− 0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V φ H	4.75	5.0	5.25	V	3	
	V_{HL}	− 0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	V_{LHH}	4.45	5.0	5.55	V	4	
	V_{LHL}	− 4.7	− 4.0	− 3.5	V	4	
	V φ LH	8.0	9.0	10.0	V	4	
Reset gate clock voltage	V φ RG	4.5	5.0	5.5	V	5	* 6
	$V_{RGLH} - V_{RGLL}$			0.8	V	5	Low level coupling
Substrate clock voltage	V φ SUB	23.0	24.0	25.0	V	6	

* 6) No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

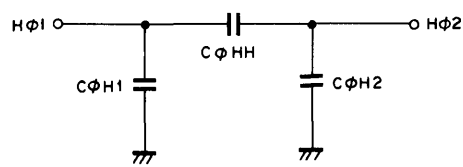
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	−0.2	0	0.2	V	5	
	$V_{\phi RG}$	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1800		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		2200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		450		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		270		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		62		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH}$		8		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		68		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	



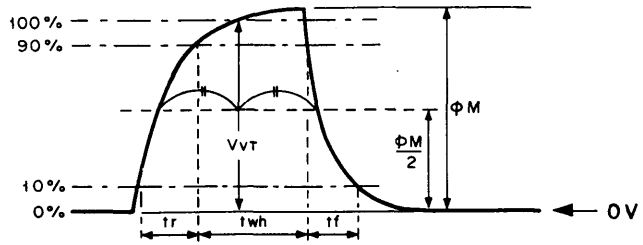
Vertical transfer clock equivalent circuit



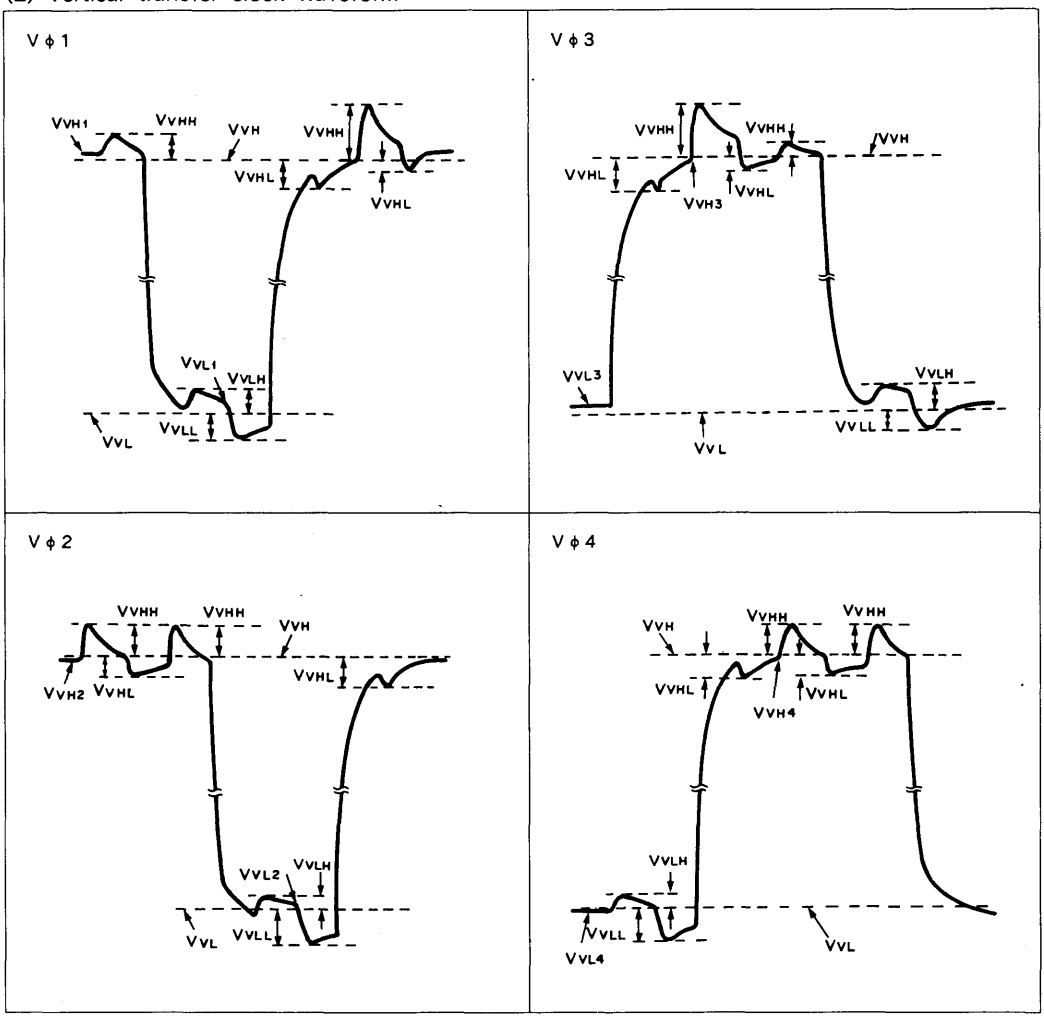
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

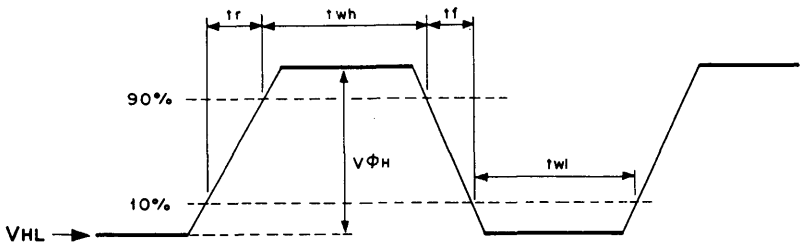
(1) Read out clock waveform



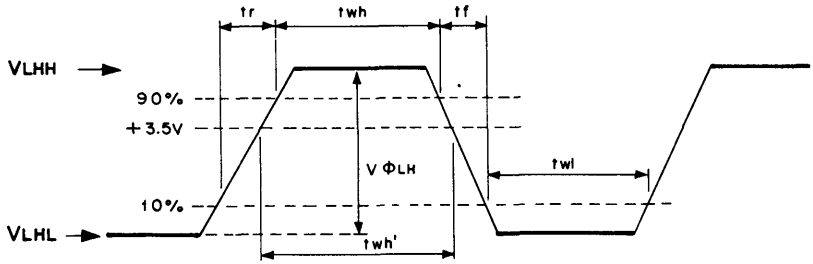
(2) Vertical transfer clock waveform



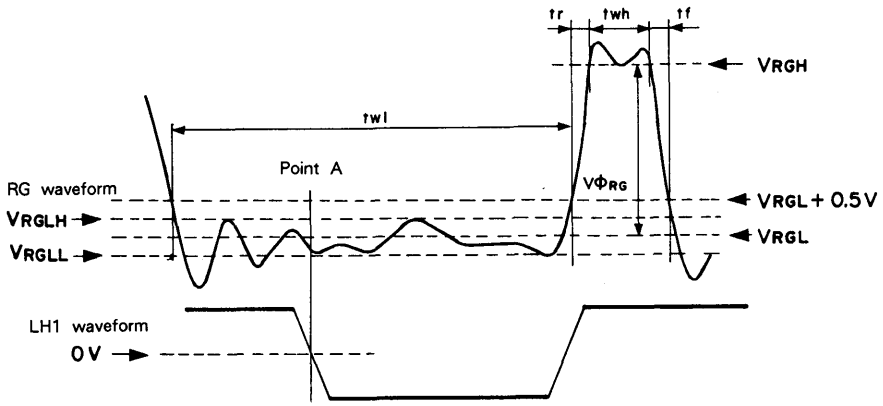
(3) Horizontal transfer clock waveform diagram



(4) Horizontal final stage transfer clock waveform diagram



(5) Reset gate clock waveform diagram



V_{RGLH} is the maximum value and V_{RGLL} the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

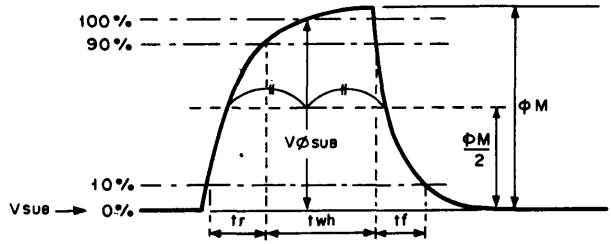
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

V_{RGH} is the minimum value for twh period.

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(6) Substrate clock waveform



Clock switching characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		μs	During read out
Vertical transfer clock	V φ 1, V φ 2, V φ 3, V φ 4										0.015		0.25	μs	* 7
Horizontal transfer clock	H φ		20			20			15	19	*8	15	19	ns	During imaging
Horizontal final stage clock	LH φ		24		22	27			10			9		ns	During imaging
Horizontal transfer /horizontal final stage clock	H φ 1, LH φ		5.38						0.01			0.01		μs	During parallel serial conversion.
Horizontal transfer clock	H φ 2					5.38			0.01			0.01		μs	
Reset gate clock	φ RG	11	13			51			3			3		ns	
Substrate clock	φ SUB	1.5	1.8							0.5			0.5	μs	During charge drain.

* **7)** When vertical transfer clock driver CXD1250 is in use.
* **8)** tf ≧ tr − 2 ns

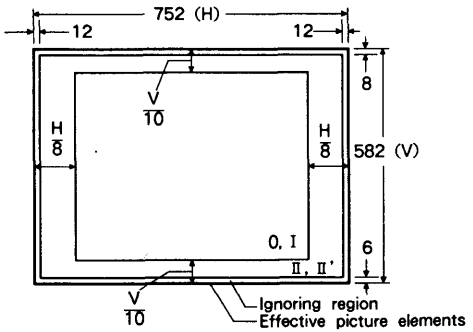
Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H φ	16	20		ns	*9
Horizontal transfer/ horizontal final stage clock	H φ 2, LH φ	15	20		ns	*10

* **9)** "two" is the overlap period of horizontal transfer clocks H φ 1 and H φ 2's twh and twl.
* **10)** "two" is the overlap period of horizontal transfer clock H φ 2's twl and horizontal final stage transfer clock LH φ's twh'

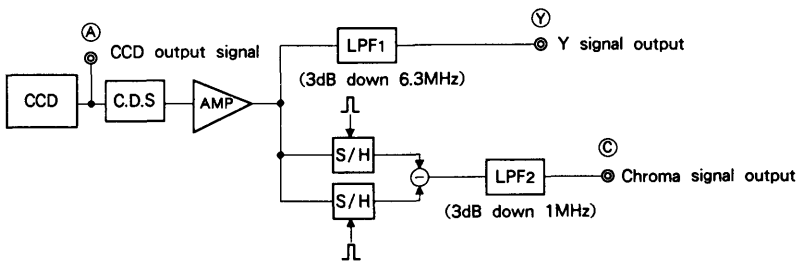
Operating Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	160	200		mV	1	
Saturation signal	Ysat	450			mV	2	Ta = 60°C
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SHy			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Uniformity between signal channels	Δ Sr			10	%	5	
	Δ Sb			10	%	5	
Dark signal	Ydt			2	mV	6	Ta = 60°C
Dark signal shading	Δ Ydt			1	mV	7	Ta = 60°C
Flicker Y	Fy			2	%	8	
Flicker R − Y	Fcr			5	%	8	
Flicker B − Y	Fcb			5	%	8	
Horizontal stripes R	Lcr			3	%	9	
Horizontal stripes G	Lcg			3	%	9	
Horizontal stripes B	Lcb			3	%	9	
Horizontal stripes W	Lcw			3	%	9	
Lag	Lag			0.5	%	10	

Zone chart of Video signal shading



Testing System



Note) Adjust AMP amplifier so that total gains between Ⓐ and Ⓨ and between Ⓐ and Ⓒ equal 1.

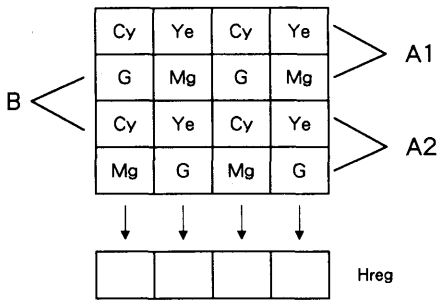
Image Sensor Characteristics Test Method

◎Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference for the signal output which is taken as the Y signal output or the chroma signal output of the testing system.

◎ Color coding of CFA (Color Filter Array) & Composition of luminance (Y) and chrominance (C) signals



Color Coding Diagram

CFA of this image sensor is shown in the Figure. This complementary CFA is used with a "field integration mode", where all of the photosites are read out during each video field. Signals from two vertically adjacent photosites, such as line A1 or A2 for field A, are summed when the image charge is transferred into the vertical storage columns. The read out line pairing is shifted down one line for field B. The sensor output signals through the horizontal register (H reg.) at line A1 are [G + Cy], [Mg + Ye], [G + Cy], [Mg + Ye].

These signals are processed in order to compose Y and C signals. By adding the two adjacent signals at line A1, Y signal is formed as follows :

$$Y = \{(G + Cy) + (Mg + Ye)\} \times 1/2$$
$$= 1/2\ \{2B + 3G + 2R\}$$

C signal is composed by subtracting the two adjacent signals at line A1.

$$R - Y = \{(Mg + Ye) - (G + Cy)\}$$
$$= \{2R - G\}$$

Next, the signals through H reg. at line A2 are

[Mg + Cy], [G + Ye], [Mg + Cy], [G + Ye]

Similarly, Y and C signals are composed at line A2.

$$Y = \{(G + Ye) + (Mg + Cy)\} \times 1/2$$
$$= 1/2\ \{2B + 3G + 2R\}$$
$$-(B - Y) = \{(G + Ye) - (Mg + Cy)\}$$
$$= -\{2B - G\}$$

Accordingly, Y signal is balanced in relation to the scanning lines, and C signal takes the form of R − Y and − (B − Y) on alternate lines.

It is the same for B field.

◎Definition of standard imaging conditions

① Standard imaging condition I : (As imaging device) Use a pattern box (luminance 706 Nit, color temperature 3200k Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (1.0mmt) as IR cut filter and image at F5.6. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Y signal output average value in this condition is called Y_A.

② Standard imaging condition II : Image a light source (color temperature of 3200k) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (1.0mmt) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I and measure Y signal (S) at the center of the screen.

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of Y signal output average value (Y_A), then test Y signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of Y signal output average value (Y_A). Stop read out clock. When the charge drain executed by the electric shutter at the respective H blankings takes place, test the maximum value Y_{SM} of Y signal output.

   $$S_M = \frac{Y_{SM}}{Y_A} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A) with lens diaphragm at F5.6 to F8. Then test maximum (Ymax) and minimum (Ymin) values of Y signal.

   $$SHy = (Ymax - Ymin)/Y_A \times 100\ (\%)$$

5. Video signal between channels uniformity
   Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then test maximum (Crmax, Cbmax) and minimum (Crmin, Cbmin) values of chroma signals from R − Y and B − Y channels.

   $$\Delta Sr = |(Crmax - Crmin)/Y_A| \times 100\ (\%)$$
   $$\Delta Sb = |(Cbmax - Cbmin)/Y_A| \times 100\ (\%)$$

6. Dark signal
   Test Y signal output average value Ydt when the device ambient temperature is at 60℃ and light is obstructed with horizontal idle transfer level as reference.

7. Dark signal shading
Following 6, test maximum (Ydmax) and minimum (Ydmin) values of dark signal output.

$\Delta Ydt = Ydmax - Ydmin$

8. Flicker
① Fy
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then test the Y signal difference (ΔYf) between even field and odd field.

$Fy = (\Delta Yf / Y_A) \times 100\ (\%)$

② Fcr, Fcb
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then insert R or B filter, and test the C signal difference (ΔCr, ΔCb) between even field and odd field and the C signal output average value (CAr, CAb).

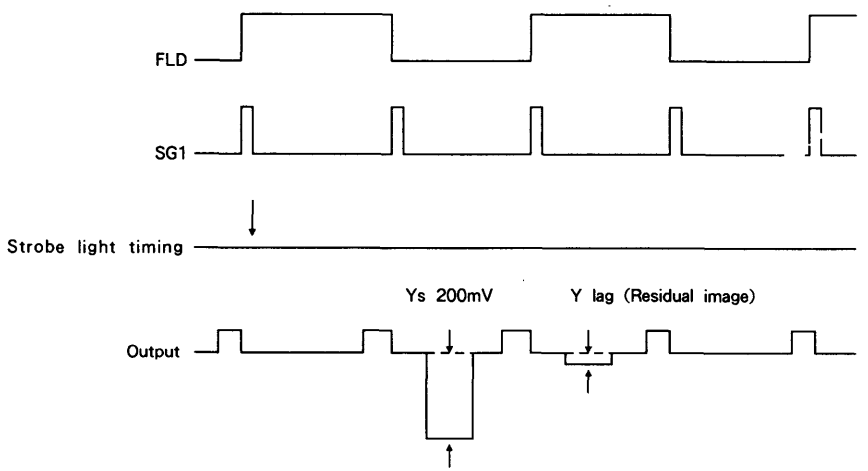
$Fci = (\Delta Ci / CAi) \times 100\ (\%)\ (i = r, b)$

9. Lateral stripe
Set to standard imaging condition II. Adjust light intensity to Y signal output average value (Y_A). Then insert R, G and B filters respectively, and test the signal difference (ΔYlw, ΔYlr, ΔYlg, ΔYlb) between Y signal lines of the same field.

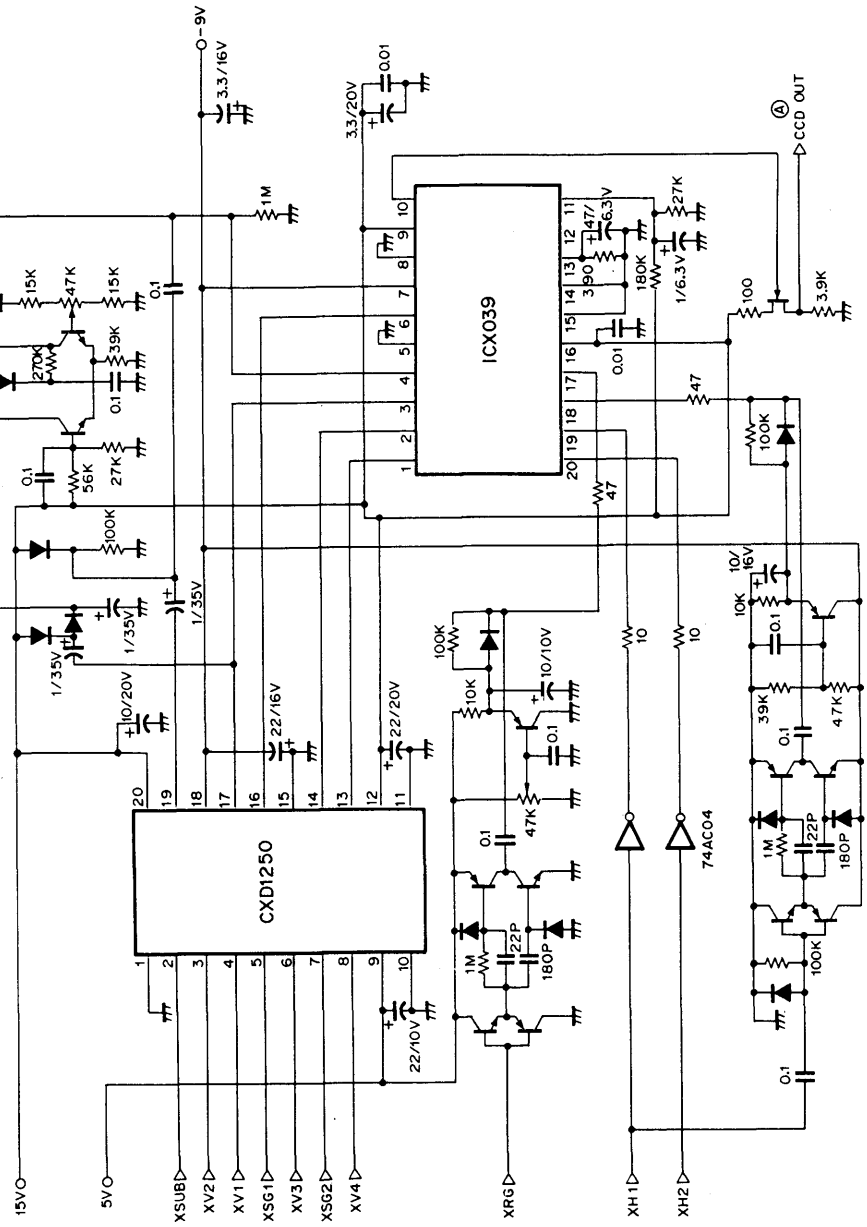
$Lci = (\Delta Yli / Y_A) \times 100\ (\%)\ (i = w, r, g, b)$

10. Residual image
Adjust Y signal output value (Ys) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Ylag).

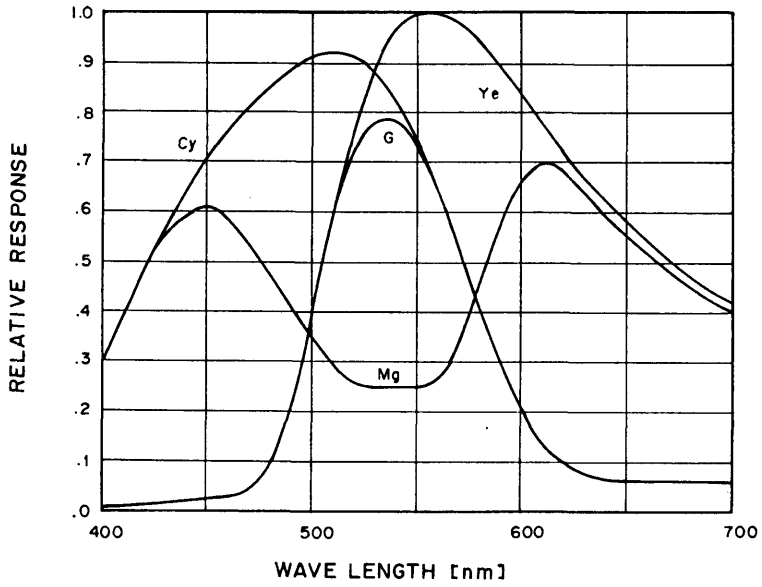
$Lag = (Ylag / Ys) \times 100\ (\%)$



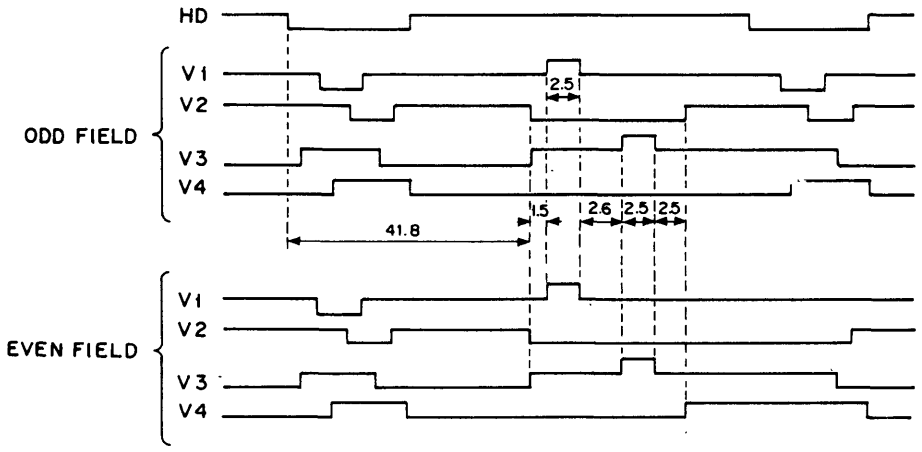
Drive Circuit



Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)

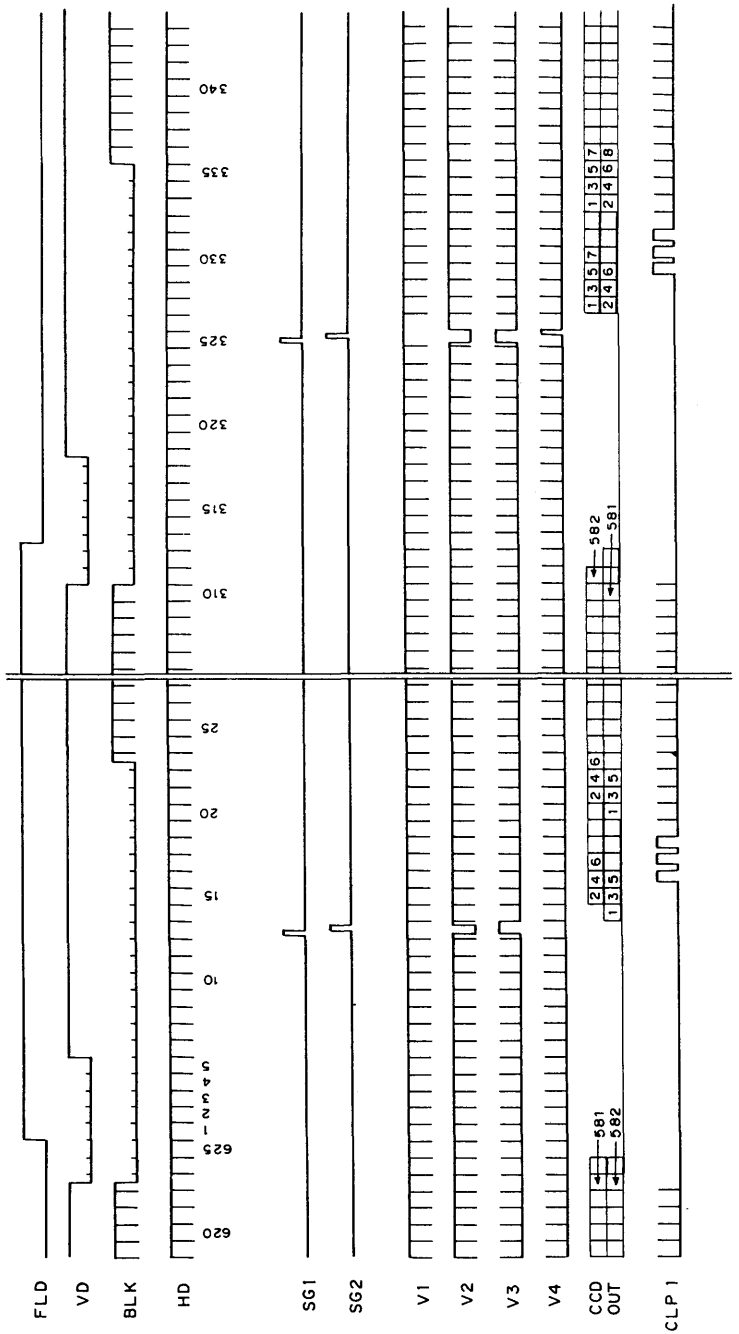


Using read out clock timing chart

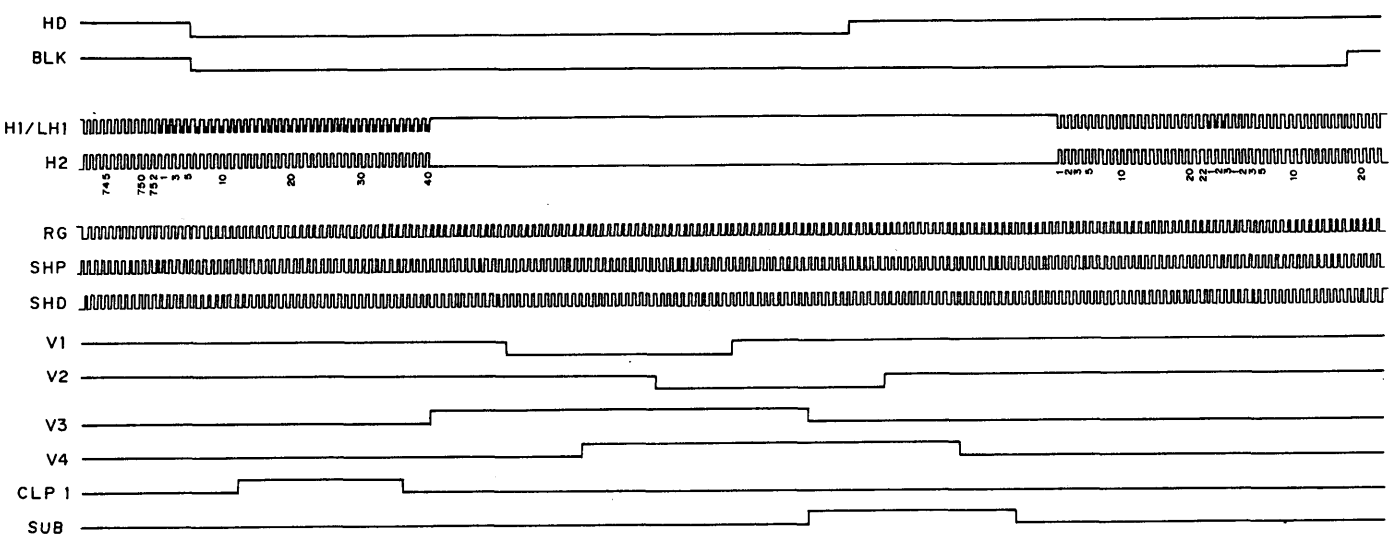


Unit : μs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80℃.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

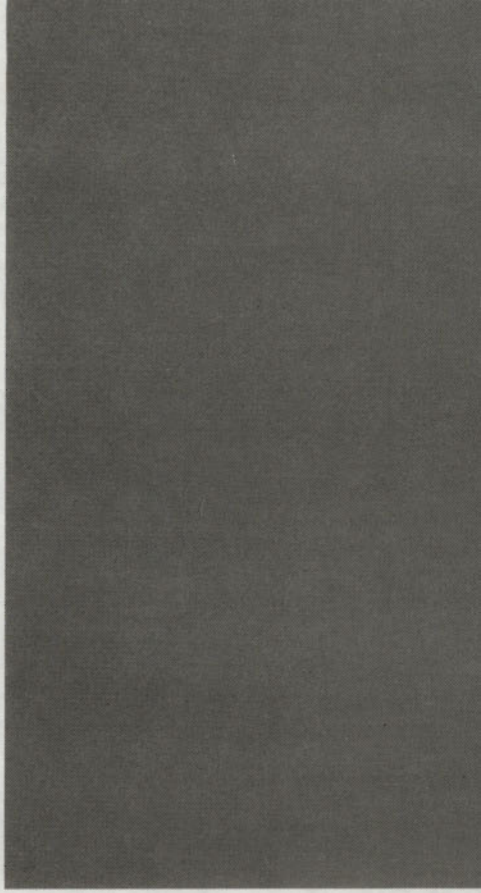
3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored.

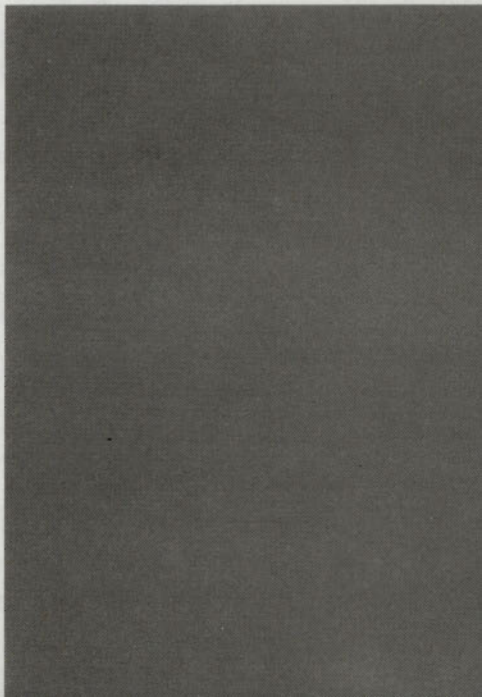
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
This is shipped in its own case in pair with the CCD image sensor.
Pair with the CCD image sensor bearing the same serial number during mounting. When the CCD image sensor has no defect, there is no ROM or serial number.



CCD Imager System



3) CCD Imager System

Type	Application	Function	Page
IS018CL	CCD imager system kit for B/W camera	ICX018CL and three peripheral hybrid ICs, for EIA	297
IS021CL		ICX018CL and three peripheral hybrid ICs, for CCIR	
IS026BK	CCD imager system kit for color camera	ICX018CL and five peripheral hybrid ICs, for NTSC	301
IS027BK		ICX018CL and five peripheral hybrid ICs, for PAL	

SONY

IS018CL/IS021CL

B/W CCD Imager System

Description

This new B/W imager system consists of a CCD imager IC with peripheral hybrid ICs, and makes possible the realization of very compact B/W CCD cameras.

CCD imager
- ICX018CL: for EIA (510H × 492V)
- ICX021CL: for CCIR (500H × 582V)

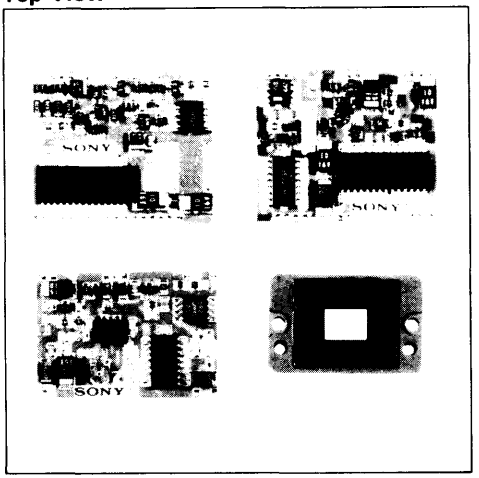
Hybrid IC's
- BX-1430: for CCD drive and timing (EIA)
- BX-1431: for CCD drive and timing (CCIR)
- BX-1432: for signal processing (EIA)
- BX-1432A: for signal processing (CCIR)
- BX-1433: for Gen Lock (EIA)
- BX-1433A: for Gen Lock (CCIR)

Features

CCD imager
- High sensitivity
- Gamma characteristic $\gamma = 1$
- Low lag, no burning
- Low smear
  P-sub, P-well structure
- Anti-blooming

Hybrid ICs
- No adjustment require
- Gamma correction ON/OFF (0.45/1)
- AGC ON/OFF
- UL approved

Top View



See page 4

System Combination

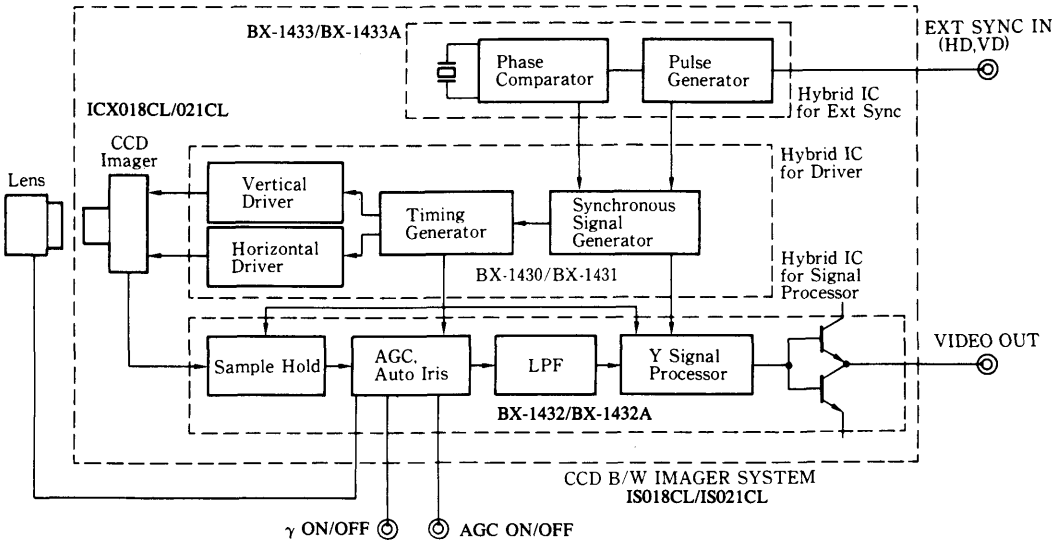
Type Name	System Combination
IS018CL-1	ICX018CL + BX-1430 + BX-1432 + BX-1433
2	ICX018CL + BX-1430 + BX-1432
3	ICX018CL + BX-1430 + BX-1433
4	ICX018CL + BX-1430
IS021CL-1	ICX021CL + BX-1431 + BX-1432A + BX-1433A
2	ICX021CL + BX-1431 + BX-1432A
3	ICX021CL + BX-1431 + BX-1433A
4	ICX021CL + BX-1431

Absolute Maximum Ratings (Ta = 25°C)

Item	Hybrid IC's		CCD imager	
Supply voltage	BX-1430/1431 V_{CC1} 20 V V_{CC2} 16 V V_{CC3} 10 V BX-1432/1432A V_{CC1} 15 V V_{CC2} 15 V BX-1433/1433A V_{CC1} 12 V V_{CC2} 6.5 V		V_{DD1} V_{DD2} −0.3 to 30 V V_{PD}	
Allowable power dissipation	BX-1430/1431 850 mW BX-1432/1432A 870 mW BX-1433/1433A 350 mW			
Operating temperature	−10 to +60	°C	−10 to +55	°C
Storage temperature	−30 to +85	°C	−30 to +80	°C

60707B-TO

Block Diagram



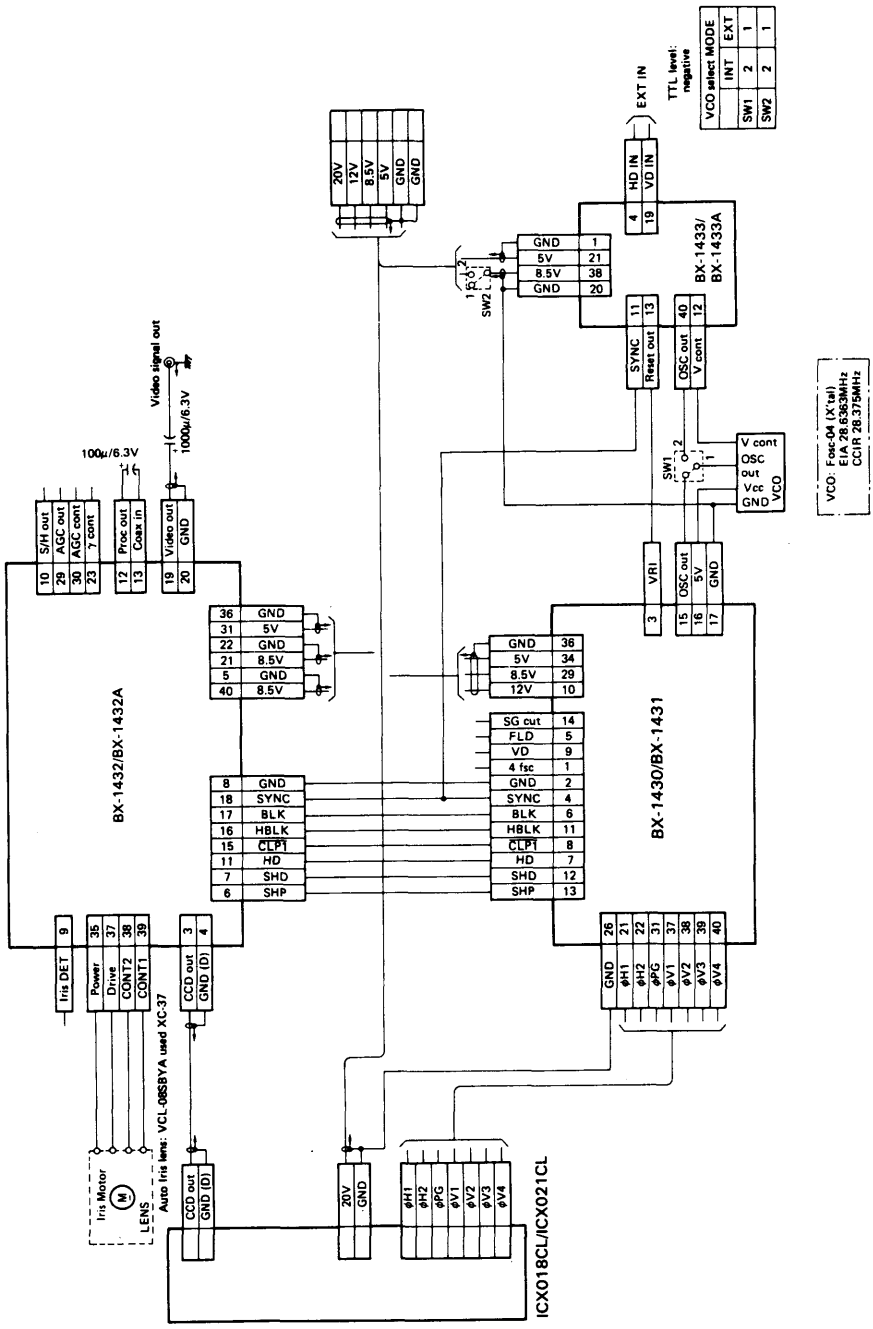
Operating Characteristics

Evaluation Board

Item	EIA specification	CCIR specification
Scanning system	525 lines 30 frame/sec.	625 lines 25 frame/sec.
	2 : 1 interlace	
Video signal	1.0 Vp-p, 75 Ω, negative sync	
Horizontal resolution	350 TV lines	
S/N ratio	More than 50 dB (with AGC off, γ off)	
Power dissipation	1.6W (without auto iris)	
Sync system*	Internal/External (external using BX-1433A, external input pulses HD, VD)	

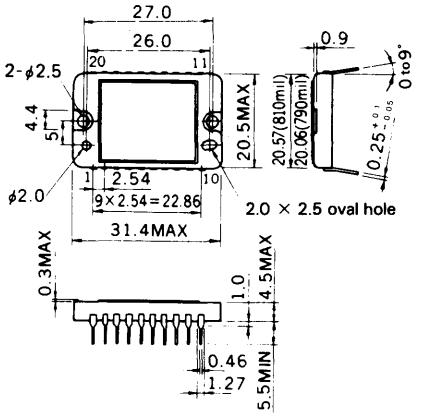
*Note) Recommended external VCO sync signal : quasi-sinusoidal output
FOSC-04 manufactured by FUJI SANGYO CO.

Block Diagram

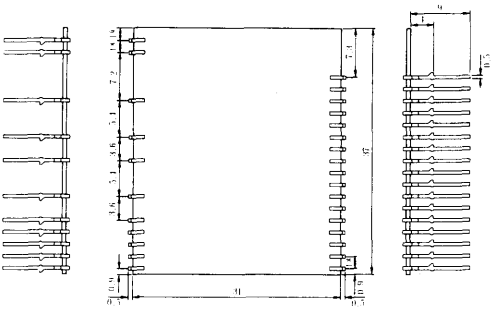


Package Outline

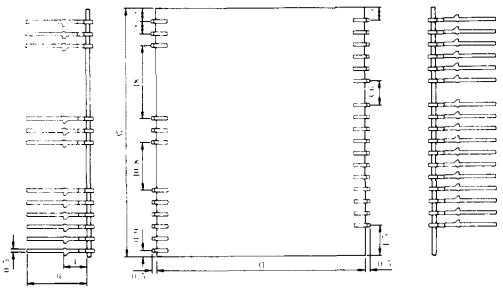
Unit: mm



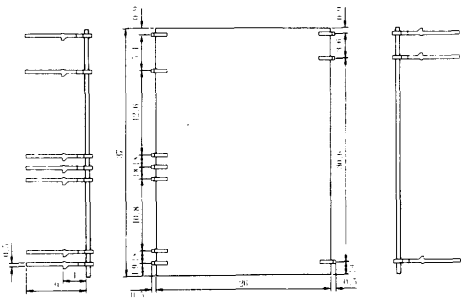
ICX018CL/ICX021CL



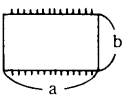
BX-1430/BX-1431



BX-1432



BX-1433



	a	b	c	d
1430/31	37.0	31.2	3.5	7.0
1432/A	37.0	31.0	3.5	7.0
1433/A	37.0	26.0	3.5	7.0

Allowable tolerance: 0.3 mm
BX-1430/BX-1431
BX-1432/BX-1432A
BX-1433/BX-1433A

SONY ISO26BK/ISO27BK

CCD Color Imager System

Description

This new color imager system made up of a CCD imager and peripheral hybrid IC's realizes very compact CCD color cameras.
Improvement in sensitivity characteristic has been realized through the adoption of ICX 026 BK/027 BK.
The system is available whereas independent hybrid IC's are not.

- CCD imagers
  ICX026BK (NTSC)
  ICX027BK(PAL)

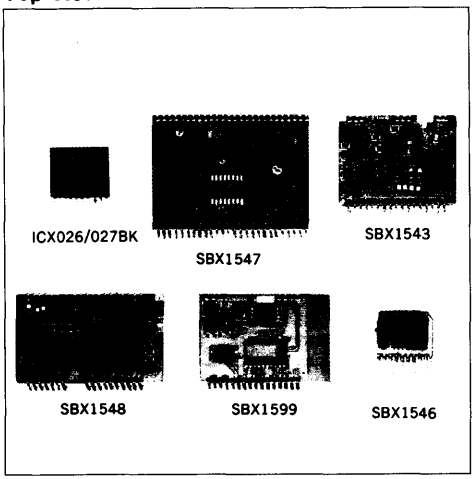
- Hybrid IC's

NTSC	SBX1547-01	Drive and AGC circuit
	SBX1543-01	Matrix circuit
	SBX1548-01	Encoder
	SBX1599-01	VBS gen-lock
	SBX1546-01	AWB circuit
PAL	SBX1547-21	Drive and AGC circuit
	SBX1543-01	Matrix circuit
	SBX1548-21	Encoder
	SBX1599-21	VBS gen-lock
	SBX1546-01	AWB circuit

Features

- CCD imager
  High sensitivity (Low dark current)
  High resolution
  Variable speed electronic shutter function
  N-sub, P-well structure
- Hybrid IC's
  No adjustment required: Function trimming used
  Highly compact mounting: Small size IC package used
  UL approved
- System kit
  Peripherals greatly reduced
  Gen lock for color framing adaptable
  Color difference signals, Y/C separated signals output
  AGC ON/OFF possible

Top View



Imager system		System structure
NTSC	ISO26BK-30F	ICX026BK-3 +SBX1547-01
	ISO26BK-30G	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01
	ISO26BK-30J	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01 +SBX1599-01
	ISO26BK-30H	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01 +SBX1546-01
	ISO26BK-30K	ICX026BK-3 +SBX1547-01 +SBX1543-01 +SBX1548-01 +SBX1599-01 +SBX1546-01
PAL	ISO27BK-30F	ICX027BK-3 +SBX1547-21
	ISO27BK-30G	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21
	ISO27BK-30J	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21 +SBX1599-21
	ISO27BK-30H	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21 +SBX1546-01
	ISO27BK-30K	ICX027BK-3 +SBX1547-21 +SBX1543-01 +SBX1548-21 +SBX1599-21 +SBX1546-01

E89420-HP

Systems

Absolute maximum ratings (Ta=25°C)

Item	Hybrid ICs					CCD Imager	
	SBX1547	SBX1543	SBX1548	SBX1599	SBX1546		
Supply voltage	V_{CC1} 6.3V	V_{CC1} 6V	V_{CC1} 6.3V	V_{CC1} 6.3V	V_{CC1} 7V	V_{DD1}	
	V_{CC2} 20V			V_{CC2} 12V		V_{DD2}	20V
	V_{CC3} 25V					V_{PD}	
	V_{CC4} −16V					V_{SS}	
						V_{SUB}	55V
Operating temperature	−10 to +60°C						
Storage temperature	−30 to +80°C						

Hybrid ICs recommended operating conditions

SBX1547		SBX1543		SBX1548		SBX1599		SBX1546	
Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)	Supply voltage (V)	Current consumption (mA)
V_{CC1} 5±0.25V	105(Typ.)	V_{CC1} 5±0.25V	100(Typ.)	V_{CC1} 5±0.25V	95(Typ.)	V_{CC1} 5±0.25V	20(Typ.)	V_{CC1} 5±0.25V	2.5(Typ.)
V_{CC2} 15±0.45V	12(Typ.)					V_{CC2} 8.5±0.5V	15(Typ.)		
V_{CC3} 22±1.5V	0.5(Typ.)								
V_{CC4} −9.5±0.5V	2(Typ.)								

System Operating Characteristics

Evaluation board

	NTSC Specifications	PAL Specifications
Scanning system	525Lines 30frame/sec.	625Lines 25frame/sec.
	2 : 1 Interlace	
Video signal	1.0Vp-p, 75Ω, Negative sync signal	
Horizontal resolution	330TV Lines	
S/N ratio	More than 43dB (AGC off, γon)	
Power consumption	1.8W (Without AWB, Gen-lock)	
Sync system	Internal/External selection possible. (composite video signal input to hybrid IC for external sync use)	

Electrical characteristics 1 (Ta=25°C)

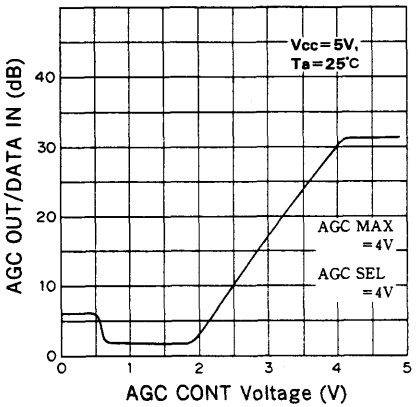
Item			Symbol	Test condition	Min.	Typ.	Max.	Unit
A to E system	Vertical transfer clock $\phi V1$, $\phi V3$	H level	V_T		13	15	17	V
		M level	V_{VM}		−0.5	0	0.7	
		Amplitude	$V_{\phi V}$		8		11	
	Vertical transfer clock $\phi V2$, $\phi V4$	H level	V_{VM}		−0.5	0	0.7	V
		Amplitude	$V_{\phi V}$		8		11	
	Horizontal transfer clock $\phi H1$, $\phi H2$	L level	V_{HL}				0.5	V
		Amplitude	$V_{\phi H}$		4.5	5	5.5	
	Precharge clock ϕPG	L level	V_{PGL}				0.5	V
		Amplitude	$V_{\phi PG}$		9		12	
	Substrate clock ϕSUB	Amplitude	$V_{\phi SUB}$		30		35	V
	Color separation output	S_1, S_2, Y output	Vf	Input data 150mVp-p		500		mVp-p
		DC output	V_{fDC}	DC bias	1.8	1.9	2.0	V
	IRIS output	IRIS output	V_{IR}			285		mVp-p
		DC output	V_{IRDC}	DC bias	1.8	1.9	2.0	V

Electrical characteristics 2 (Ta=25°C)

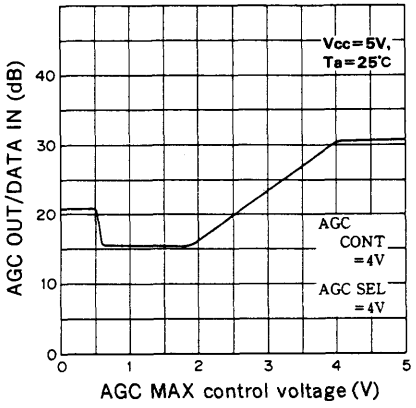
Item				Symbol	Test condition	Min.	Typ.	Max.	Unit
B to E System	R, G, B, output	NTSC	R	V_{RNT}	Standard Imaging Condition, Application system circuit	340	400	460	mV
			G	V_{GNT}	Standard Imaging Condition, Application system circuit	450	520	590	
			B	V_{BNT}	Standard Imaging Condition, Application system circuit	210	260	310	
		PAL	R	V_{RPA}	Standard Imaging Condition, Application system circuit	310	370	430	mV
			G	V_{GPA}	Standard Imaging Condition, Application system circuit	480	550	620	
			B	V_{BPA}	Standard Imaging Condition, Application system circuit	240	290	340	
		DC		V_{CLDC}	DC bias	1.7	1.9	2.0	V
	WB Control	Cont32		V_{C32}	Typ. (3200°k) DC bias		1.0		V
	Set up level			V_{set}			20	50	mV
	Sync level	NTSC		V_{SYNT}		250	285	320	mV
		PAL		V_{SYPA}		270	300	330	
	Burst level	NTSC		V_{BUNT}		250	285	320	mV
		PAL		V_{BUPA}		270	300	330	

* Definition of Standard Imaging condition
A pattern box (luminance 706 Nit, Color temperature 3200°K, with halogen lamp) is imaged using a test standard lens, F5.6 contraction, at that time there is no pattern and CM-500S 1.0mmt is utilized as I.R cut filter.

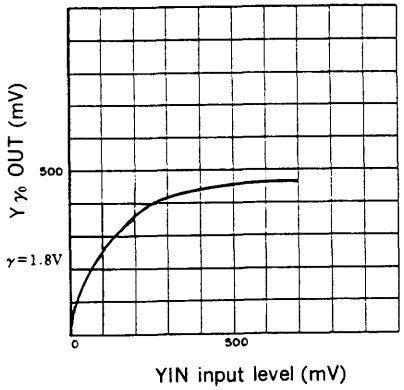
AGC Amp gain control characteristics
(SBX1547)



AGC Amp Max. gain control characteristics
(SBX1547)

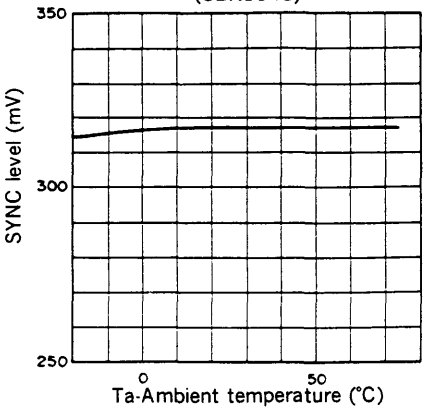


Yγ characteristics
(SBX1543)



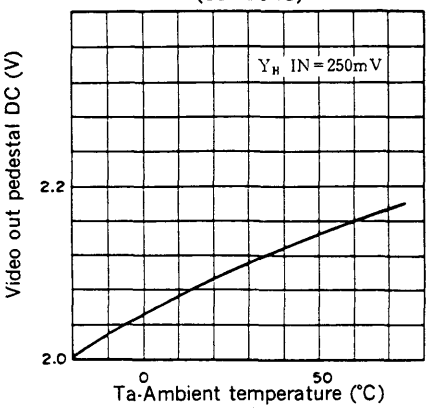
SYNC level temperature characteristics

(SBX1548)



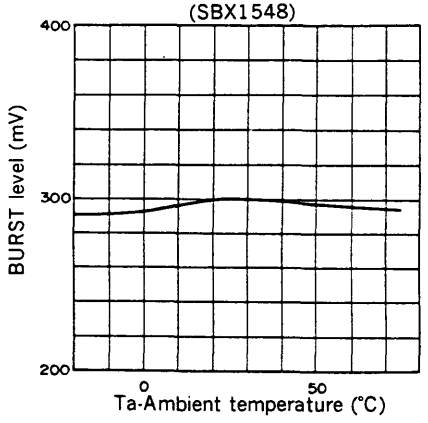
VIDEO OUT pin pedestal DC

(SBX1548)



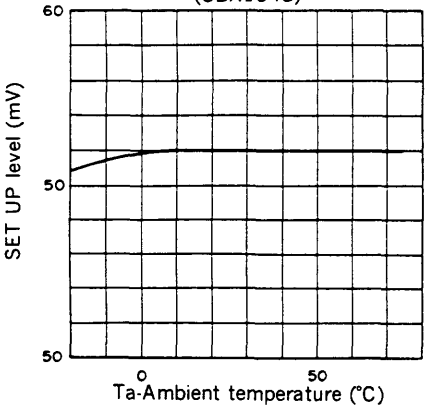
Burst level temperature characteristics

(SBX1548)



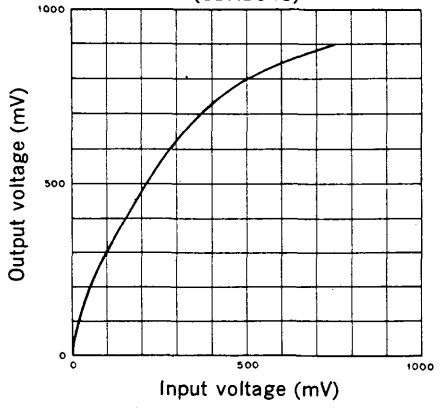
SET UP level temperature characteristics

(SBX1548)



C-γ control characteristics

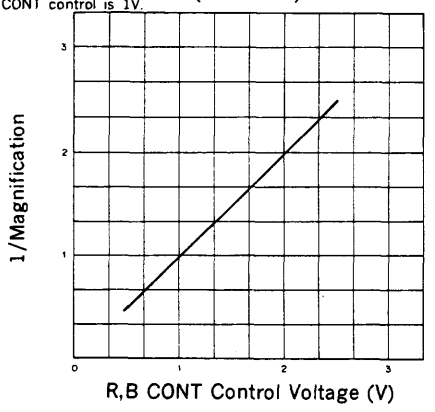
(SBX1548)



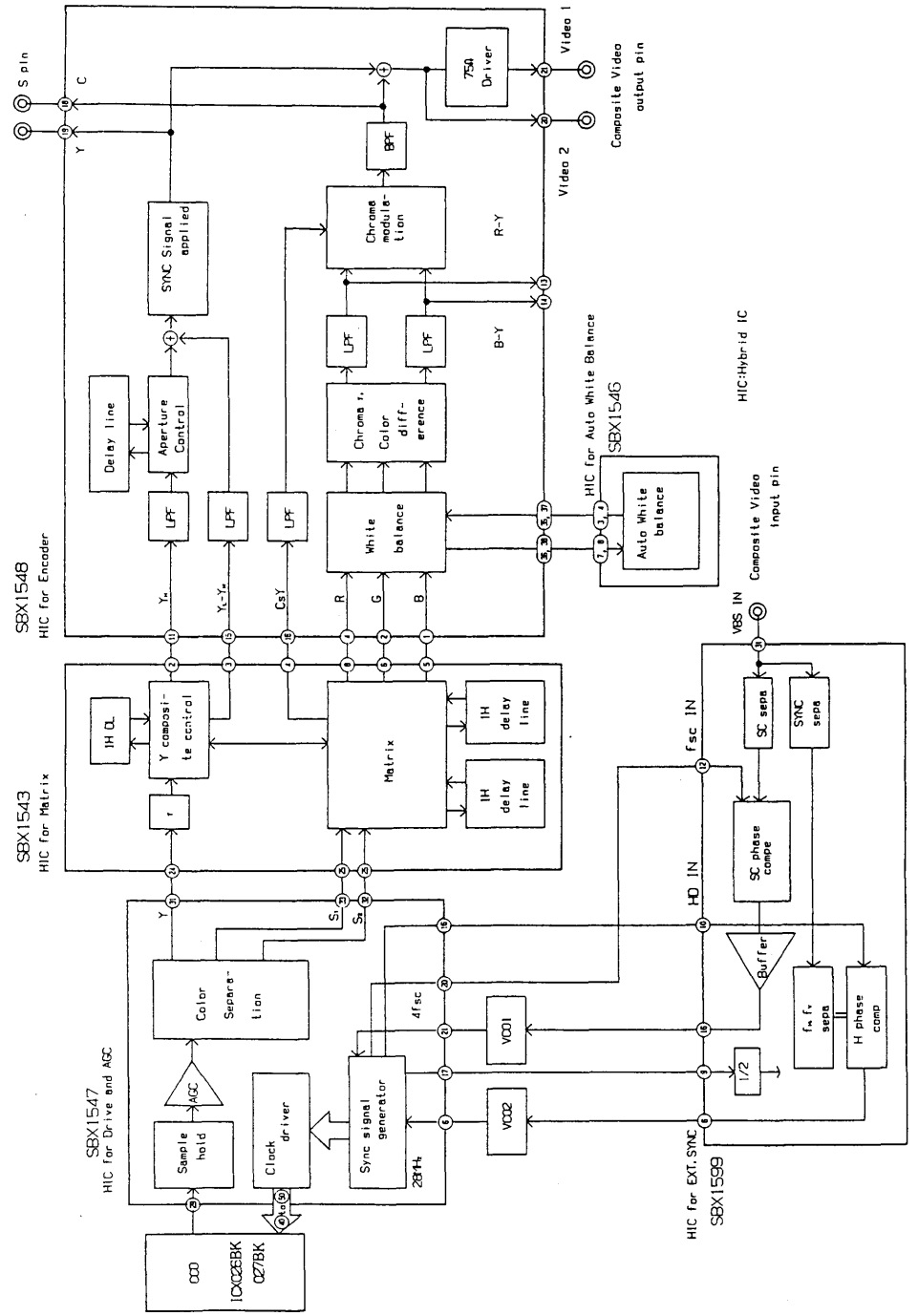
WB R, B CONT control characteristics

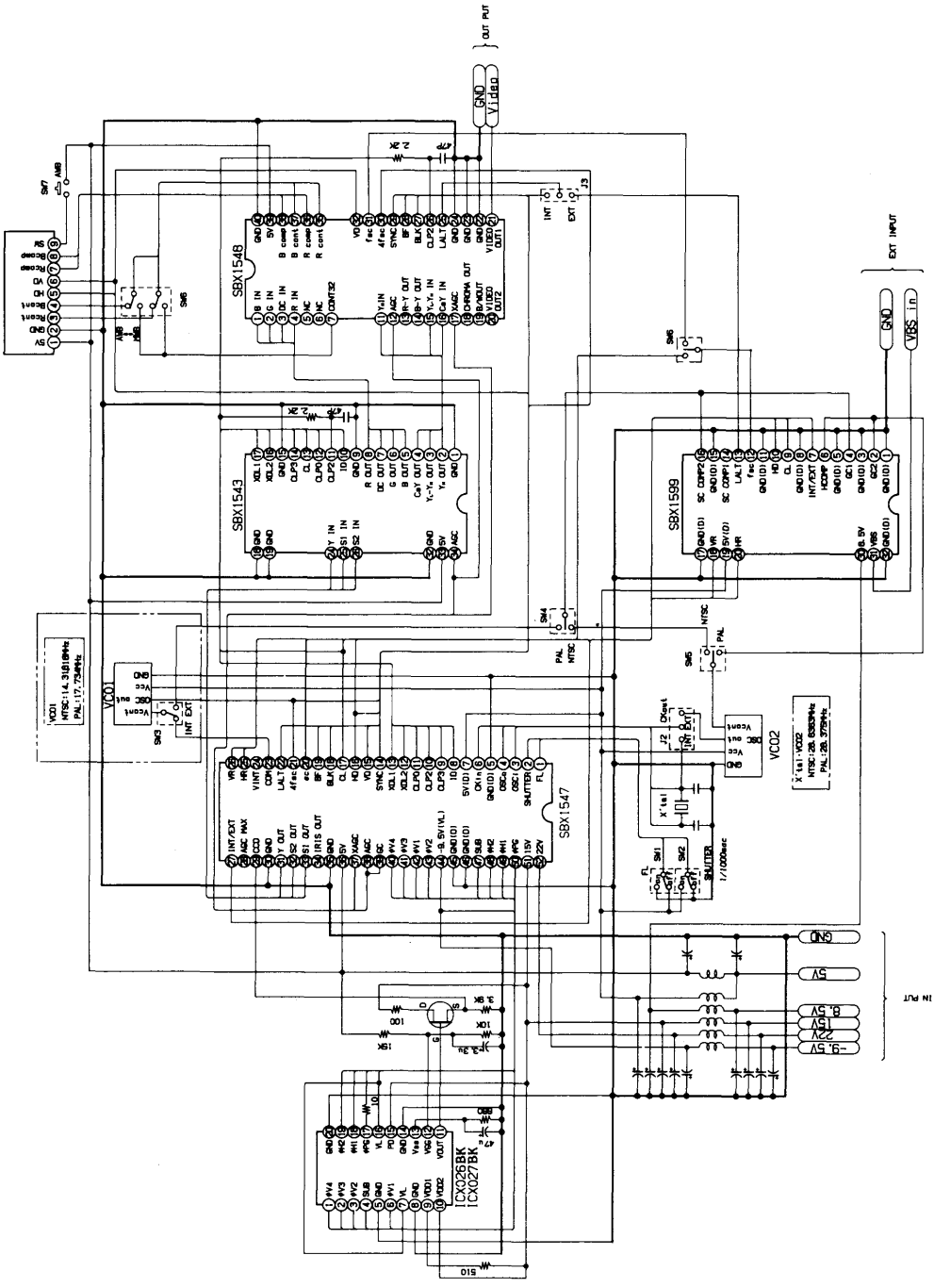
Output is taken at 1 when R,B CONT control is 1V.

(SBX1548)



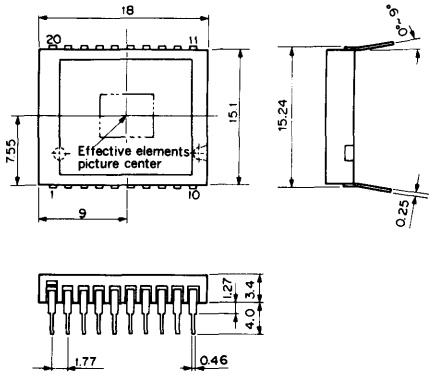
System Block Diagram



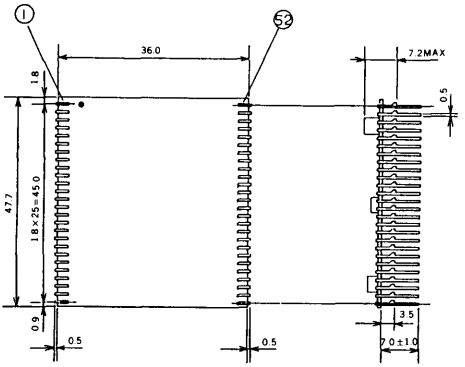

SBX1546
SBX1548
SBX1543
SBX1599
SBX1547
VCO1
VCO2
ICX026BK
ICX027BK
OUT PUT
EXT INPUT
IN PUT
GND
Video
VBS in
INT
EXT
PAL
NTSC
SHUTTER
5V
9.5V
12V
-9.5V

Package Outline **Unit: mm**

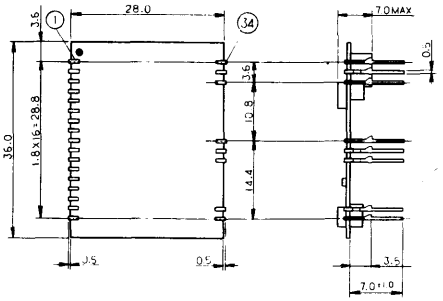
20pin DIP (Ceramic) ICX026BK-3 ICX027BK-3



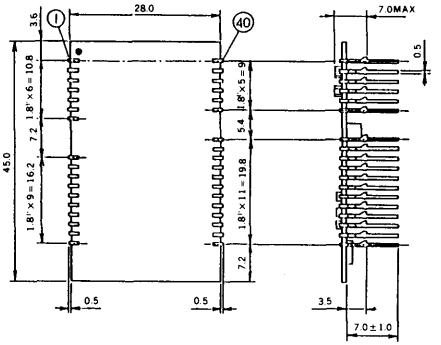
SBX1547-01/02



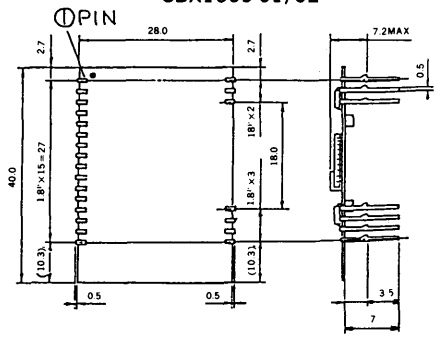
SBX1543-01



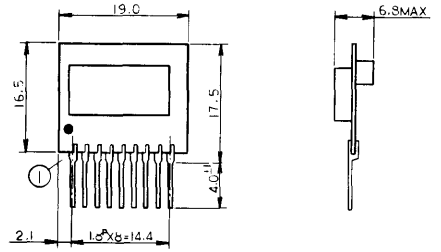
SBX1548-01/21



SBX1599-01/02



SBX1546-01



CCD image sensor Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures.
- Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
- When handling directly use an earth band.
- Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- Ionized air is recommended for discharge when handling CCD image sensor.
- For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
- Make sure the package temperature does not exceed 80°C.
- Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30 W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently.
- To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
- Operate in clean environments (around class 1000 will be appropriate).
- Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended).
- Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
- Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods to ultra violet rays, color filters are discolored.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.

7) Defect compensation ROM
- This is shipped mounted on SBX1547 in pair with the CCD image sensor. To load on the set, match with a CCD image sensor bearing an indentical serial number label.
When there is no defect there is no ROM or serial number.

IC for Scanning System of Video Camera

4) IC for Scanning System of Video Camera

Type	Application	Function	Page
CXD1030M	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL	313
CXD1158M	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL sub carrier output × 3	322
CXD1159Q	Sync signal generator	14MHz (18MHz) demultiplier, for NTSC, PAL window pulse output	332
CXD1217M	Sync signal generator	Compatible with the respective systems, NTSC, PALM, PAL and SECAM color framing by the respective systems, NTSC, PALM, PAL and SECAM	341
CX23047B	Timing pulse generator for scanning system	CCD drive timing pulse generation, signal processing pulse generation, for ICX018CK/CL, ICX021CK/CL	353
CXD1035BQ-Z	Timing pulse generator for scanning system	CCD drive timing pulse generation, signal processing pulse generation, for ICX022AK/AL, ICX024AK/AL	364
CXD1141M	Variable electric shutter timing generator	Variable electronic shutter timing generation (1/60 to 1/10000 sec.) for ICX022AK/AL, ICX024AK/AL	376
CXD1156Q/R	Timing Generator for CCD driving Camera	CCD drive timing pulse generation, Variable electronic shutter timing generation (1/60 to 1/10000 sec,) for ICX026BK/BL, ICX027BK/BL	380
CXD1251Q	Blemish compensation timing generator	Blemish compensation timing generator, for ICX026BK/BL, ICX027BK/BL	393
CXD1255Q	Timing Generator for CCD driving Camera	CCD drive timing pulse generation, signal processing pulse generation, for ICX038AK/ICX039AK variable electronic shutter timing generation (1/60~1/10000 sec)	398
CXB0026AM	CCD clock driver	CCD imager driver × 2, compatible with high frequency operation	412
CX20180	Vertical clock drive	CCD imager driver × 4, lead-out generation inverter, negative voltage generation inverter	415
CXA1065M	Vertical clock drive	CCD imager driver × 4, lead-out generation inverter, negative voltage generation inverter	426
CXD1250M	Vertical clock drive	CCD imager driver × 4, lead-out generation inverter	441

SONY

CXD1030M

Sync. Signal Generator for Camera

Description

The CXD1030M is a sync. signal generator for video cameras.

Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption
  (Standard NTSC: 25 mW; PAL: 30 mW)
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync.

Function

Sync. signal generator

Structure

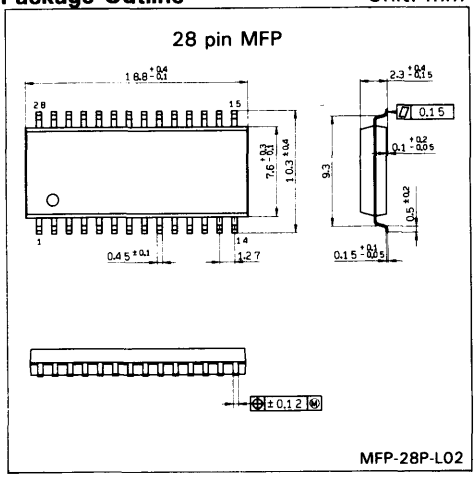
Silicon gate CMOS IC

Application

Video • Camera

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS}* − 0.3 to 7.0	V
• Input voltage	V_I	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Output voltage	V_O	V_{SS}* − 0.3 to V_{DD} + 0.3	V
• Operating temperature	T_{opr}	− 20 to + 75	°C
• Storage temperature	T_{stg}	− 55 to + 150	°C

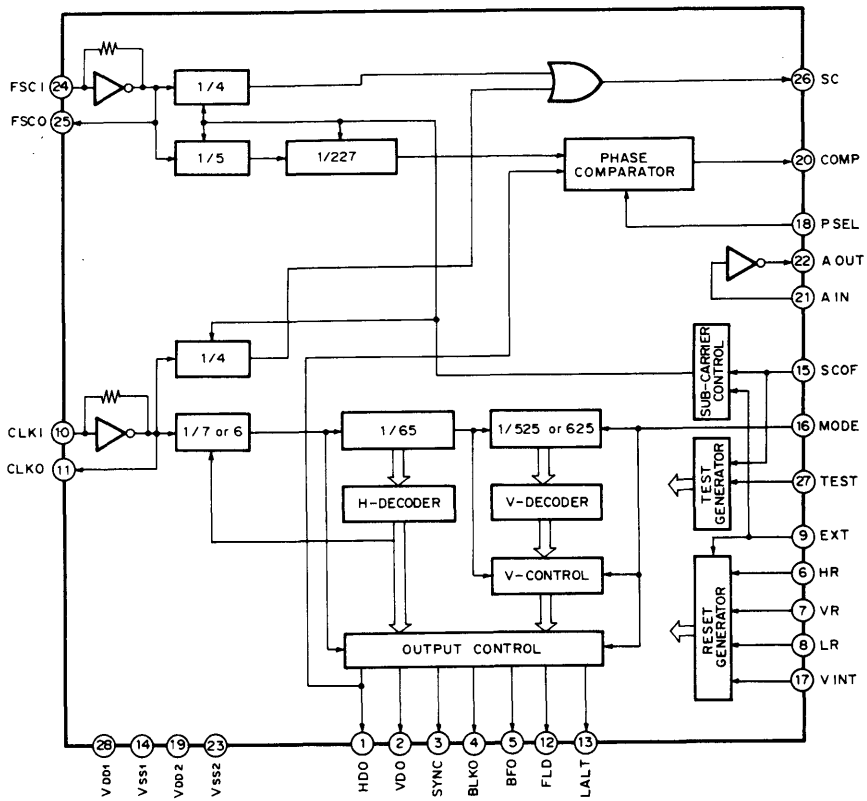
* V_{SS} = 0V

Recommended Operating Conditions

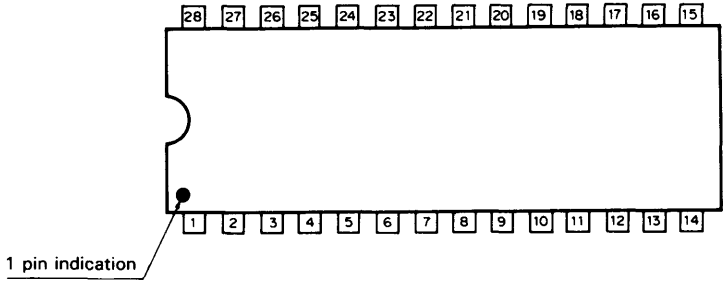
• Supply voltage	V_{DD}	4.50 to 5.50	V
• Operating temperature	T_{opr}	− 20 to + 75	°C

70110-TO

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	HDO	O	Horizontal drive pulse
2	VDO	O	Vertical drive pulse
3	SYNC	O	Complex synchronized pulse
4	BLKO	O	Complex branking pulse
5	BFO	O	Burst flug pulse
6	HR	I	H reset input
7	VR	I	V reset input
8	LR	I	LALT reset input
9	EXT	I	Internal/external mode switching $\overline{\text{INT}}$/EXT
10	CLKI	I	Clock input (NTSC: 14.31818 MHz, PAL: 14.1875 MHz)
11	CLKO	O	Clock output
12	FLD	O	Field pulse
13	LALT	O	Line alternate pulse
14	V_{SS1}	–	GND
15	SCOF	I	Sub carrier suppress input L: OFF
16	MODE	I	NTSC/PAL mode switching $\overline{\text{NTSC}}$/PAL
17	VINT	I	Initialize input
18	PSEL	I	Phase comparator polarity switching
19	V_{DD2}	–	Inverter +5V for filter
20	COMP	O	Phase comparator output
21	AIN	I	Inverter input for filter
22	AOUT	O	Inverter output for filter
23	V_{SS2}	–	Inverter GND for filter
24	FSCI	I	$4f_{SC}$ clock input
25	FSCO	O	$4f_{SC}$ clock output
26	SC	O	Sub carrier output
27	TEST	I	Test input (L normal)
28	V_{DD1}	–	+5V

Electrical Characteristics

DC characteristics

$V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_{opr} = -20$ to $+75°C$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}	Test circuit (2)		2.0		mA
		I_{DDS}	Static state*1	0		0.1	μA
Output voltage I*2	H level	V_{OH}	$I_{OH} = -1.0$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 1.0$ mA	V_{SS}		0.4	V
Output voltage II*3	H level	V_{OH}	$I_{OH} = -0.5$ mA	$V_{DD}-0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 0.5$ mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		$0.7V_{DD}$			V
	L level	V_{IL}				$0.3V_{DD}$	V
Input leak current		I_{LI}	V_I = 0V to V_{DD}	−25		25	μA
Input leak current*4		I_{LZ}		−40		40	μA

Note) *1 $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
*2 Output pins except "AOUT"
*3 "AOUT" pin
*4 Three state pin

I/O Capacitance

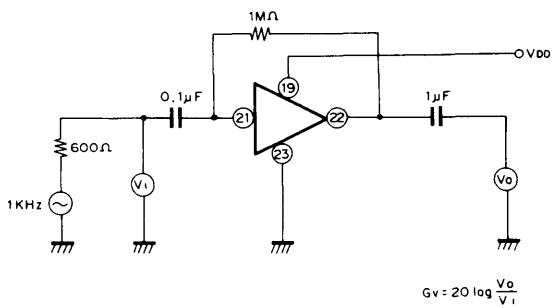
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			12	pF
Output pin	C_{OUT}			12	pF

Test condition: $V_{DD} = V_I = 0V$, $f_M = 1$ MHz

Filter amplifier characteristics

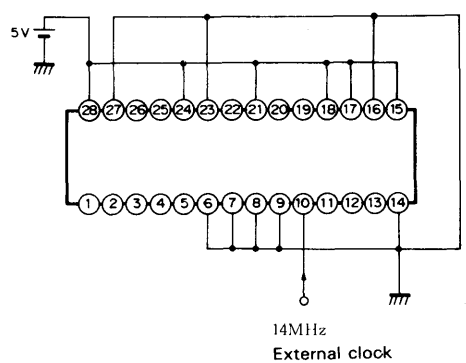
Voltage gain GV 23dB (Typ.)

Test circuit (1)



$Gv = 20 \log \frac{Vo}{Vi}$

Test circuit (2)



14MHz
External clock

Description of Function

1. Generation of various sync. signals (See the Timing Chart.)
   Various sync. signals are generated from clocks.

- Clock frequencies
  NTSC: 910 fH (14.31818 MHz)
  PAL : 908 fH (14.1875 MHz)
  4 fSC (17.734475 MHz)

2. PAL 4 fSC PLL
   Using 908 fH as the master clock, the 4 fSC is put in phase. Corresponding to an external filter (passive or active), the phase comparator polarity can be switched.

Filter	PSEL	Master (908fH)	4fSC	COMP
Passive	L	Fast	Slow	H
		Slow	Fast	L
Active	H	Fast	Slow	L
		Slow	Fast	H

3. SC (SubCarrier) generation

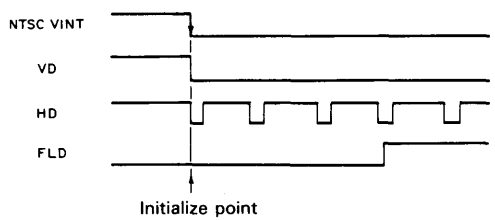
Mode	INT or EXT	SC
NTSC	INT	910fH/4
NTSC	EXT	4fSC/4
PAL	×	4fSC/4

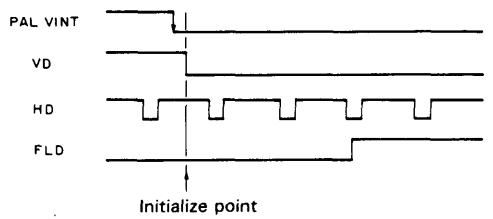
INT : INTERNAL mode
(EXT = L)
EXT: EXTERNAL mode
(EXT = H)

Unused counters are stopped in any of the mode.
When SC is not required, any counters on SC are stopped and SC is not output by SCOF being set to L.

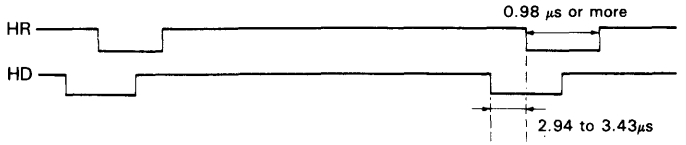
4. Initialization and Reset
   In the INT mode, the circuit is initialized with the fall of VINT. At this time, the H reset, V reset, and LALT reset are not accepted. In the EXT mode, VINT is not accepted but the H reset, V reset, and LALT reset are accepted.

- Initialization (VINT)
  When EXT is L, the fall of VINT is detected and operation is started by the circuit being initialized at the VD fall position immediately prior to field I. (The initialization is completed within 100 ns after the fall is detected.)

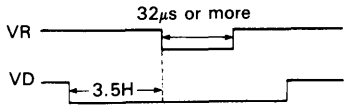




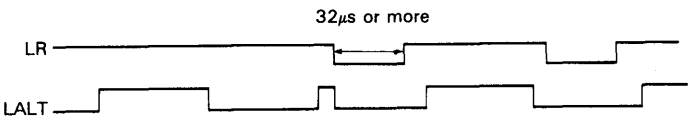
- H reset (HR)
  A reset is executed with the first fall but no reset will be done as long as the subsequent edges do not deviate by more than two clocks (0.98 μs).
  The minimum reset pulse width is 0.98 μs.
  HD is reset 2.94 to 3.43 μs in advance of HR input.



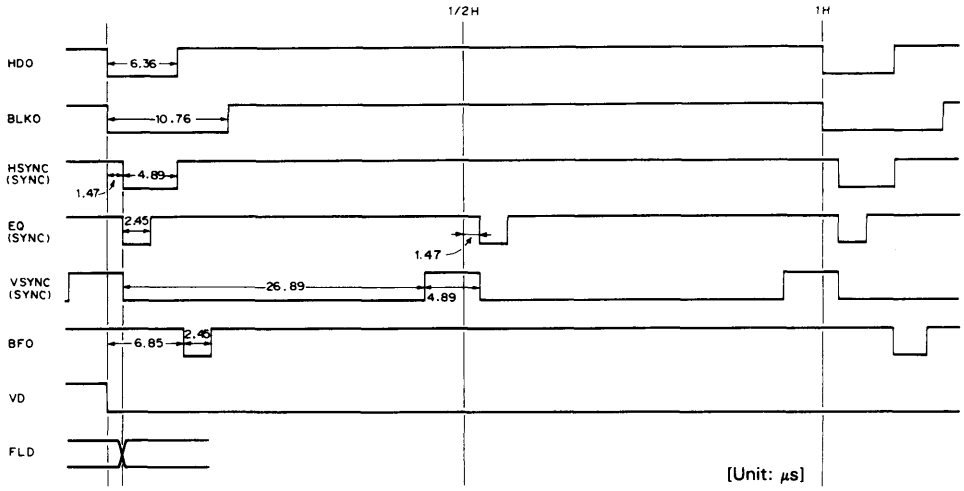
- V reset (VR)
  VD is reset 3.5H in advance of VR input.
  The minimum reset pulse width is 32 μs.



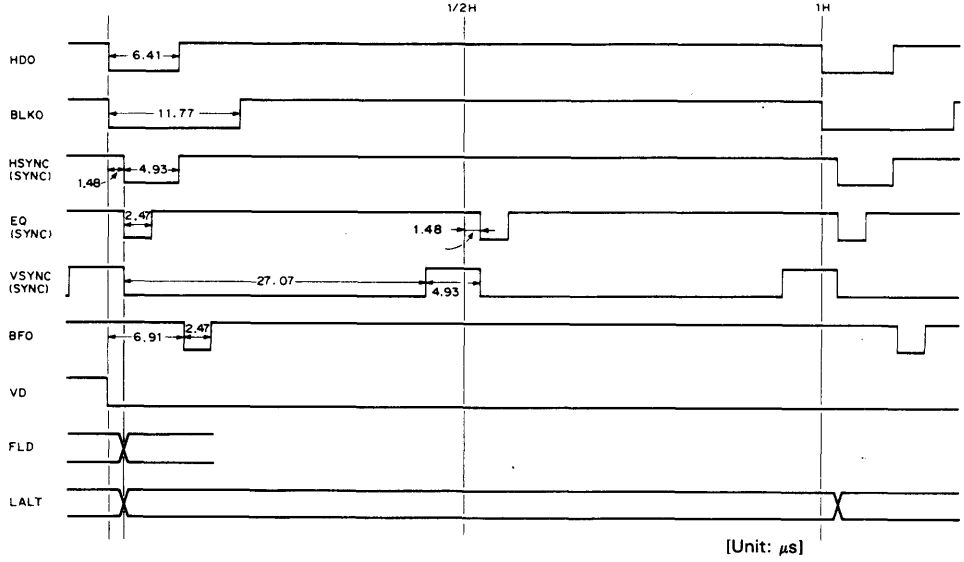
- LALT reset (LR)
  LALT is reset in the same phase as the LR input.
  The minimum reset pulse width is 32 μs.



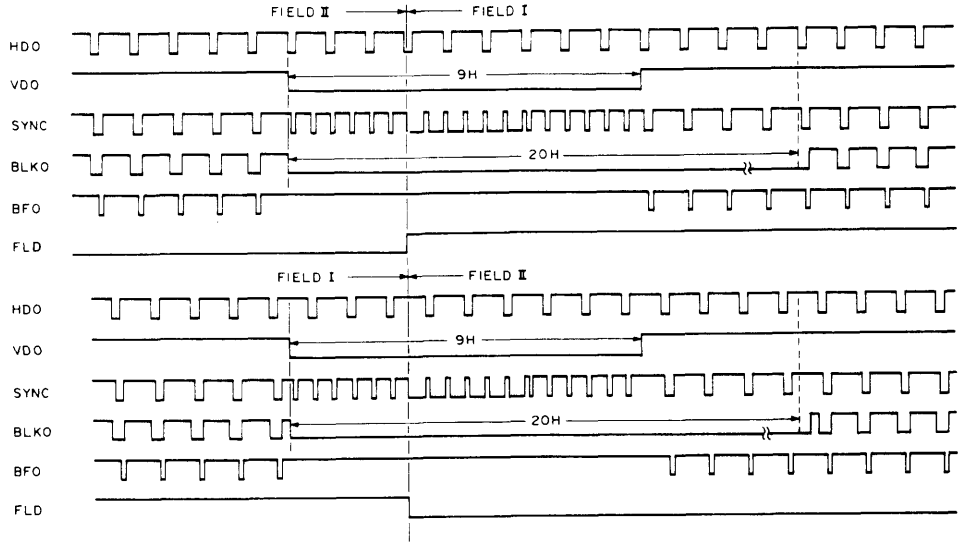
Timing Chart H (NTSC)



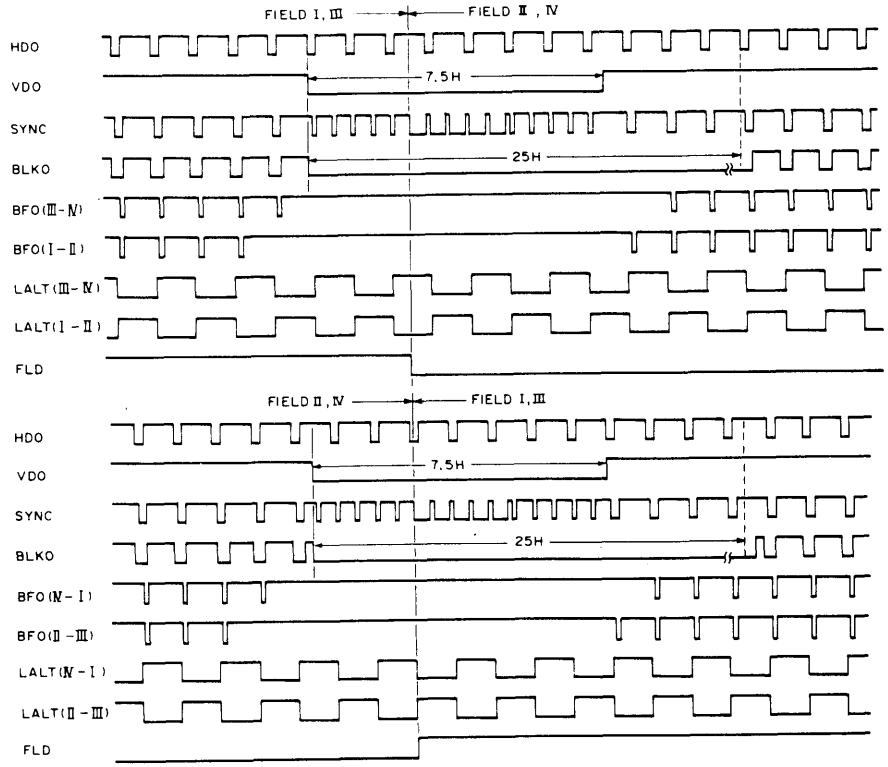
Timing Chart H (PAL)



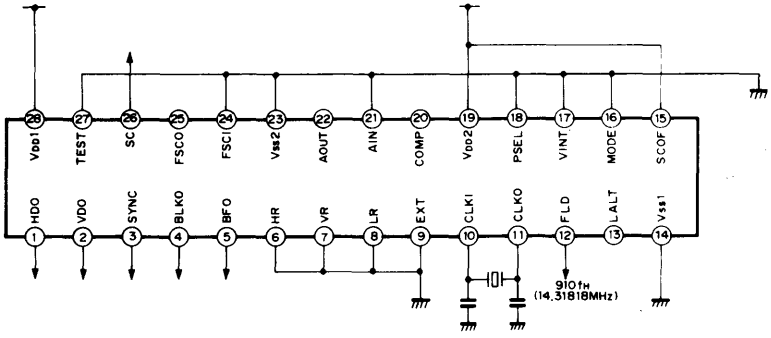
Timing Chart V (NTSC)



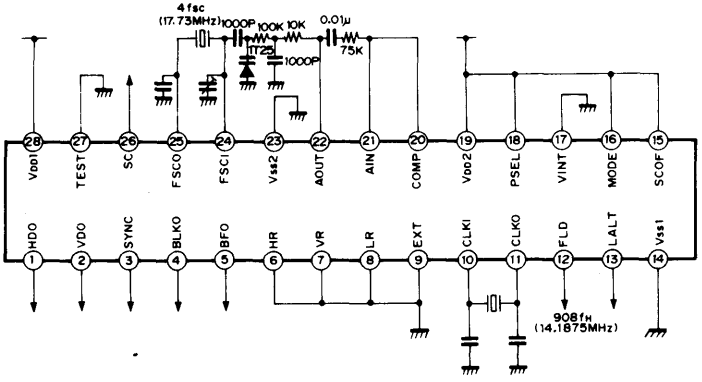
Timing Chart V (PAL)



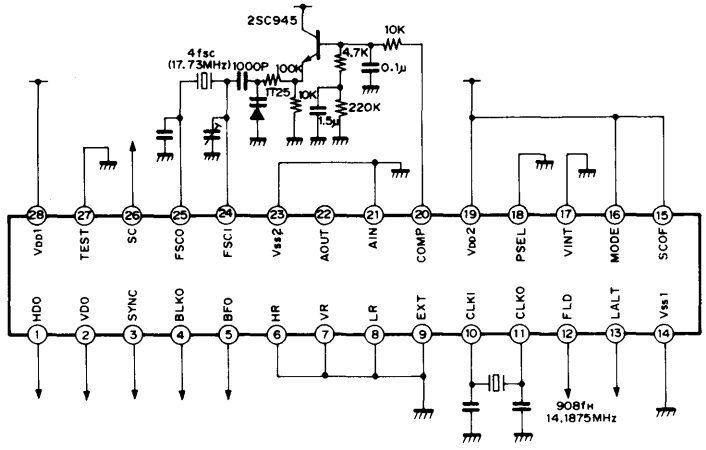
Application Circuits
NTSC (Internal mode)



PAL (Filter configuration 1, Internal mode)



PAL (Filter configuration 2, Internal mode)



SONY

CXD1158M

Synchronizing Signal Generator for Consumer Video Camera

Description

CXD1158M is a synchronizing signal generator for video camera.

Features

- Adapts to NTSC or PAL by switching mode
- Low power consumption
- Built-in phase comparator and inverter for active filter (separate power supply for the filter inverter)
- External sync

Structure

Silicon gate CMOS IC

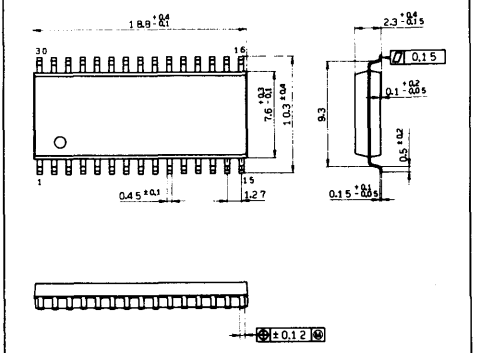
Application

Consumer video camera

Package Outline

Unit: mm

30 pin SOP (Plastic)



SOP-30P-L01

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS}*1	−0.3 to +7.0	V
• Input voltage	V_I	V_{SS}*1	−0.3 to V_{DD} + 0.3*2	V
• Output voltage	V_O	V_{SS}*1	−0.3 to V_{DD} + 0.3*2	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C

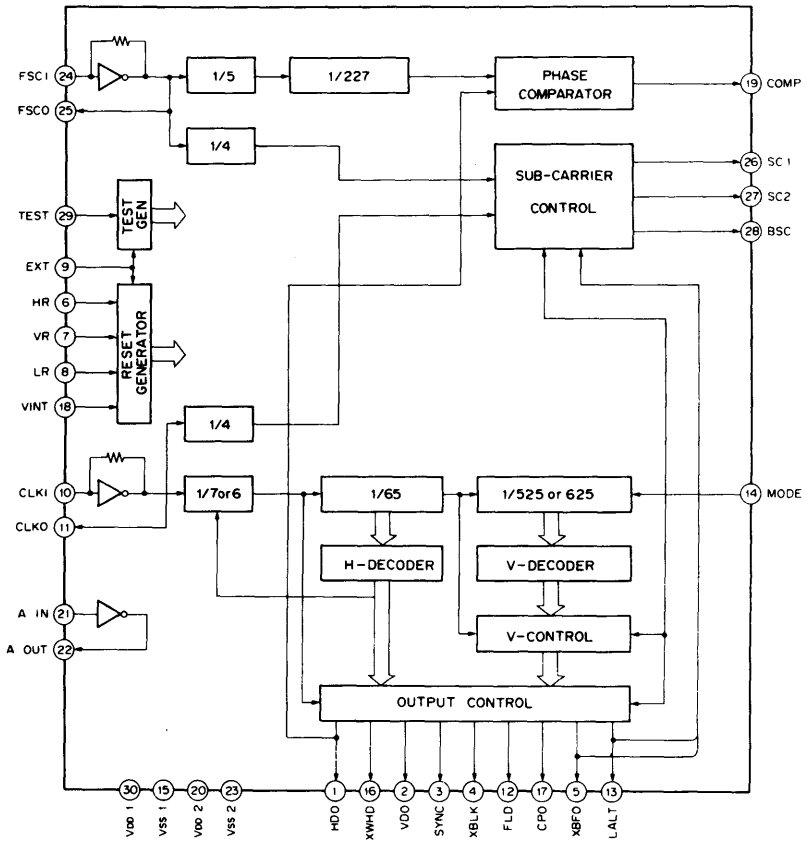
Note) *1. V_{SS} = 0V
*2. Normal value, Transient value 0.5V (20 to 30 ns)

Recommended Operating Conditions

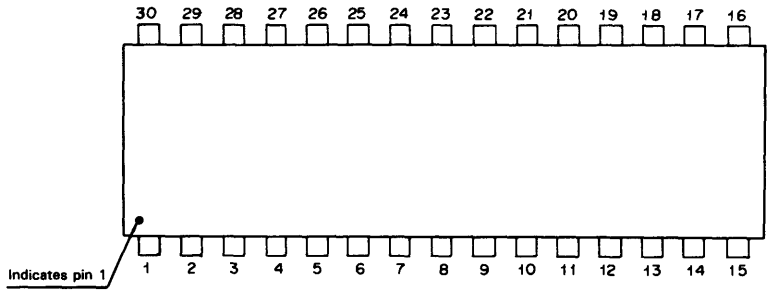
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	−20 to +75	°C

80307-TO

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	HDO	O	Horizontal drive pulse
2	VDO	O	Vertical drive pulse
3	SYNC	O	Composite sync. pulse
4	XBLK	O	Composite blanking pulse
5	XBFO	O	Burst•flag pulse
6	HR	I	H reset input
7	VR	I	V reset input
8	LR	I	LALT reset input
9	EXT	I	$\overline{\text{INT}}$/EXT mode switching
10	CLKI	I	Clock input
11	CLKO	O	Clock output
12	FLD	O	Field pulse
13	LALT	O	Line alternate pulse
14	MODE	I	NTSC/PAL mode switching NTSC/PAL
15	$V_{SS}1$	—	GND
16	XWHD	O	Wide Horizontal drive pulse
17	CPO	O	Clamp pulse
18	VINT	I	Initialize input
19	COMP	O	Phase comparator output
20	$V_{DD}2$	—	Inverter +5V for filter
21	AIN	I	Inverter input for filter
22	AOUT	O	Inverter output for filter
23	$V_{SS}2$	—	Inverter GND for filter
24	FSCI	I	Clock input 4 f_{SC}
25	FSCO	O	Clock output 4 f_{SC}
26	SC1	O	Sub carrier 1
27	SC2	O	Sub carrier 2
28	BSC	O	Bursted sub carrier
29	TEST	I	Test input (Normally L)
30	$V_{DD}1$	—	+5V

Electrical Characteristics

DC characteristics

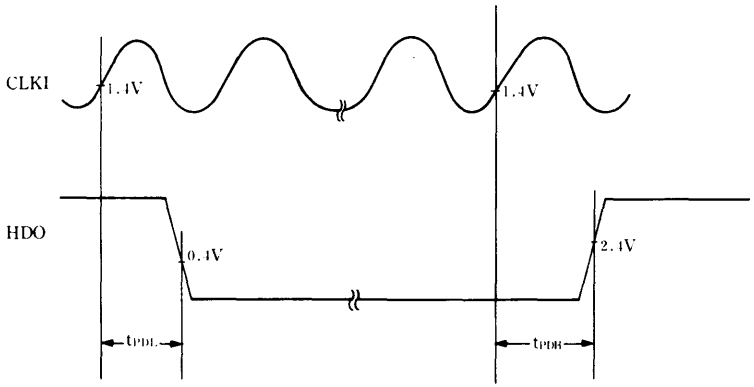
$V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$ $T_{op} = -20$ to $+75°C$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}			2.0		mA
		I_{DDS}	Static state*1	0		0.1	mA
Output voltage I*2	H level	V_{OH}	$I_{OH} = -2mA$	$V_{DD} - 0.5$		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 4mA$	V_{SS}		0.4	V
Output voltage II*3	H level	V_{OH}	$I_{OH} = -1.5mA$	2.5		V_{DD}	V
	L level	V_{OL}	$I_{OL} = 1.5mA$	V_{SS}		2.5	V
Input voltage	H level	V_{IH}		0.7 V_{DD}			V
	Level	V_{IL}				0.3 V_{DD}	V
Input leak current		I_{LI}	$V_I = 0V$ to V_{DD}	−10		10	μA
Output leak current*4		I_{OZ}		−10		10	μA

*1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
*2. Output pins except "A OUT"
*3. "A OUT" pin
*4. Tri-state pin 19

AC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
H to L Propagation delay time	t_{PDL}	$V_{OL} = 0.4V$			45	ns
L to H Propagation delay time	t_{PDH}	$V_{OH} = 2.4V$			45	ns



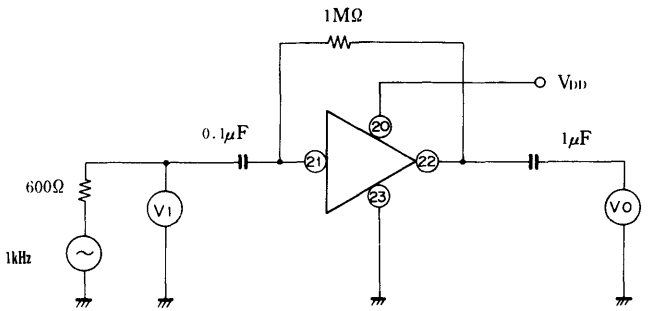
I/O capacitance

$V_{DD}V_I = 0V$, $f_M = 1MHz$

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Filter Amplifier Characteristics

Voltage gain Gv: 25dB (Typ.)



Test circuit

Description of Function

Generation of various synchronizing signals (See the Timing Chart).

Generates various synchronizing signals from Clock.

- Clock frequency:

  NTSC: 910 fH (14.31818 MHz)

  PAL: 908 fH (14.1875 MHz)

  4 fSC (17.734475 MHz)

PLL for PAL 4 fSC

Matches 4 fSC phase, with 908 fH as Master clock.

An active filter is used as filter.

908 fH	4 fSC	COMP
Forward	Back	L
Back	Forward	H

Generation of SC (Sub-Carrier)

Generates three kinds of sub-carrier.

SC1, SC2 and BBC. (Refer to the Timing Chart for phase.)

Mode	Sync.	Sub-carrier (SC)
NTSC	INT	910 fH/4
NTSC	EXT	No output
PAL	INT or EXT	4 fsc/4

INT: INTERNAL mode (EXT = L)

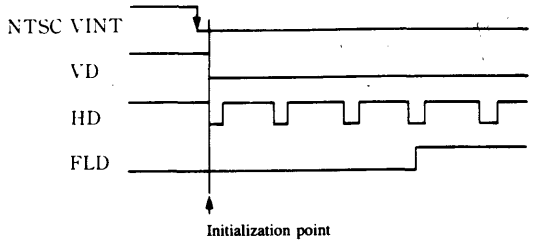
EXT: EXTERNAL mode (EXT = H)

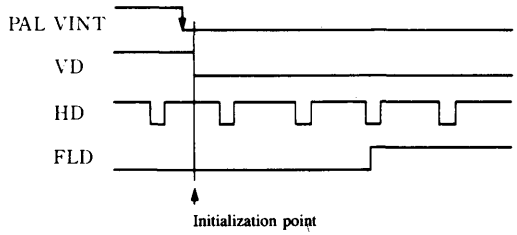
Any unused counter is stopped in any mode.

Initialize and Reset

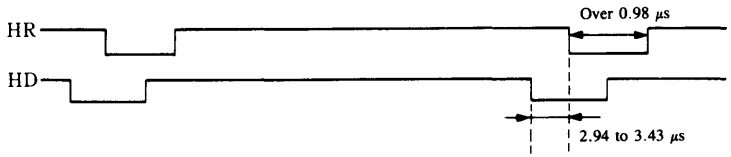
In the INT mode, the circuit is initialized at falling edge of VINT. H reset, V reset and LALT reset are not accepted in this mode. In the EXT mode, in contrast, VINT is not accepted, while H reset, V reset and LALT reset are accepted.

- Initialize (VINT)
  Detection of VINT's falling edge causes, at the first clock, initialization at the position of falling edge of VD immediately before the ODD (1st) field to start operation. (Initialization is completed within 100 ns from the detection of falling edge.)



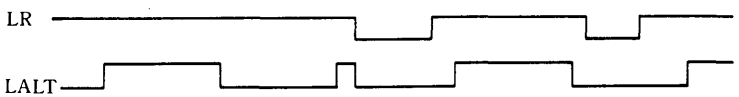


- H reset (HR)
  It is reset at the first falling edge, and not reset unless there is an offset of over 2 clocks (0.98 μs) for the next and subsequent edges. The minimum pulse duration is 0.98 μs.
  The position of reset is at 2.94 to 3.43 μs forward from HR input.



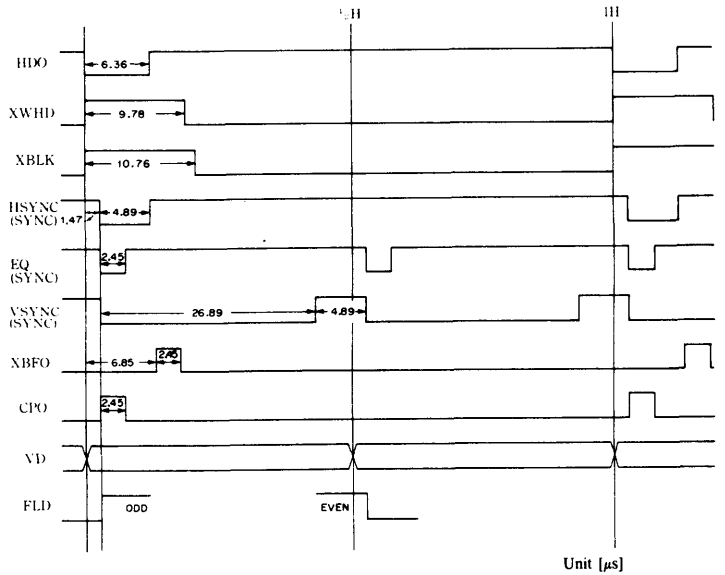
- V reset (VR)
  It is reset at a position of VD at 3.5 H forward from VR. The minimum reset pulse duration is 32 μs.

- LALT reset (LR)
  LALT is reset to the same phase as that of LR input. The minimum reset pulse duration is 32 μs.

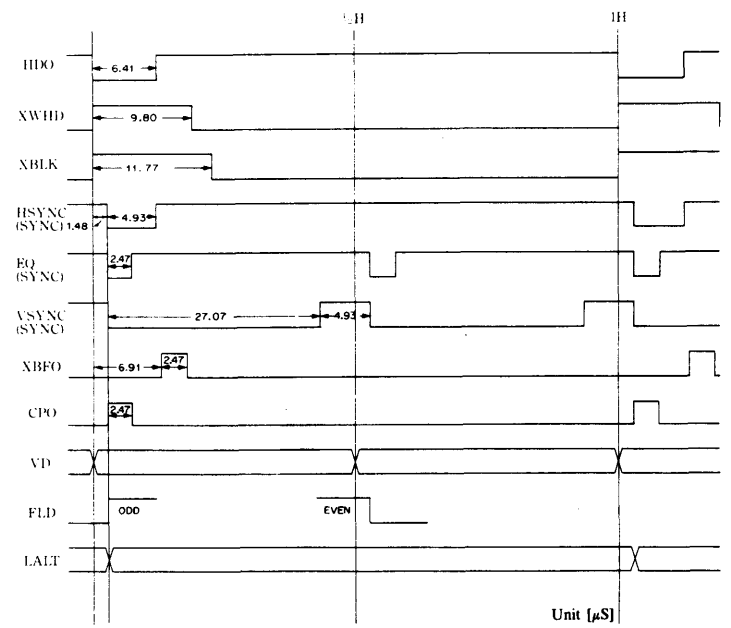


Timing Chart

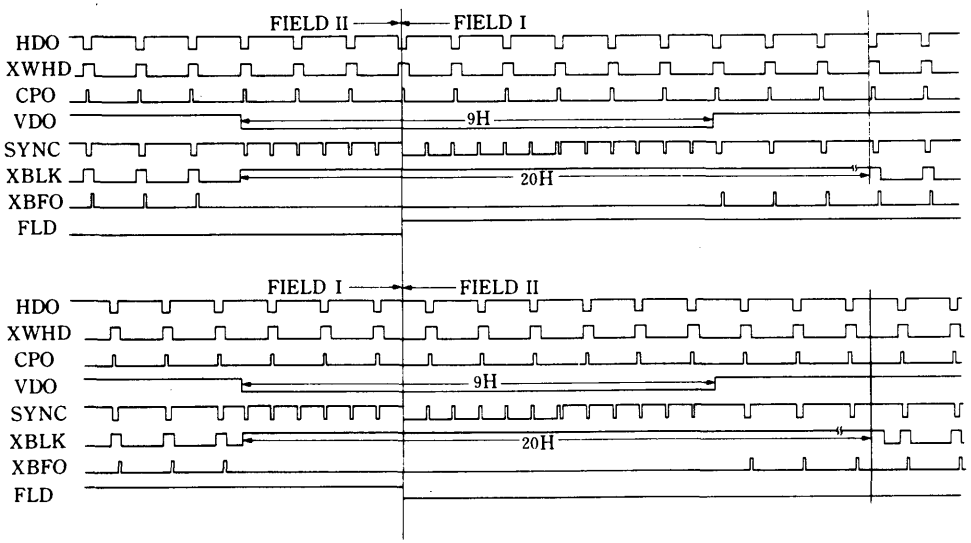
NTSC H



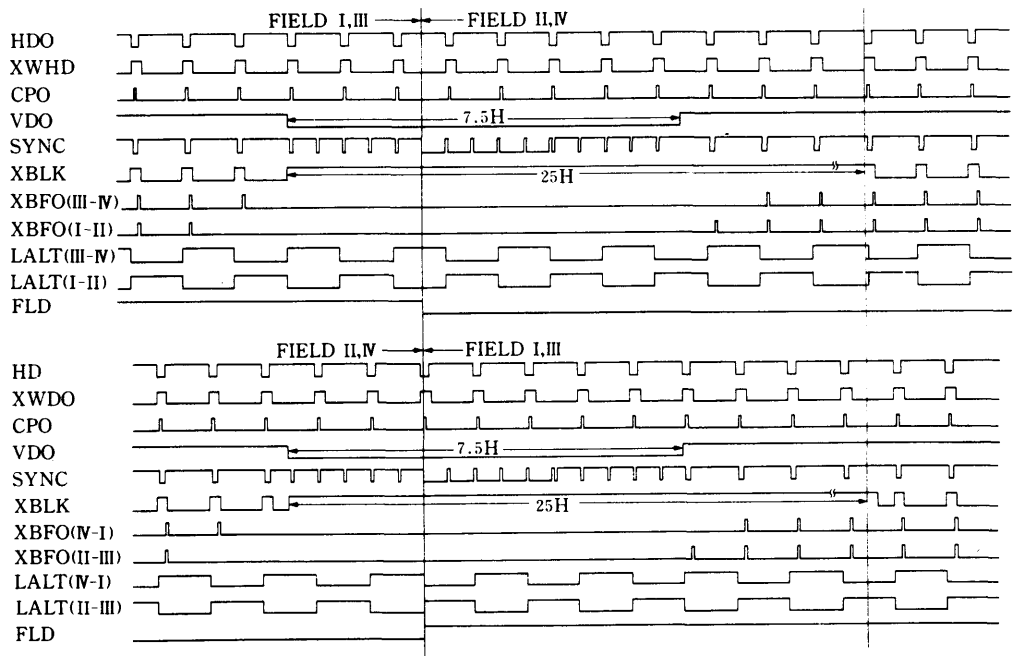
PAL H



NTSC V

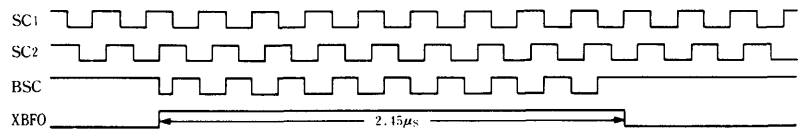

FIELD II
FIELD I
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO
FLD
9H
20H
FIELD I
FIELD II
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO
FLD
9H
20H

PAL V


FIELD I,III
FIELD II,IV
HDO
XWHD
CPO
VDO
SYNC
XBLK
XBFO(III-IV)
XBFO(I-II)
LALT(III-IV)
LALT(I-II)
FLD
7.5H
25H
FIELD II,IV
FIELD I,III
HD
XWDO
CPO
VDO
SYNC
XBLK
XBFO(IV-I)
XBFO(II-III)
LALT(IV-I)
LALT(II-III)
FLD
7.5H
25H

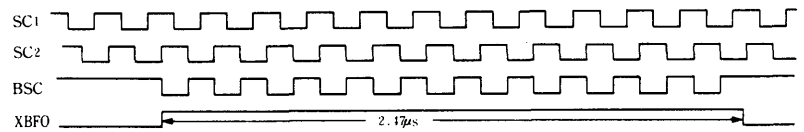
Sub Carrier

NTSC

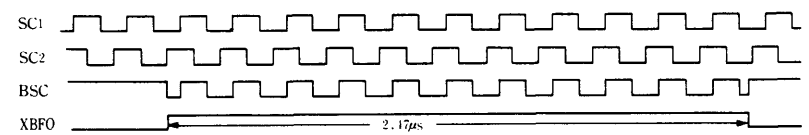


PAL

LALT=H

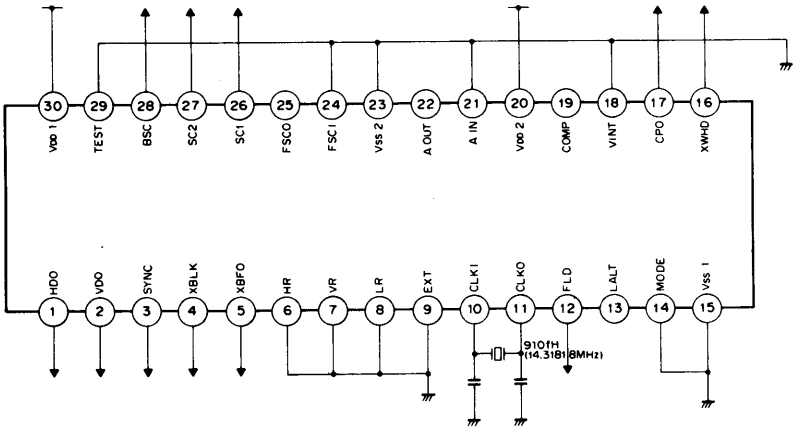


LALT=L

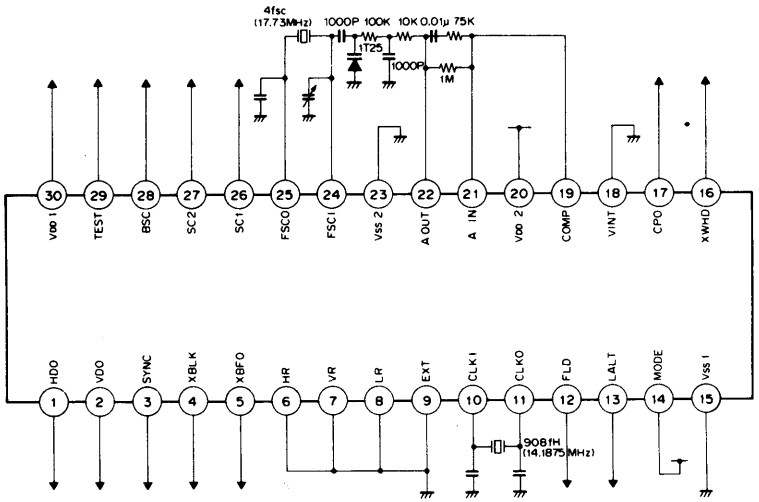


Application Circuit

NTSC (Internal mode)



PAL (Internal mode)



SONY

CXD1159Q

Sync. Signal Generator for Camera

Description

CXD1159Q is a sync. signal generator for consumer video cameras.

Features

- Adapts to NTSC or PAL through mode switching.
- Low power consumption.
- Phase comparator and built in inverter for active filter.
- Internal/External sync.

Functions

- Generator of various sync. signals.

Structure

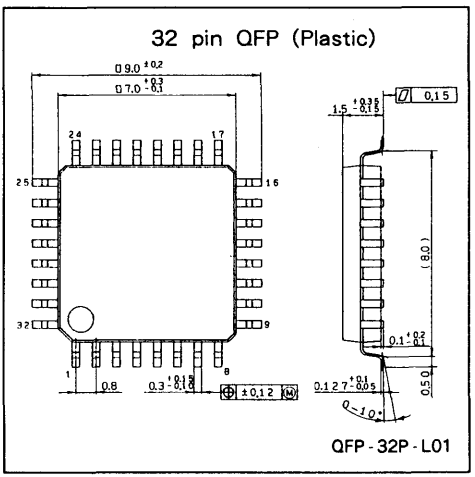
Silicon gate CMOS

Application

- Video cameras

Package Outline

Unit : mm



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS} * − 0.5 to 7.0	V
• Input voltage	V_I	V_{SS} * − 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} * − 0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	− 55 to + 150	°C

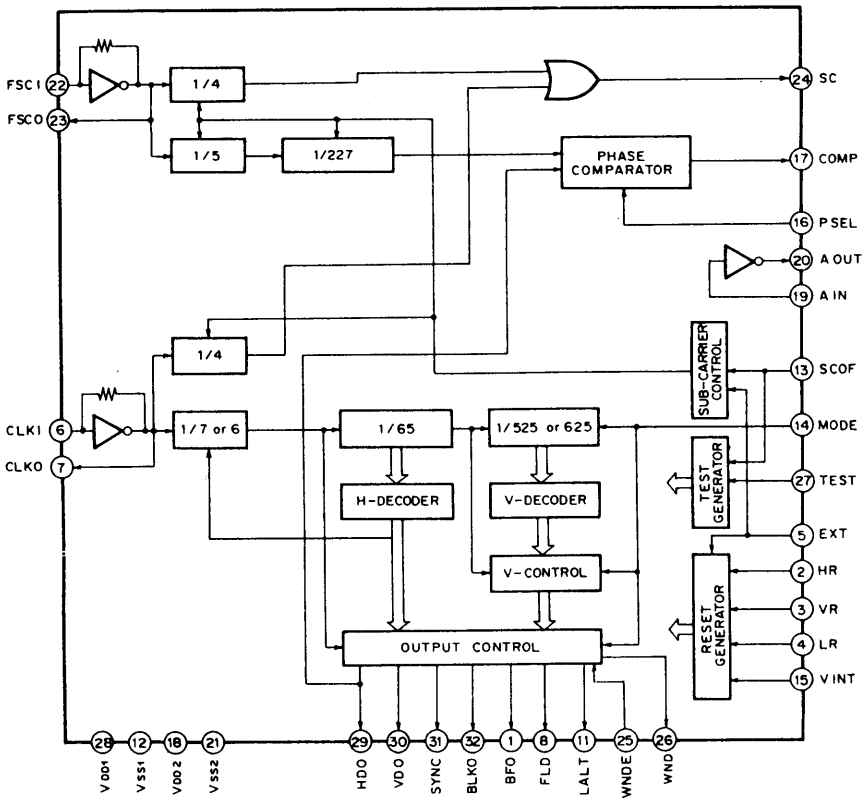
*Vss = 0V

Rcommended Operating Conditions

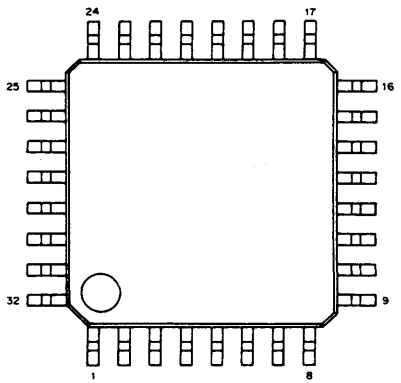
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	− 20 to + 75	°C

80924 – ST

Block Diagram



Pin Configuration



Pin Description

No.	Symbol	I/O	Description
1	BFO	O	Burst flag pulse
2	HR	I	H reset input
3	VR	I	V reset input
4	LR	I	LALT reset input
5	EXT	I	Internal/External mode switching $\overline{INT}$/EXT
6	CLKI	I	Clock input (NTSC : 14.31818MHz, PAL : 14.1875MHz)
7	CLKO	O	Clock output
8	FLD	O	Field pulse
9	N.C.	—	
10	N.C.	—	
11	LALT	O	Line alternate pulse
12	V_{SS1}	—	GND
13	SCOF	I	Sub carrier suppress input L : OFF
14	MODE	I	NTSC/PAL mode switching $\overline{NTSC}$/PAL
15	VINT	I	Initialize input
16	PSEL	I	Phase comparator polarity switch
17	COMP	O	Phase comparator output
18	V_{DD2}	—	+5 power supply for filter inverter
19	AIN	I	Input for filter inverter
20	AOUT	O	Output for filter inverter
21	V_{SS2}	—	GND for filter inverter
22	FSCI	I	4 fsc clock input
23	FSCO	O	4 fsc clock output
24	SC	O	Sub carrier output
25	WNDE	I	WND output enable input (at L : Enable)
26	WND	O	Window output
27	TEST	I	Test input (Normally "L")
28	V_{DD1}	—	+5V
29	HDO	O	Horizontal drive pulse
30	VDO	O	Vertical drive pulse
31	SYNC	O	Composite sync. pulse
32	BLKO	O	Composite blanking pulse

Electrical Characteristics

DC characteristics

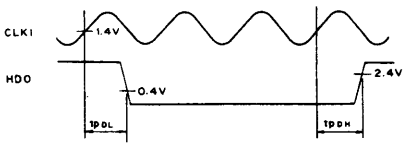
V_{DD} = 5V ± 10%, V_{SS} = 0V, Topr = − 20 to + 75℃

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}			2.0		mA
		I_{DDS}	Static state*1	0		0.1	mA
Output voltage I *2	H level	V_{OH}	I_{OH} = − 2mA	V_{DD} − 0.5		V_{DD}	V
	L level	V_{OL}	I_{OL} = 4mA	V_{SS}		0.4	V
Output voltage II *3	H level	V_{OH}	I_{OH} = − 1.5mA	2.5		V_{DD}	V
	L level	V_{OL}	I_{OL} = 1.5mA	V_{SS}		2.5	V
Input voltage	H level	V_{IH}		0.7V_{DD}			V
	L level	V_{IL}				0.3V_{DD}	V
Input leak current		I_{LI}	V_I = 0V to V_{DD}	− 10		10	μA
Input leak current *4		I_{LZ}		− 10		10	μA

* 1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
* 2. Output pins except "AOUT".
* 3. "AOUT" pin.
* 4. Three state pin.

AC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Falling edge delay time	t_{PDL}	V_{OL} = 0.4V			45	ns
Rising edge delay time	t_{PDH}	V_{OH} = 2.4V			45	ns



I/O capacitance

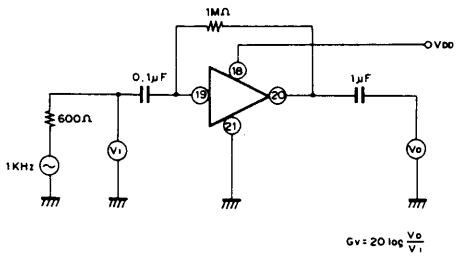
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Test conditions : $V_{DD} = V_I$ = 0V, f_M = 1MHz

Filter amplifier characteristics

Voltage gain Gv 25dB (Typ.)

Test circuit



Functions

1. Generation of various sync. signals (See the Timing Chart.)

Various sync. signals are generated from clocks.

- Clock frequencies

  NTSC : $910f_H$ (14.31818MHz)

  PAL : $908f_H$ (14.1875MHz)

  $4f_{SC}$ (17.734475MHz)

  For the System Clock

  NTSC : $910f_H/7$

  PAL : $908f_H/7$ or 6

2. PAL PLL for 4fsc

To a master clock of $908f_H$ is matched a phase of $4f_{SC}$. The polarity of the phase comparator can be switched according to the type of external filter (passive or active).

Filter	PSEL	Master ($908f_H$)	$4f_{SC}$	COMP
Passive	L	Fast	Delay	H
		Slow	Fast	L
Active	H	Fast	Delay	L
		Slow	Fast	H

3. SC (Sub-Carrier) generation

Mode	INT or EXT	SC
NTSC	INT	$910f_H/4$
NTSC	EXT	$4f_{SC}/4$
PAL	×	$4f_{SC}/4$

INT : Internal mode (EXT = L)
EXT : External mode (EXT = H)

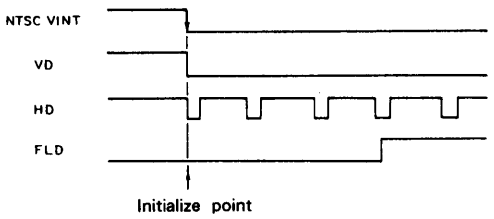
In either mode unused counters are stopped. When SC is not required, by setting SCOF to L all SC counters are stopped and SC is not output.

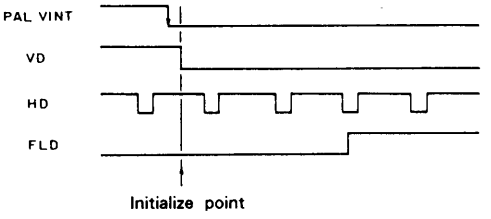
4. Initialization and Reset

In INT mode the circuit is initialized with the fall of VINT. At that time, H, V and LALT resets are not accepted. In EXT mode, VINT is not accepted, whereas H, V and LALT resets are.

- Initialize (VINT)

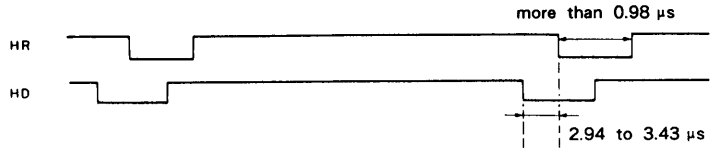
  When EXT = L, VINT fall is detected and operation is started as the circuit is initialized at the VD fall position just before field 1. (Initialization is completed within 100ns after the fall is detected).





- H reset (HR)

  Reset is performed with the first fall. However reset is not done anymore unless there is a deviation of more than 2 clocks (0.98 µs) to the subsequent edges.
  The minimum reset pulse width is 0.98 µs.
  HD is reset 2.94 to 3.43 in advance of HR input.

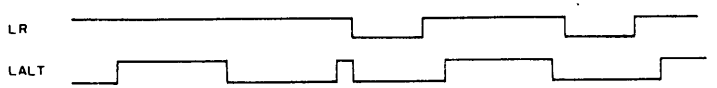


- V reset (VR)

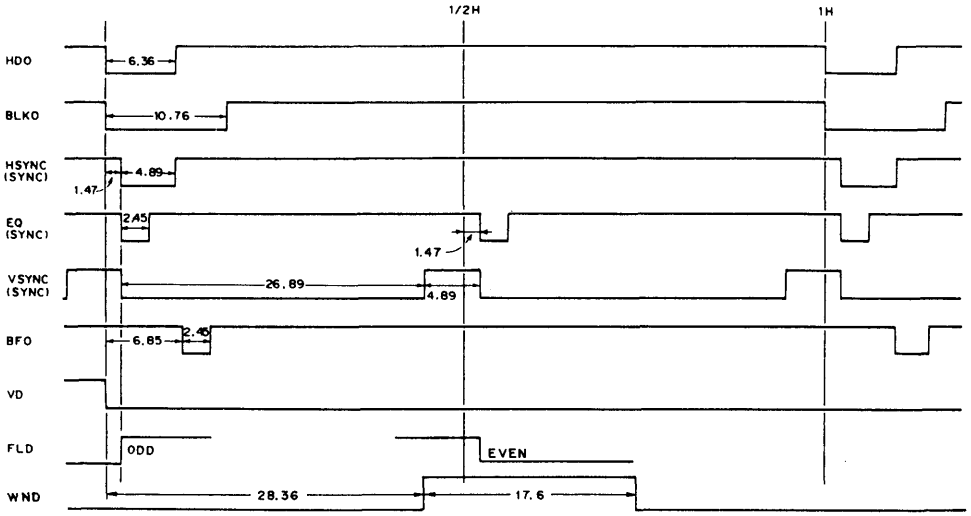
  VD is reset 3.5H in advance of VR input.
  The minimum reset pulse width is 32 µs.

- LALT reset (LR)

  LALT is reset in the same phase as LR input.
  The minimum reset pulse is 32 µs.

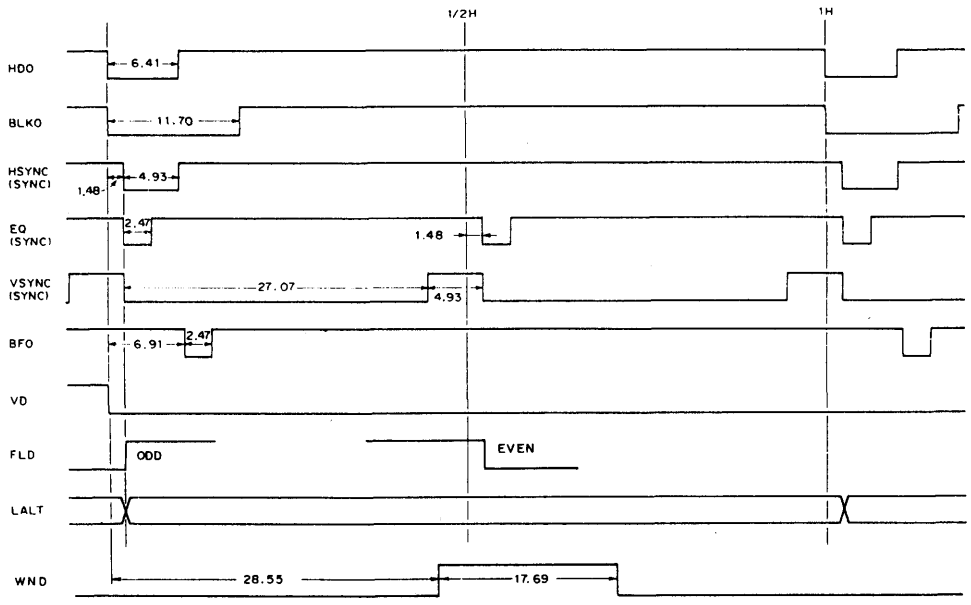


Timing Chart H (NTSC)



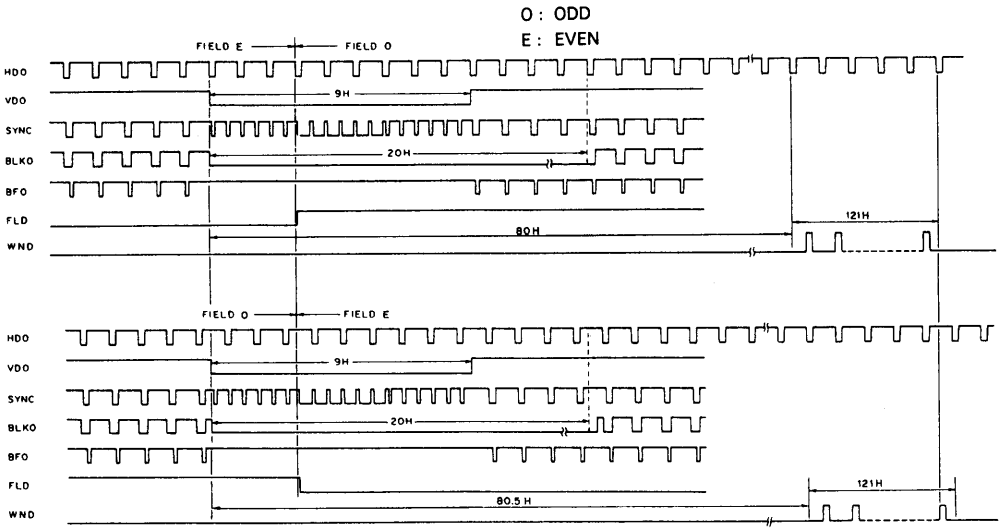
Unit : μs

Timing Chart H (PAL)

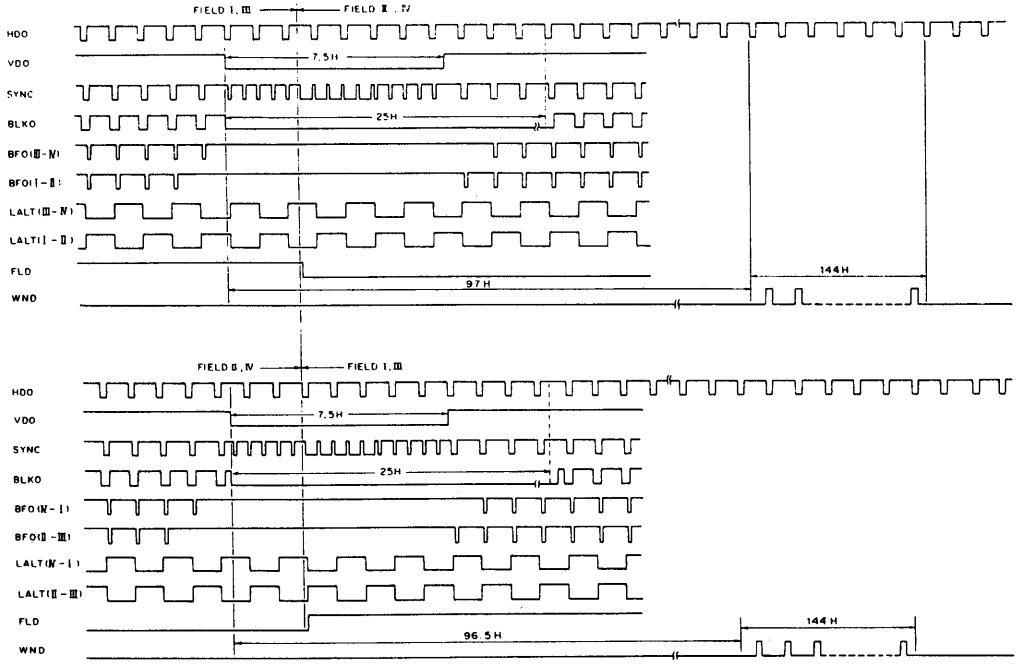


Unit : μs

Timing Chart V (NTSC)

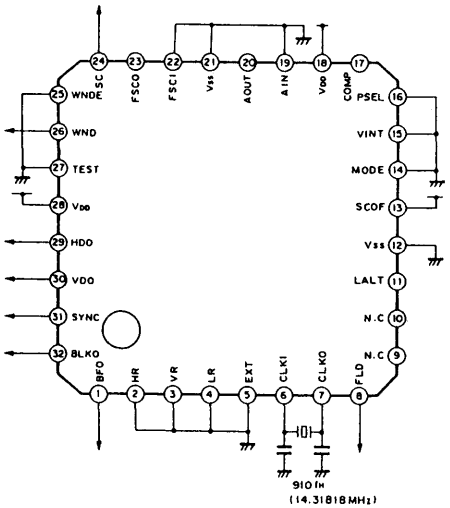


Timing Chart V (PAL)

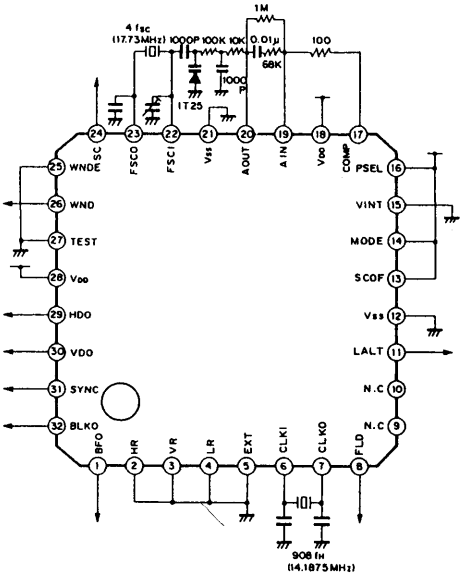


Application Circuit

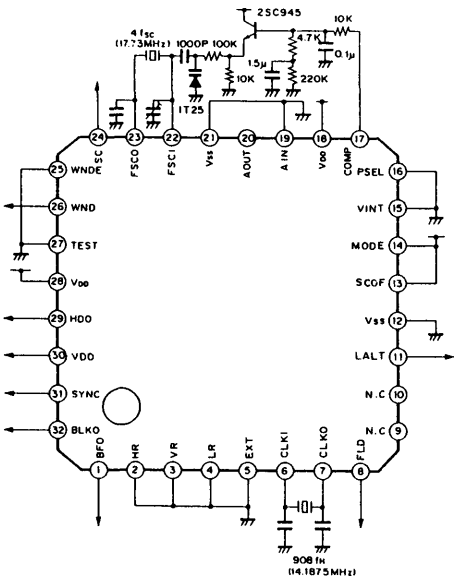
NTSC (Internal mode)



PAL (Filter configuration 2, Internal mode)



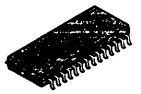
PAL (Filter configuration 1, Internal mode)



SONY CXD1217M

Synchronizing Signal Generator for Video Camera

28 pin SOP (Plastic)



Description

The CXD1217M is a synchronizing signal generator for color video cameras.

Features

- Compatible with the respective systems, NTSC, PALM, PAL and SECAM
- Output is synchronized with the clock of $910f_H$ or $908f_H$
- 25Hz offset processing by PAL system
- Color framing by the respective systems, NTSC, PALM and PAL
- Possible external synchronization by H reset, V reset and line-switchover reset pins

Applications

Synchronizing signal generator for color video cameras.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

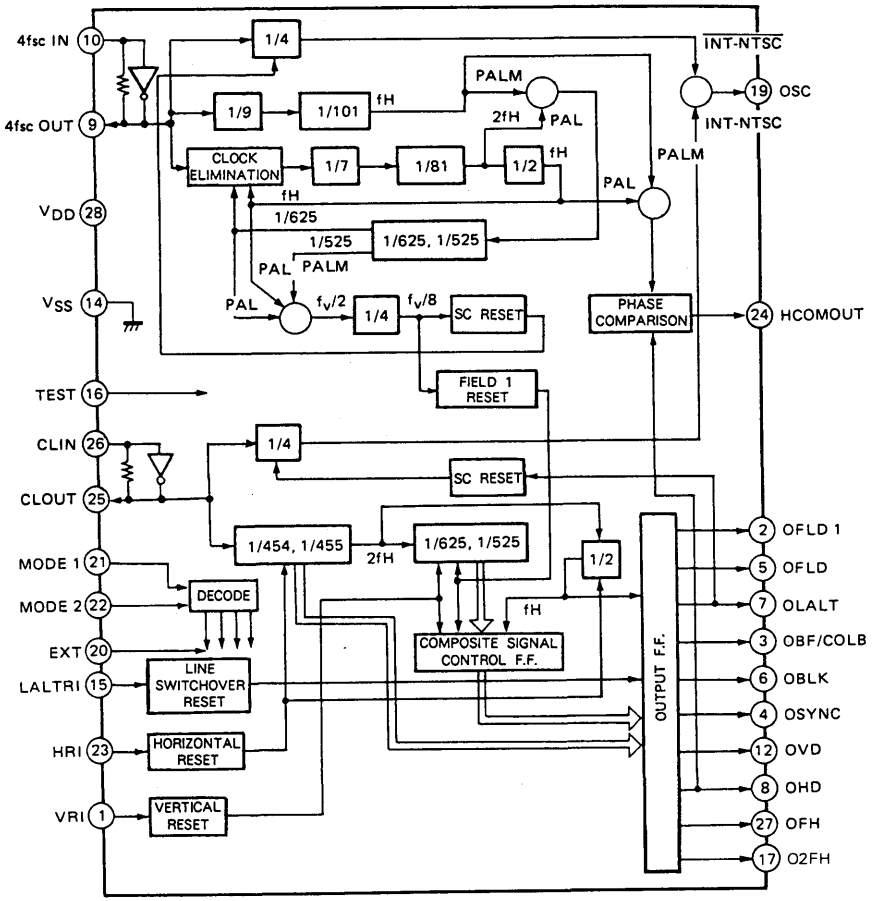
• Supply voltage	V_{DD}	Vss − 0.5 to + 7.0	V
• Input voltage	V_I	Vss − 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	Vss − 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	− 20 to + 75	°C
• Storage temperature	Tstg	− 55 to + 150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	− 20 to + 75	°C

E89626 – ST

Block Diagram and Pin Configuration



Note : Pin 19 output is (a) a signal based on Pin 26 in INT mode at NTSC.
(b) each signal is based on Pin 10 in other modes.

Pin Description

Pin No.	Symbol	I/O	Description
1	VRI	I	Vertical reset signal
2	OFLD1	O	First field output
3	OBF/COLB	O	Burst flag/color blanking output
4	OSYNC	O	Composite sync output
5	OFLD	O	Even and Odd output
6	OBLK	O	Composite blanking output
7	OLALT	O	Line alternate output
8	OHD	O	Horizontal drive output
9	4fscOUT	O	4fsc output
10	4fscIN	I	4fsc input
11	NC	—	
12	OVD	O	Vertical drive output
13	NC	—	
14	Vss	—	GND pin
15	LALTRI	I	Line alternate reset input
16	TEST	I	Test input
17	O2FH	O	$2f_H$ output (Double the frequency of Pin 27)
18	NC	—	
19	OSC	O	Sub carrier output
20	EXT	I	Internal and external synchronizing modes switchover L : Internal synchronization H : External synchronization
21	MODE1	I	System selecting input 1
22	MODE2	I	System selecting input 2
23	HRI	I	Horizontal reset input
24	HCOMOUT	O	Phase comparator output
25	CLOUT	O	Clock output
26	CLIN	I	Clock input
27	OFH	O	Horizontal frequency output
28	V_{DD}	—	Power supply pin

Electrical Characteristics

DC characteristics

(V_{DD} = 5V ± 10%, Vss = 0V, Topr = − 20 to + 75℃)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage 1	V_{OH}	I_{OH} = − 2mA	V_{DD} − 0.5		V_{DD}	V
	V_{OL}	I_{OL} = 4mA	Vss		0.4	V
Output voltage 2*1	V_{OH}	I_{OH} = − 4mA	V_{DD} − 0.5		V_{DD}	V
	V_{OL}	I_{OL} = 4mA	Vss		0.4	V
Output voltage 3*2	V_{OH}	I_{OH} = − 4mA	$V_{DD}/2$			V
	V_{OL}	I_{OL} = 8mA			$V_{DD}/2$	V
Input voltage	V_{IH}		0.7V_{DD}			V
	V_{IL}				0.3V_{DD}	V
Input current*3 (Pull-down pin)	I_{IH}	V_{IH} = V_{DD}	20	50	120	μA
Output leak current*1	I_{LZ}	At high impedance		± 30		nA
Power current supply	I_{DD}	At output pin in no-load		8		mA
Feedback resistance*4	R_{FB}	V_{DD} = 5V	250k		2.5M	Ω

*1 HCOMOUT pin
*2 4fscOUT and CLOUT pins
*3 LALTRI, TEST, EXT, MODE1 and MODE2 pins
*4 4fscOUT, 4fscIN, CLOUT and CL IN pins

I/O capacitance

(V_{DD} = V_I = 0V, f_M = 1 MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin	C_{IN}		—	—	9	pF
Output pin	C_{OUT}		—	—	11	pF

Description of Operation (See Block Diagram.)

The CXD1217 is applicable to 4 systems ; namely, NTSC, PAL, PALM and SECAM. In order to realize them, the following relative equations of Sub-carrier (4fscIN) and Clock (CLIN) are adopted.

	Sub carrier	Clock
NTSC	4fsc = 910fH	910fH
PAL	4fsc = 1135fH + 2fv	908fH
PALM	4fsc = 909fH	910fH
SECAM	———	908fH

As it is obvious from the above equations, the 4fsc and clock frequency do not coincide with each other in the PAL and PALM. Therefore matching of the clock frequency is carried out by providing PLL.

1. MODE specified input

The CXD1217 provides 4 inputs to specify the respective modes.

* EXT input : Set this pin to V_{DD} side, and it becomes into external synchronizing mode. At this time, the counters in connection with the PLL loop as shown in the upper part of the block diagram become into stand still state.

* MODE1 and MODE2 inputs : These are inputs for the system selection.

MODE1	MODE2	System
0	0	NTSC
0	1	SECAM
1	0	PALM
1	1	PAL

"0" → V_{SS}
"1" → V_{DD}

* TEST input : An input to be used to measure IC. This input is normally kept opened. (Because it is dropped internally to Vss with MOS resistance.)

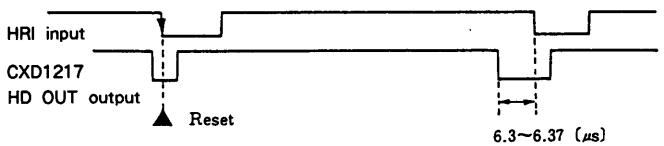
2. Reset operation

The CXD1217 has three reset inputs ; namely, HRI, VRI, LALTRI, and it works to perform reset operation when it detects falling edge. These three inputs are so designed as to take in synchronization with the IC internal clock. Therefore, it is a prerequisite that both systems should have clock frequencies that are matched as a reset operation to each other (GEN locked).

* H reset (HRI input)

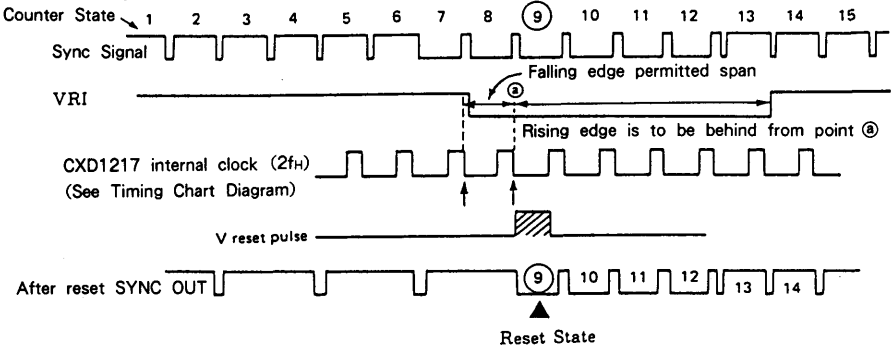
When the HRI input is continuous with H synchronization, resetting is activated with the initial falling edge, and for the subsequent edges they do not have to be reset unless they are deviated more than 2-bit (140ns) against the initial edge in the internal clock. That is, if the jitter of HRI input is less than 140ns, it is absorbed. The minimum resetting pulse width is over 0.3 µs.

The phase to be reset is the advanced point of 6.3 to 6.37 µs (=90 to 91-bit X 70ns) than the HRI input as shown in the diagram below.



• V reset (VRI input)

When the VRI is input as shown in figure below, OSYNC can be reset at the same phase with the SYNC signal.



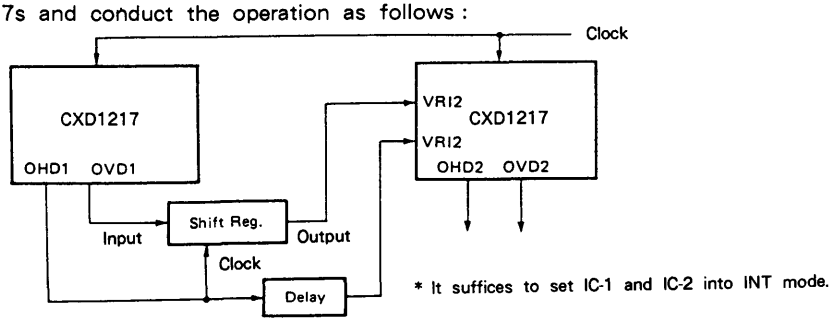
Since the falling edge point in the diagram above (marked with ↑) is the boundary of reset, if the falling edge of the VRI input traverses that point, it causes 1/2H deviation to the reset state.

Accordingly, if resetting is applied between two similar systems whose frequency are different, the V to which resetting is applied generates jitter of 1/2H. (When the resetting is applied continuously.)

• LALT reset (LALTRI input)

Phase relation between LALTRI pulse polarity and 2FH is the same as in the case of V resetting.

Resetting operation is basically required only in the external synchronizing mode (GEN LOCK mode). However, even in the internal synchronizing mode, it sometimes requires H and V outputs whose phases are deviated against a certain output. In that case, it suffices to use two CXD1217s and conduct the operation as follows :



By varying the Delay and Shift Reg. of the above diagram, any phases of OHD2 and OVD2 can be provided against the respective OHD1 OVD1.

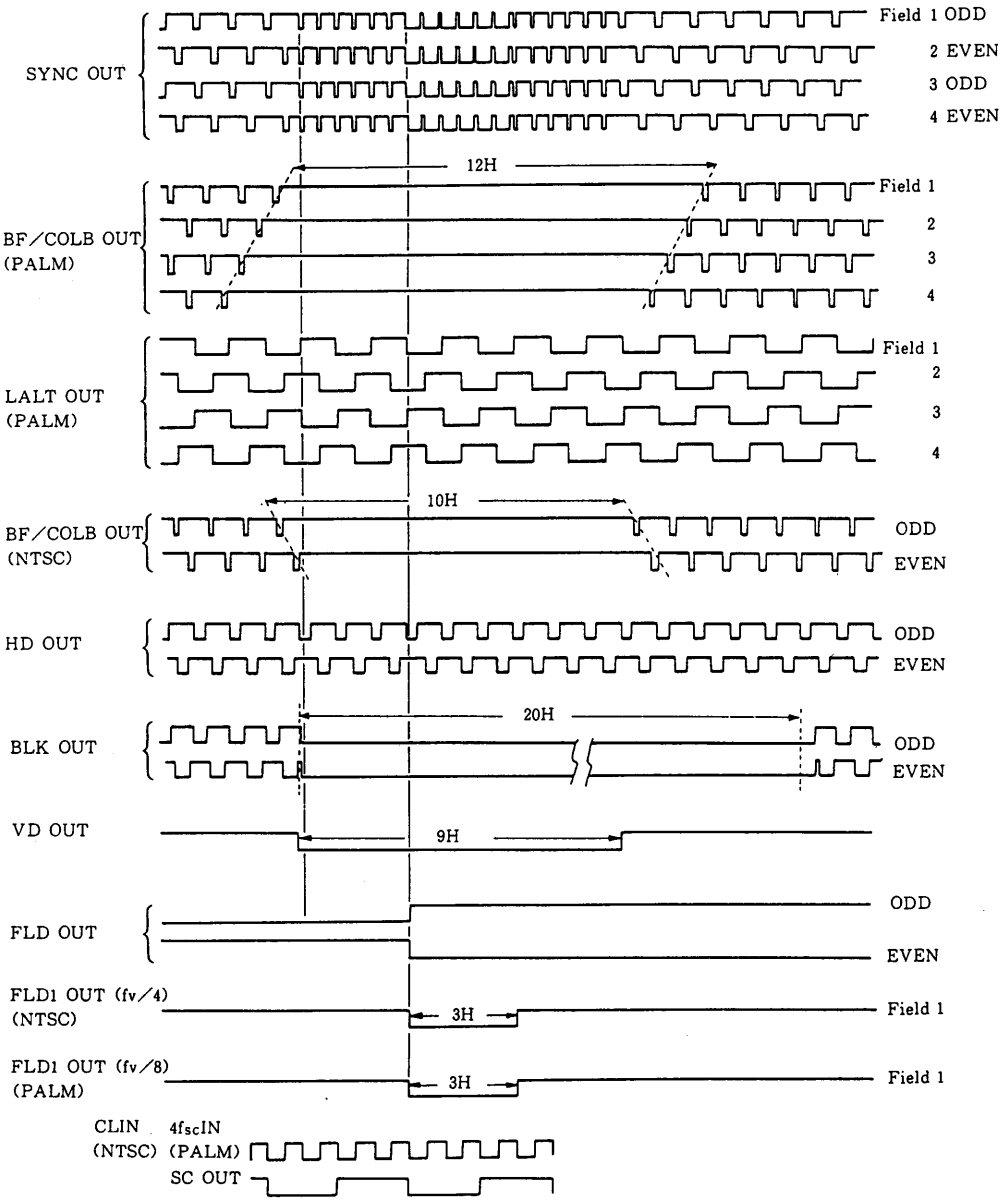
3. Color framing

In the case of internal synchronization in the individual NTSC, PAL and PALM systems, the phase relationships between SYNC of the 1st field and sub-carrier are kept stable regardless of the power supply being ON or OFF. However, as the PAL and PALM systems are comprised of PLL, the absolute values concerning the phase according to variation of the ambient temperature drifts.

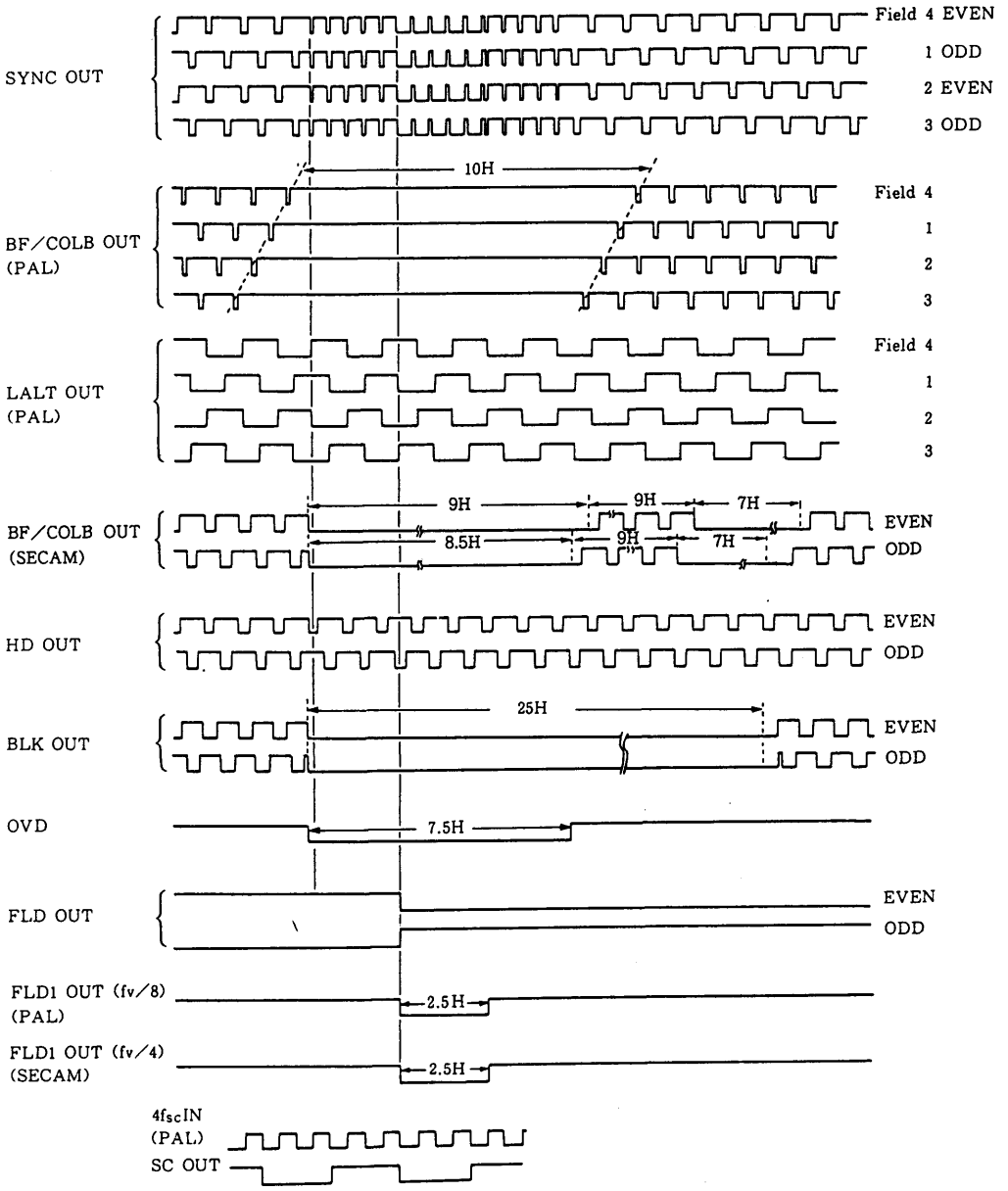
Timing Chart

Output Timing Chart Diagram

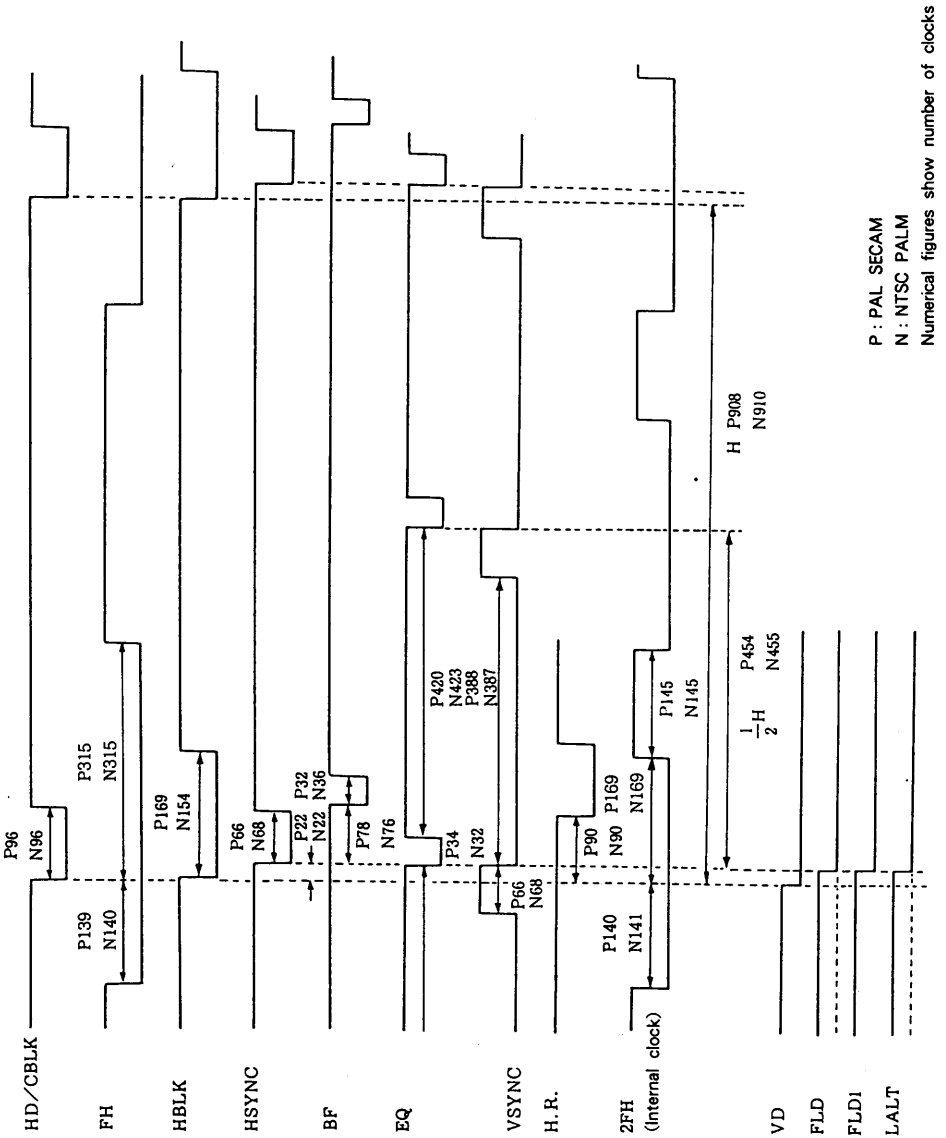
CXD1217 NTSC, PALM



CXD1217 PAL, SECAM



CXD1217 fH

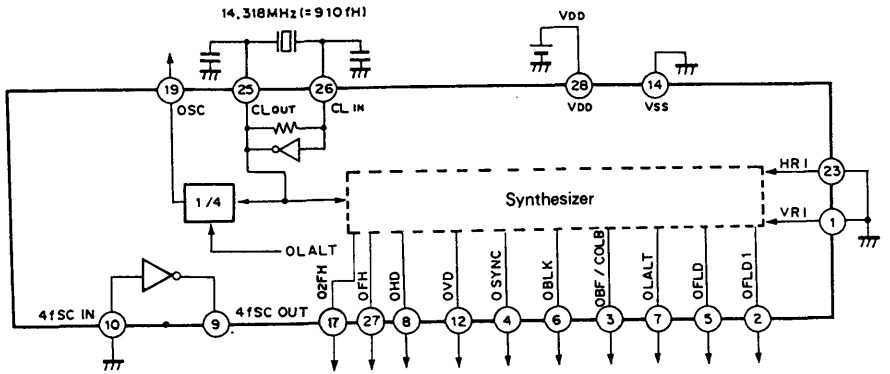

HD/CBLK
FH
HBLK
HSYNC
BF
EQ
VSYNC
H.R.
2FH (Internal clock)
VD
FLD
FLD1
LALT
P96
N96
P139
N140
P315
N315
P169
N154
P66
N68
P22
N22
P32
N36
P78
N76
P34
N32
P66
N68
P420
N423
P388
N387
P140
N141
P90
N90
P169
N169
P145
N145
1/2H
P454
N455
H P908
N910
P : PAL SECAM
N : NTSC PALM
Numerical figures show number of clocks

Application Circuit

Basic connection in individual systems

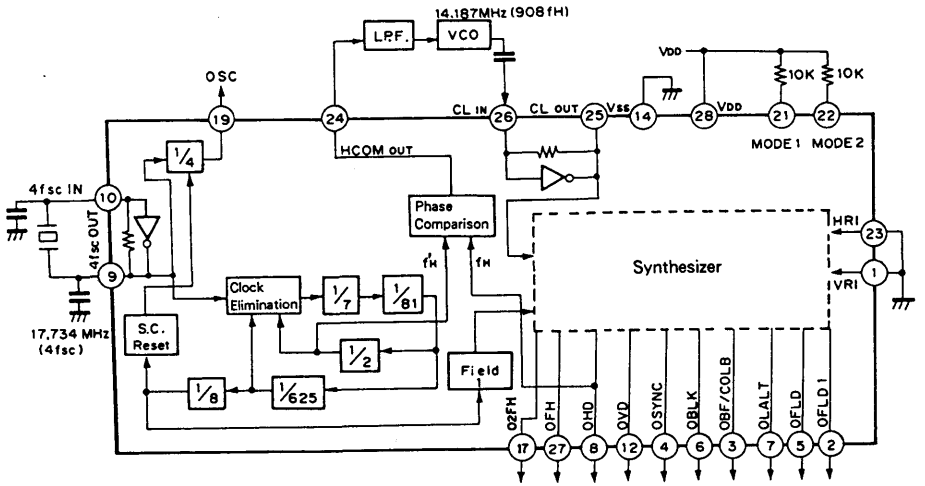
Basic connection in individual systems at internal synchronization mode (EXT input = "0") is as follows. See waveform diagram for each output.

• NTSC



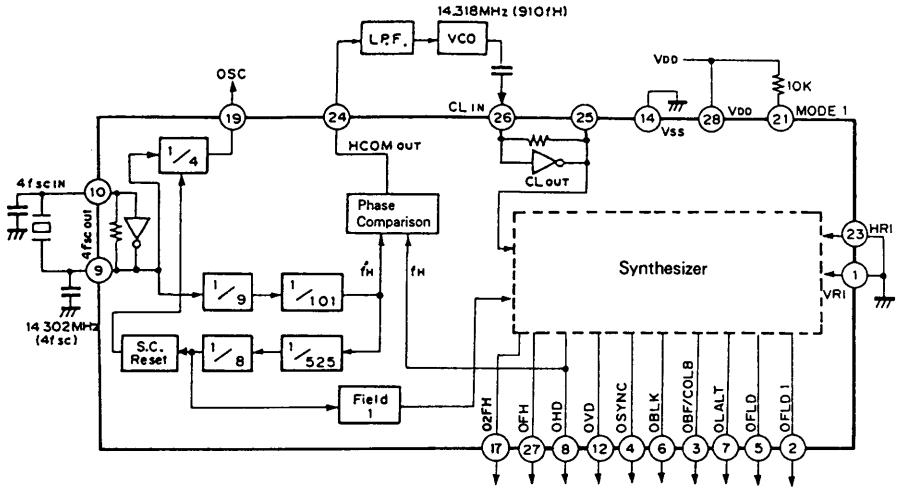
* H/2 is output for LALT OUT even in NTSC mode.
* MODE1, MODE2, EXT, TEST and LALTRI pins can be kept open.
  (If noise annoys, connect to Vss by low impedance.)

• PAL



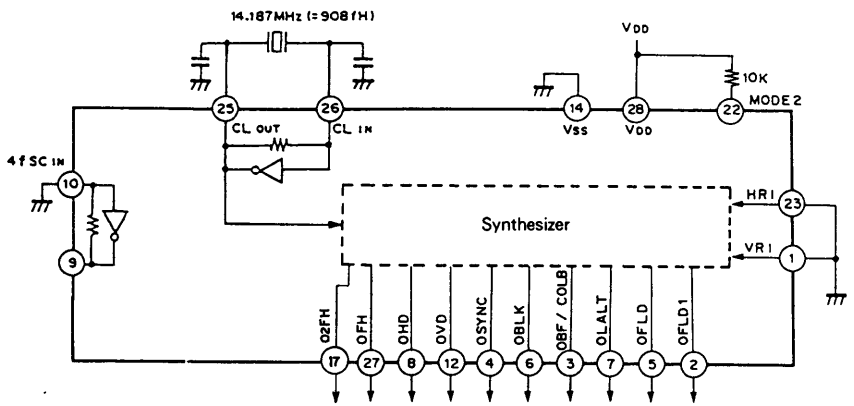
* Inverter of CL_{IN} or CL_{OUT} pins are usable as VCO.

• PALM



* Internal inverter is usable as VCO.

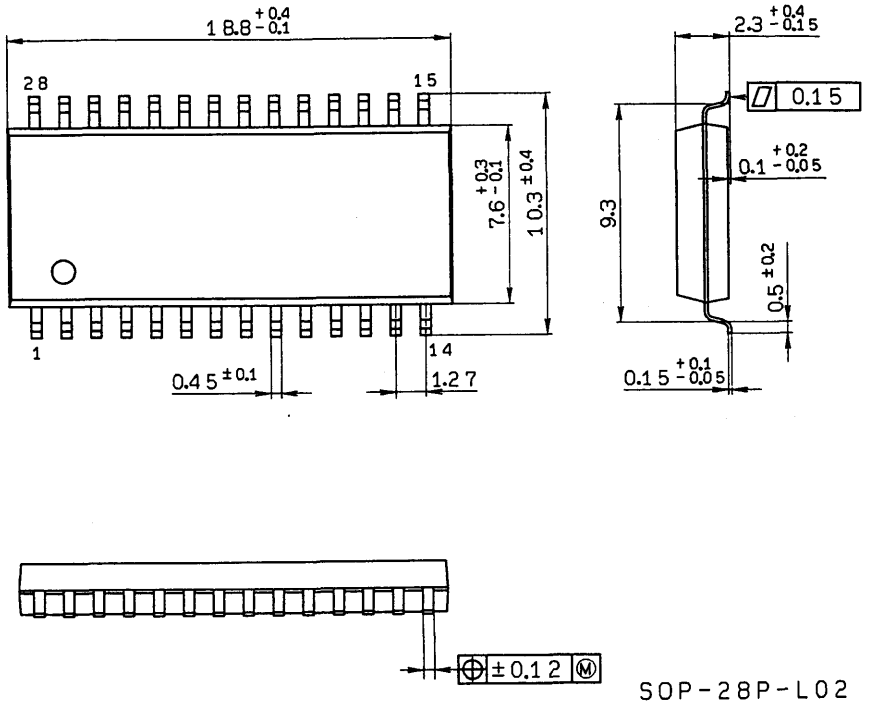
• SECAM



* COLB is output to BF/COLB OUT pin.
* S_{DR} and S_{DB} are formed in PLL using 908f_H.

Package Outline Unit : mm

28 pin SOP (Plastic) 375mil 0.6g



SOP-28P-L02

SONY CX23047B

CCD Camera Scanning System Timing Signal Generator

Description

CX23047B has been developed as a CMOS type LSI to be used for the scanning system for both imagers of ICX018CK/CL(NTSC), and ICX021CK/CL(CCIR), and displays the following functions by using together with CX-7930A (synchronized signal generator).

Features

- Generates imagers (ICX018CK/CL and ICX021CK/CL) drive pulses.
- Generates signal processing pulses for color and B & W cameras.
- Switchover of NTSC/CCIR modes is possible.
- Correction of defect of 1 picture element of every 1H of imager is possible. (external ROM is appended)

Structure

Silicon gate CMOS

Absolute Maximum Ratings (Ta=25°C, Vss=0V)

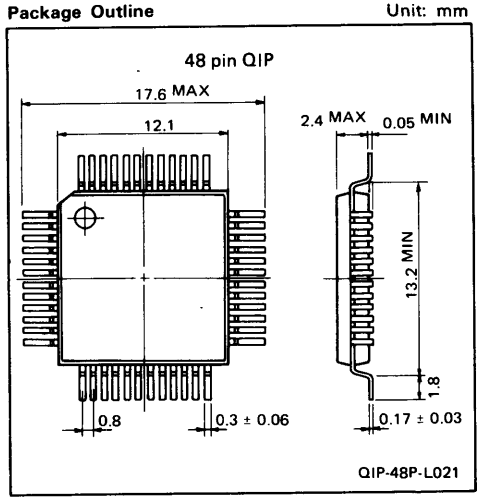
• Supply voltage	V_{DD}	$V_{SS}-0.5$ to 7.0	V
• Input voltage	V_I	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Output voltage	V_O	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Recommended Operating Conditions

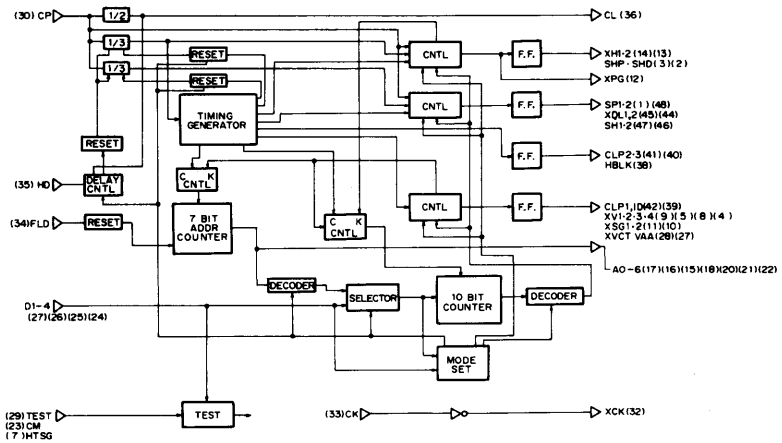
• Supply voltage	V_{DD}	4.5	to 5.5	V
• Operating temperature	Topr	−20	to +75	°C

Package Outline

Unit: mm

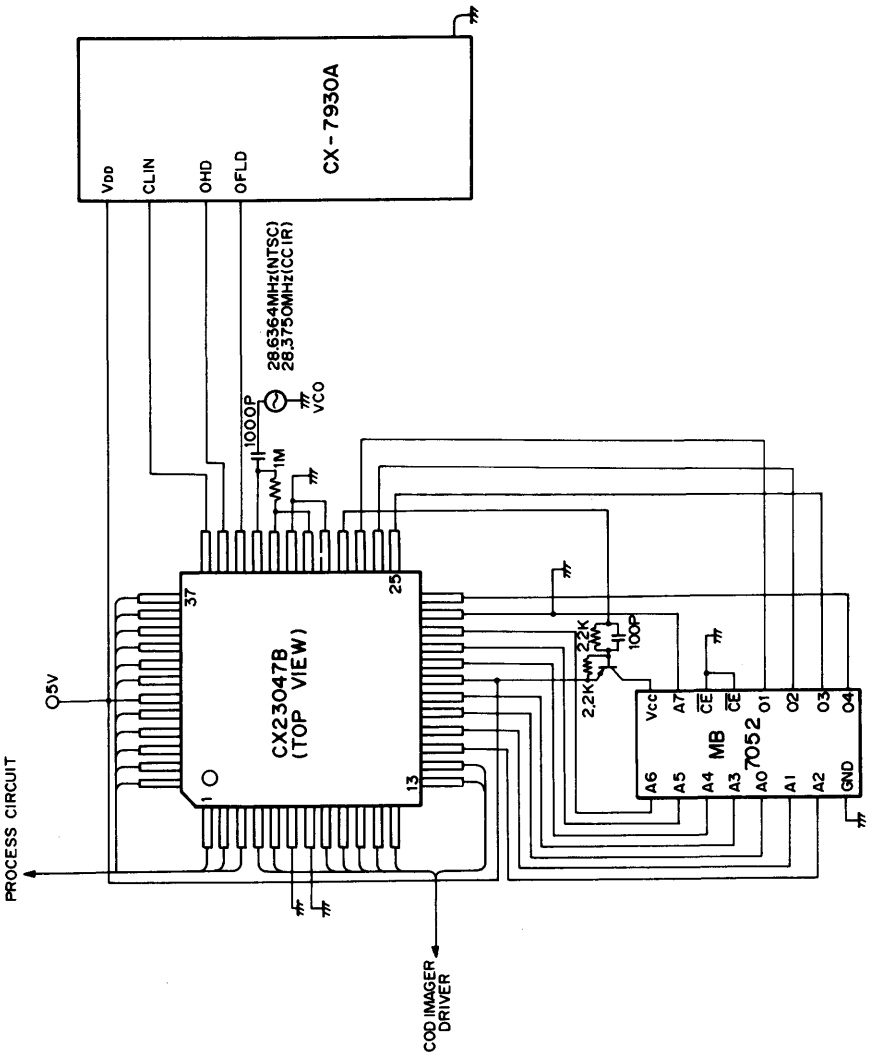


Block Diagram

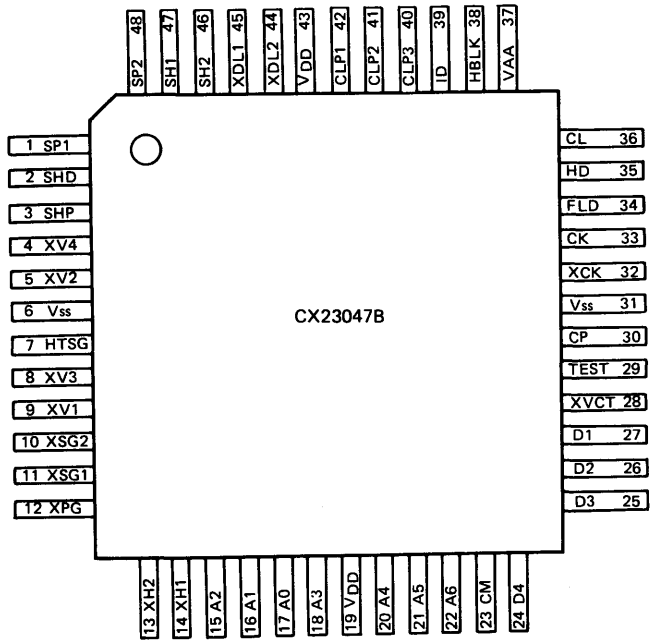


60963-ST

Application Circuit



Pin Configuration (Top View)

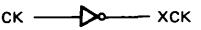


Pin Number and Name

No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol
1	O	SP1	13	O	XH2	25	I	D3	37	O	VAA
2	O	SHD	14	O	XH1	26	I	D2	38	O	HBLK
3	O	SHP	15	O	A2	27	I	D1	39	O	ID
4	O	XV4	16	O	A1	28	O	XVCT	40	O	CLP3
5	O	XV2	17	O	A0	29	I	TEST	41	O	CLP2
6	P*	Vss	18	O	A3	30	I	CP	42	O	CLP1
7	I	HTSG	19	P*	VDD	31	P*	Vss	43	P*	VDD
8	O	XV3	20	O	A4	32	O	XCK	44	O	XDL2
9	O	XV1	21	O	A5	33	I	CK	45	O	XDL1
10	O	XSG2	22	O	A6	34	I	FLD	46	O	SH2
11	O	XSG1	23	I	CM	35	I	HD	47	O	SH1
12	O	XPG	24	I	D4	36	O	CL	48	O	SP2

* P: power source

Pin Description

No.	Symbol	I/O	Description
4, 5, 8, 9	XV1 to XV4	O	Imager driving pulse. Add inverse shape driver and drive CCD imagers (ICX-018 and ICX-021).
10, 11	XSG1, 2	O	
12	XPG	O	
13, 14	XH1, 2	O	
15 to 18 20 to 22	A0 to A6	O	Address output for external ROM. A6 is MSB.
23	CM	I	Test pin. Normally GND.
24 to 27	D4 to D1	I	External ROM input pin. When external ROM is not used, mode setting is possible by pulling up or pulling down. When ROM is not used: D1 . . . always GND D2 . . . GND: monochrome mode, Vcc: color mode D3 . . . always Vcc D4 . . . GND: CCIR, Vcc: NTSC
28	XVCT	O	ROM (MB7052) power supply switching pulse. When performing switching, it is necessacy to add PNP transistor.
29	TEST	I	Test pin. Normally GND.
30	CP	I	Clock input. NTSC: 28.6364 MHz, CCIR: 28.3750 MHz
32	XCK	O	Inverter circuit 
33	CK	I	
34, 35	FLD, HD	I	Synchronizing signal input. It is taken in by trailing of CL (Pin 36).
36	CL	O	Clock output for SYNC generator (CX-7930A). Half the frequency of CP
37	VAA	O	Vertical effective sphere of CCD imager output. Used together with CLP1 in the clamping circuit.
38	HBLK	O	Horizontal effective sphere of CCD imager output. Used for pre-blanking.
39	ID	O	R/B lines discriminating signal. B line . . . "H", R line . . . "L"
40, 41	CLP2, 3	O	Clamping pulse. Continuous pulse.
42	CLP1	O	Clamping pulse. CCD output optical black section clamping pulse.
44, 45	XDL1, 2	O	1H delay line (CX23039) driving pulse.
46, 47	SH1, 2	O	Sample hold pulse for 1H delay line (CX23039).
48, 1	SP1, 2	O	Sample hold pulse for color separation. Possesses defect correction function.
2	SHD	O	Sample hold pulse for imager output. Possesses defect correction function.
3	SHP	O	Pulse to sample hold the pre-charge level of imager output.
7	HTSG	I	Test pin. Normally GND.
6, 31	Vss	I	Ground pin.
19, 43	VDD	I	+5V power source pin.

Electrical Characteristics

DC characteristics

V_{DD} =5V ± 10% Vss = 0V,
Topr = −20 to +75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current		I_{DDS}	Static state*	0		0.02	mA
Output voltage	H level	V_{OH}	I_{OH} = −0.4 mA	V_{DD} −0.5		V_{DD}	V
	L level	V_{OL}	I_{OL} = 3.2 mA	Vss		0.4	V
Input voltage	H level	V_{IH}		2.2			V
	L level	V_{IL}				0.8	V
Input leakage current		I_{LI}		−5		5	μA

*Note) V_{IH} = V_{DD}, V_{IL} = Vss

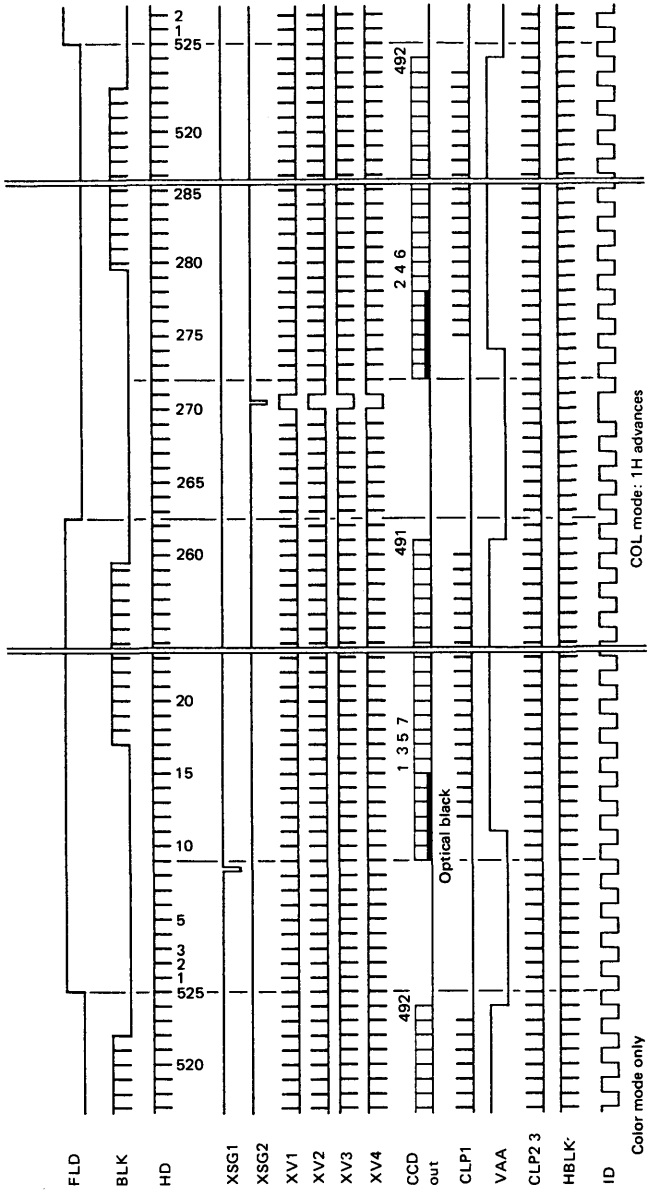
I/O Capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			12	pF
Output pin	C_{OUT}			12	pF

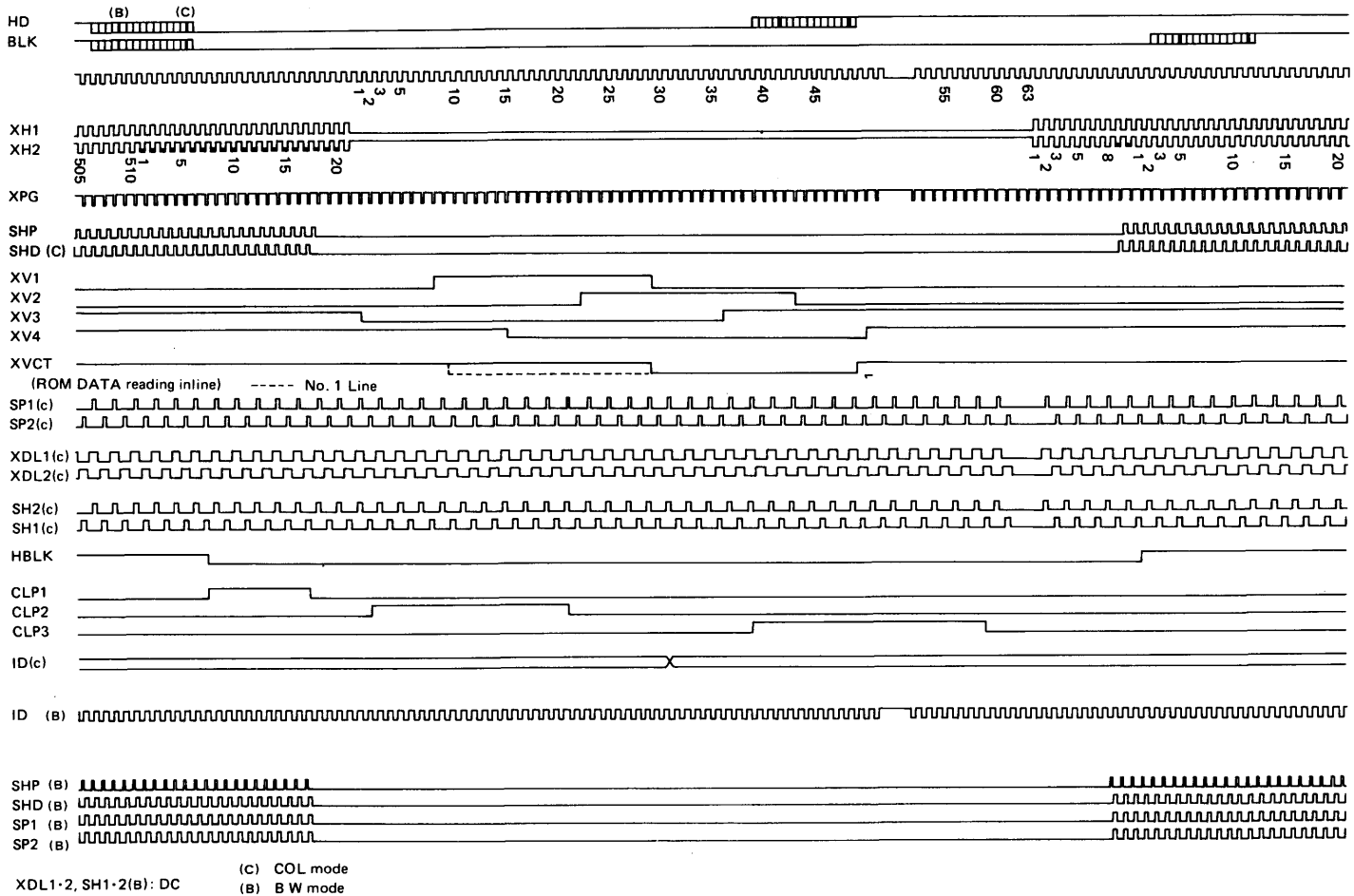
Test condition: V_{DD} = V_I = 0V, f_M = 1 MHz

Timing Chart

1. (NTSC BW ROM OFF)



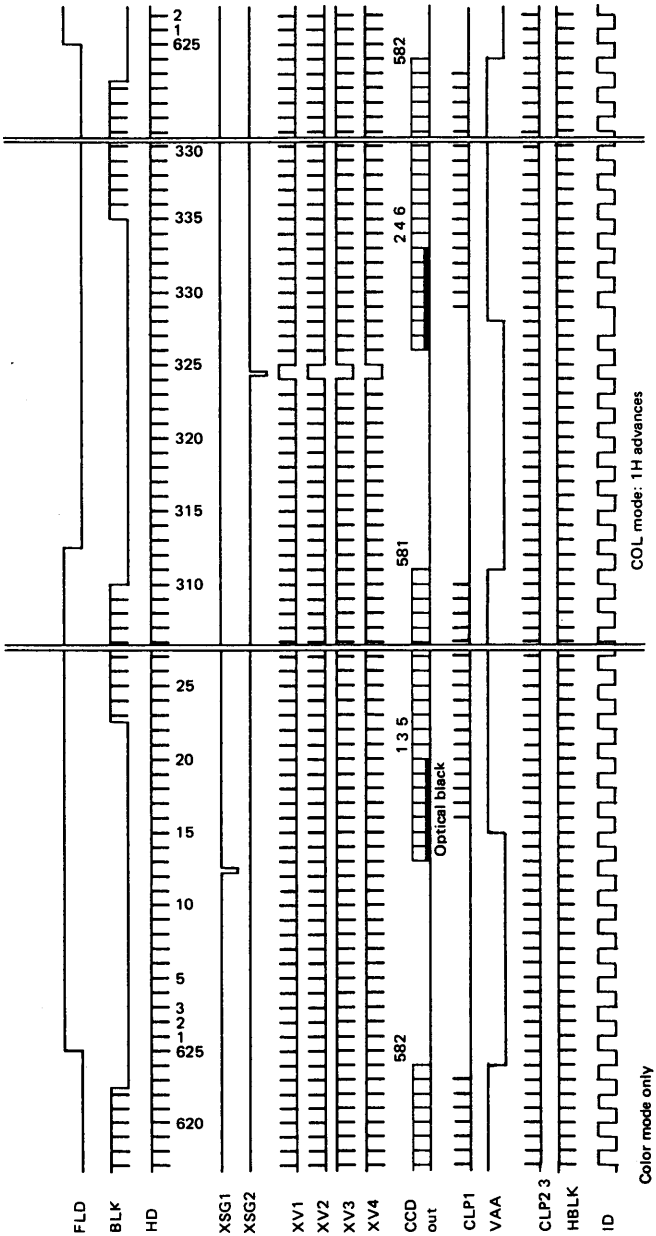
2. (NTSC ROM OFF)



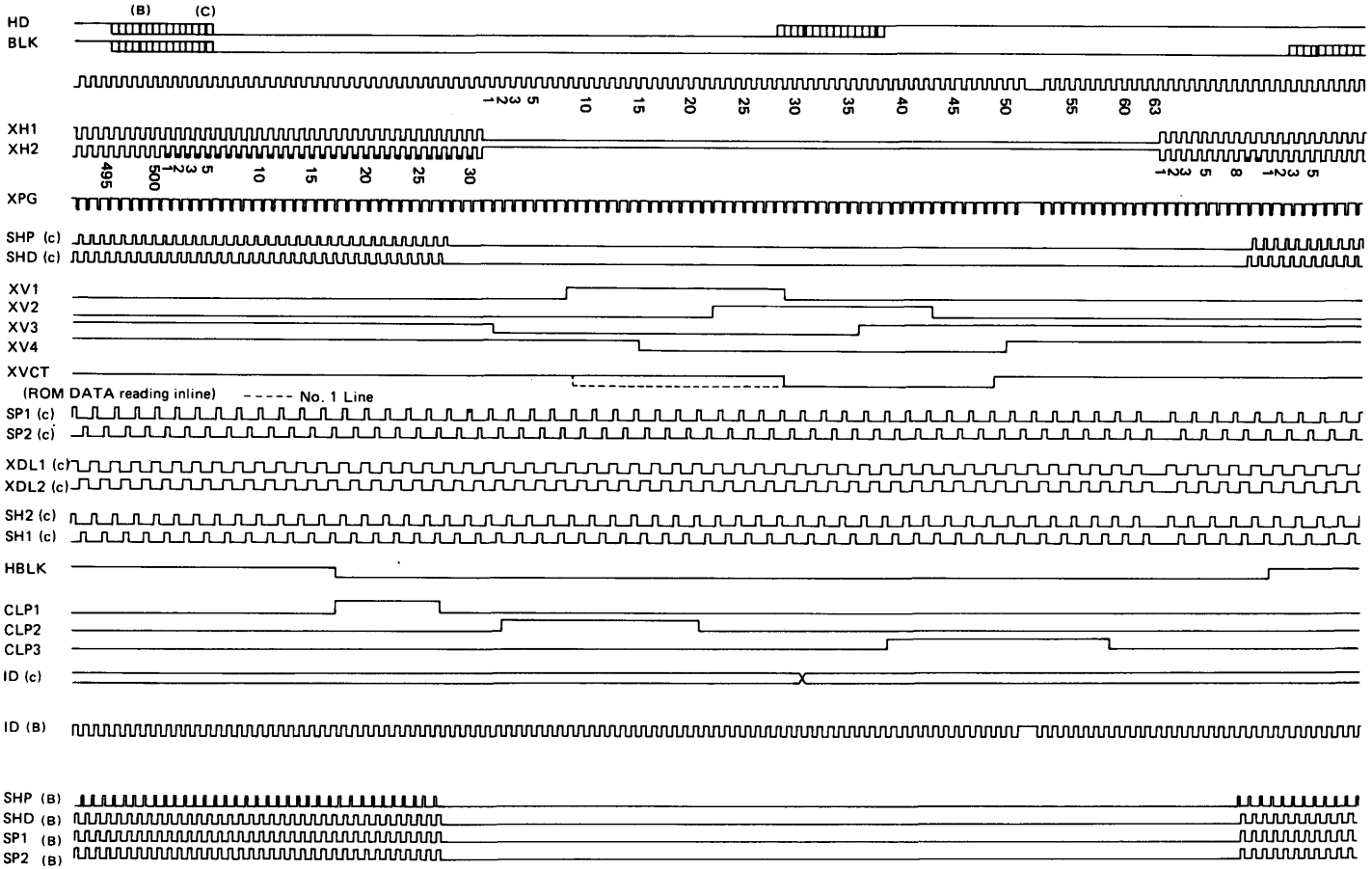
SONY®

CX23047B

3. (CCIR.B/W.ROM OFF)



4. (CCIR ROM OFF)



XDL12 SH12(B): DC

(C) COL mode

(B) B W mode

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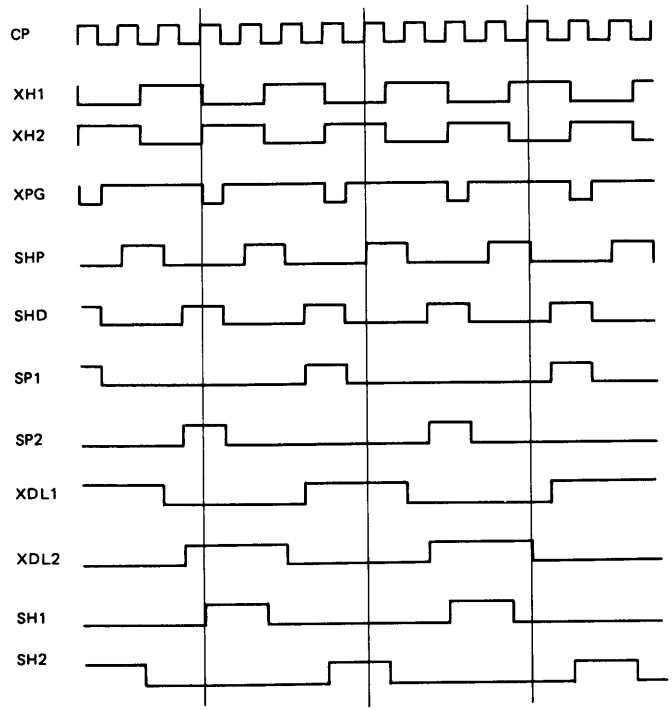
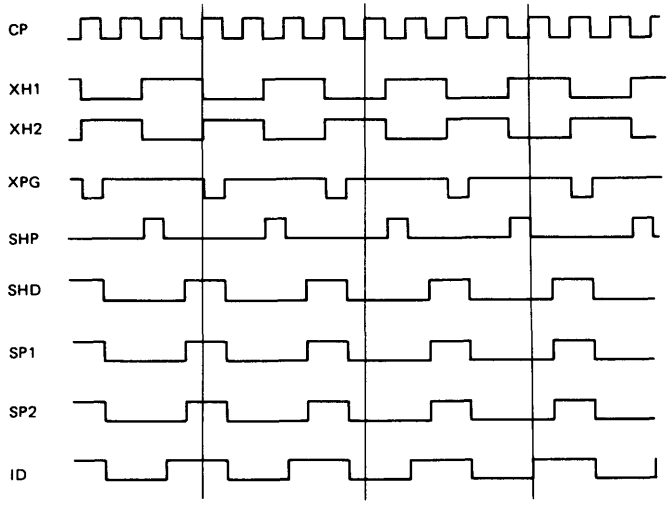
CX23047B

5. (C·L·ROM OFF)



6. (B/W.ROM OFF)



SONY®

CXD1035BQ-Z

CCD Camera Scanning System Timing Signal Generator

48pin QFP (Plastic)

Description

CXD1035BQ-Z is a CMOS type LSI developed for use with the scanning system of both ICX022AK (NTSC) and ICX024AK (PAL).

This IC is employed in conjunction with either CXD1030M or CXD1158M (synchronized signal generator).

Features

- Generates drive pulses for imagers (ICX022AK, ICX024AK).
- Generates signal processing pulse for color cameras.
- Switchover of NTSC/PAL modes is possible.
- Blemish compensation is possible (through usage of external ROM).

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=25°C, Vss=0V)

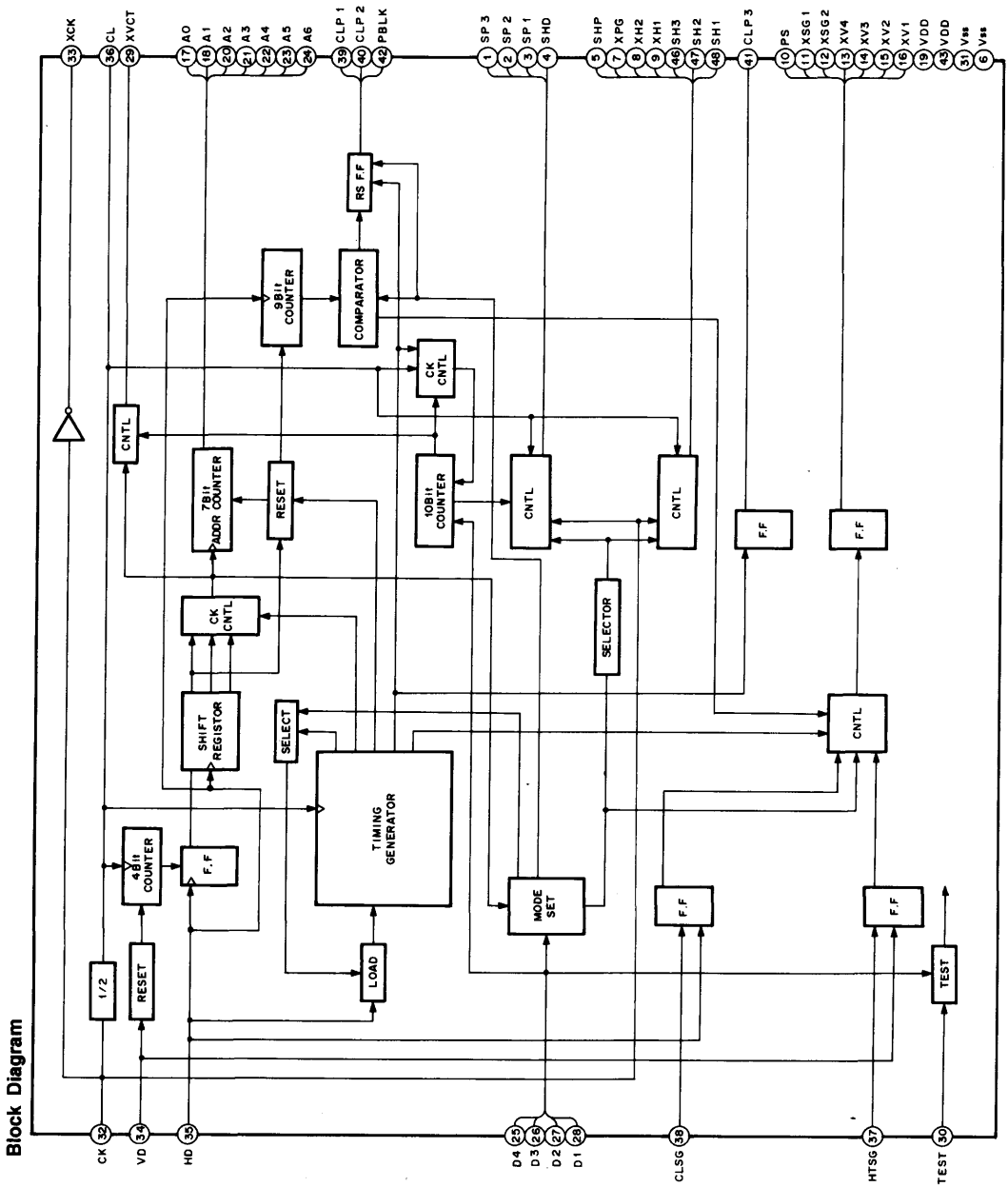
• Supply voltage	V_{DD}	Vss–0.5	to	6.0	V
• Input voltage	V_I	Vss–0.5	to	V_{DD}+0.5	V
• Output voltage	V_O	Vss–0.5	to	V	V
• Operating temperature	Topr	–25	to	+85	°C
• Storage temperature	Tstg	–40	to	+125	°C
• Allowable power dissipation	P_D		500		mW

Recommended Operating Conditions

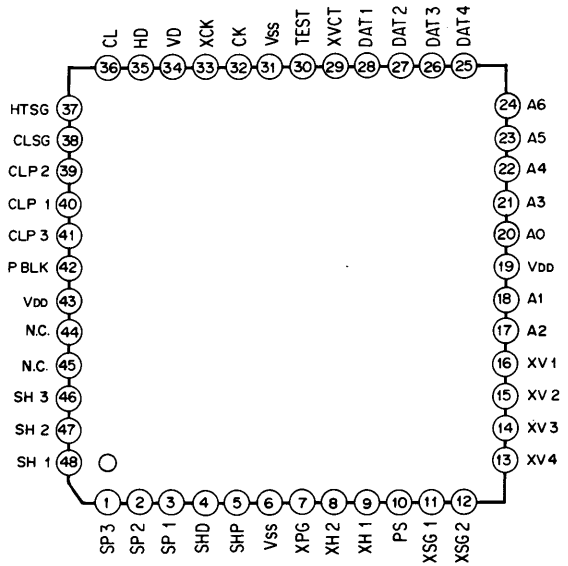
• Supply voltage	V_{DD}	4.75	to	5.25	V
• Operating temperature	Topr	–20	to	+75	°C

E89Z23-YA

Block Diagram



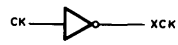
Pin Configuration (Top View)



Pin Name

No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol	No.	I/O	Symbol
1	O	SP3	13	O	XV4	25	I	DAT4	37	I	HTSG
2	O	SP2	14	O	XV3	26	I	DAT3	38	I	CLSG
3	O	SP1	15	O	XV2	27	I	DAT2	39	O	CLP2
4	O	SHD	16	O	XV1	28	I	DAT1	40	O	CLP1
5	O	SHP	17	O	A2	29	O	XVCT	41	O	CLP3
6	–	Vss	18	O	A1	30	I	TEST	42	O	PBLK
7	O	XPG	19	–	VDD	31	–	Vss	43	–	VDD
8	O	XH2	20	O	A0	32	I	CK	44	–	N.C.
9	O	XH1	21	O	A3	33	O	XCK	45	–	N.C.
10	O	PS	22	O	A4	34	I	VD	46	O	SH3
11	O	XSG1	23	O	A5	35	I	HD	47	O	SH2
12	O	XSG2	24	O	A6	36	O	CL	48	O	SH1

Pin Description

Symbol	I/O	Description
XV1 to XV4	O	Drive pulses for the imagers (ICX022, ICX024) through CCD drivers.
XSG1, 2	O	
XPG	O	
XH1, 2	O	
A0 to A6	O	Address output for external ROM. A6 is MSB.
D4 to D1	I	External ROM data input pin.
XVCT	O	ROM (MB7144) power supply switching pulse.
TEST	I	Test pin. Normally GND.
CK	I	Clock input. NTSC : 28.6364 MHz PAL : 28.3750 MHz
XCK	O	CK inversion output 
VD, HD	I	Synchronizing signal input. Latched by falling edge of CL (Pin 36).
CL	O	Clock output for synchronized signal generator. Half CK's frequency.
PBLK	O	Horizontal and vertical effective area of CCD imager output. Used for pre-blanking.
PS	O	Power save for V driver IC.
CLP1, 2, 3	O	Clamping pulse.
SH1, 2, 3	O	Sampling pulse for signal processor.
SP1, 2, 3	O	Sampling pulse for color separation.
SHD	O	Sampling pulse for imager output signal.
SHP	O	Sampling pulse for pre-charge level.
HTSG, CLSG	I	Test pin. Nomrally GND.
V_{SS}	I	Ground pin.
V_{DD}	I	+5V power supply pin.

Electrical Characteristics

DC characteristics

V_{DD}=5V±5%, V_{SS}=0V, Topr=20 to +75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current		I_{DDS}	Static state*	0		0.1	mA
Input voltage	H level	V_{OH}	I_{OH} = –0.4 mA	4.2		V_{DD}	V
	L level	V_{OL}	I_{OL} = 3.2 mA	V_{SS}		0.4	V
Output voltage	H level	V_{IH}		2.4			V
	L level	V_{IL}				0.8	V
Input leakage current		I_{LI}	V_I = 0V to V_{DD}	–10		+10	µA

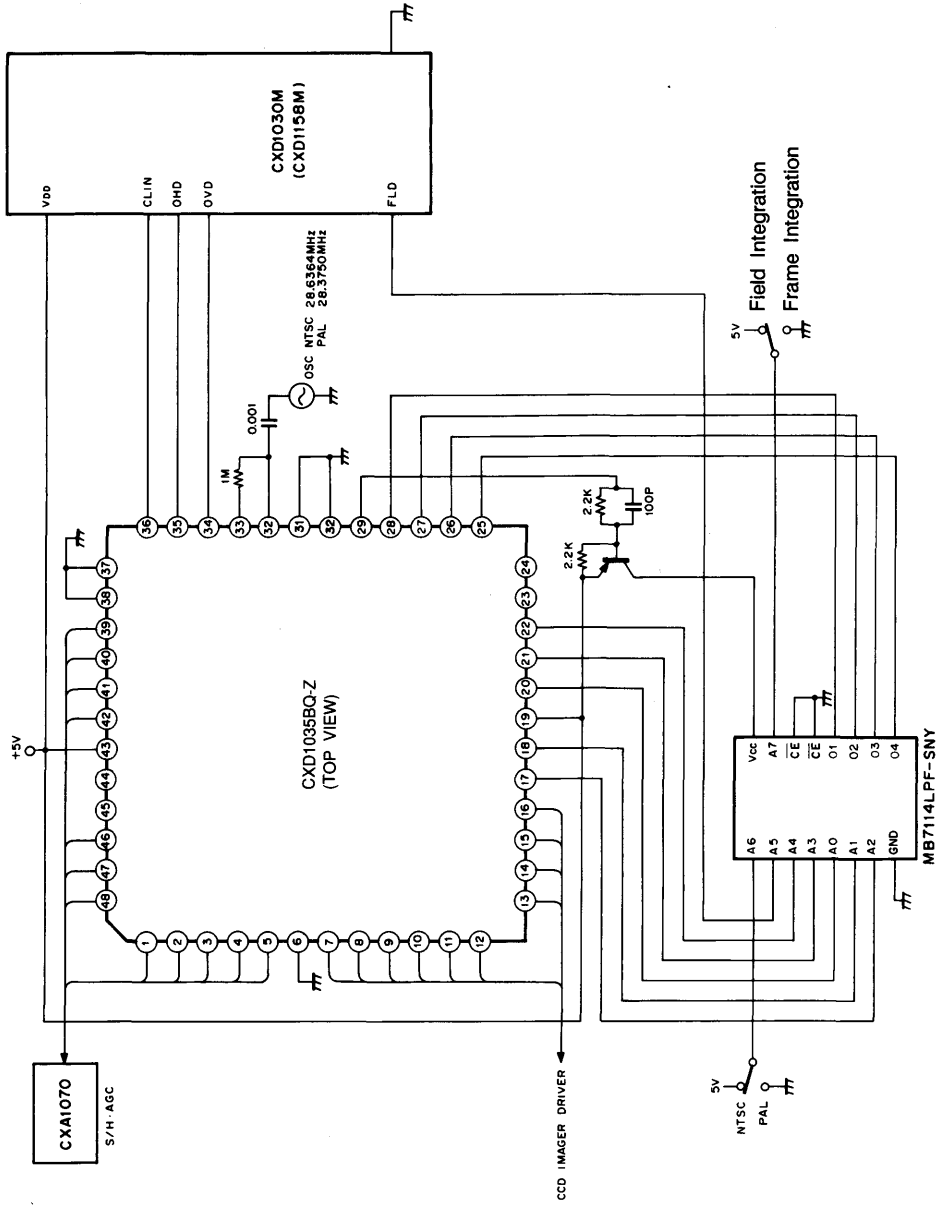
* **Note)** V_{IH} = V_{DD}, V_{IL} = V_{SS}

I/O characteristics

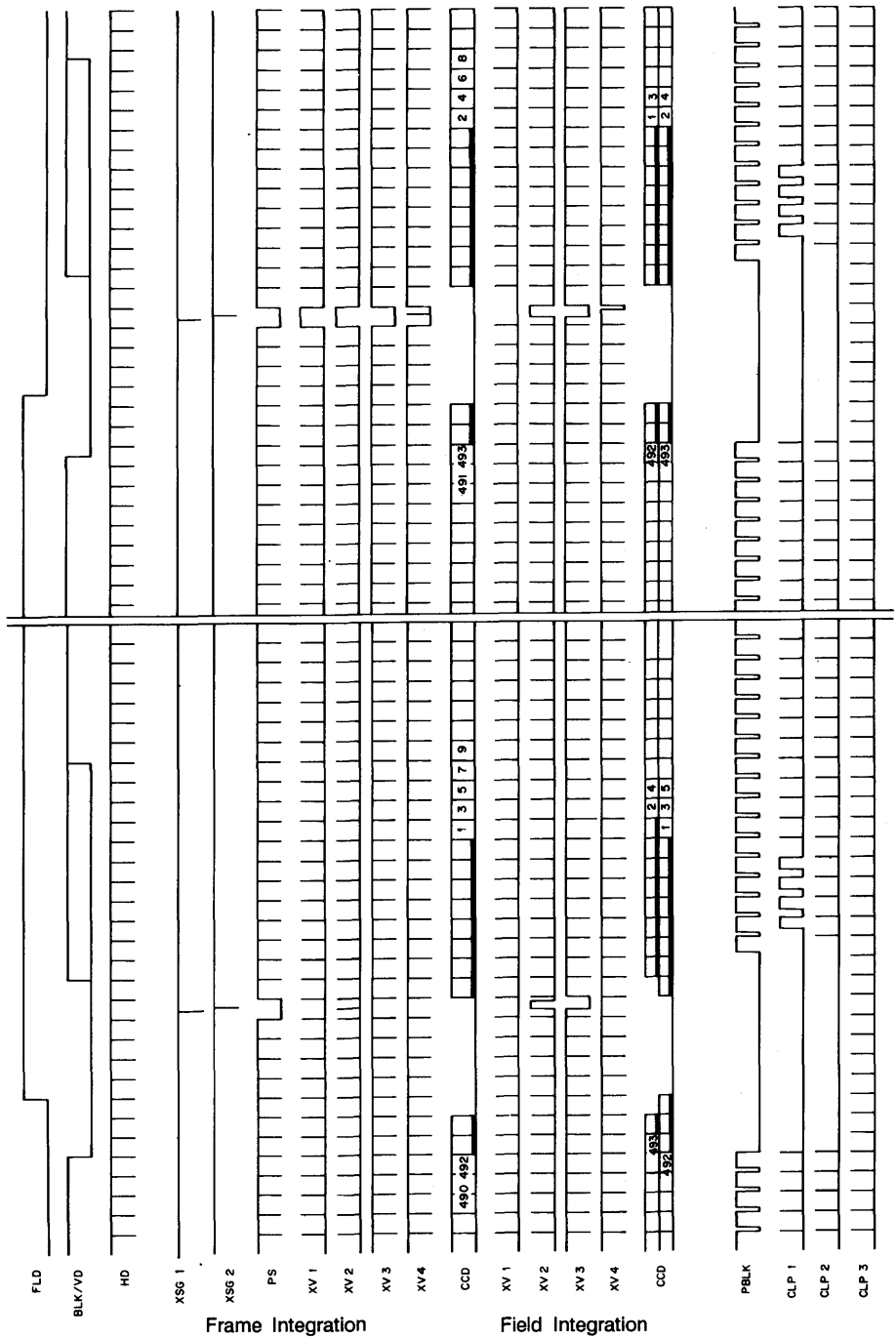
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			9	pF

Test condition: V_{DD}=V_I=0V, f_M=1MHz

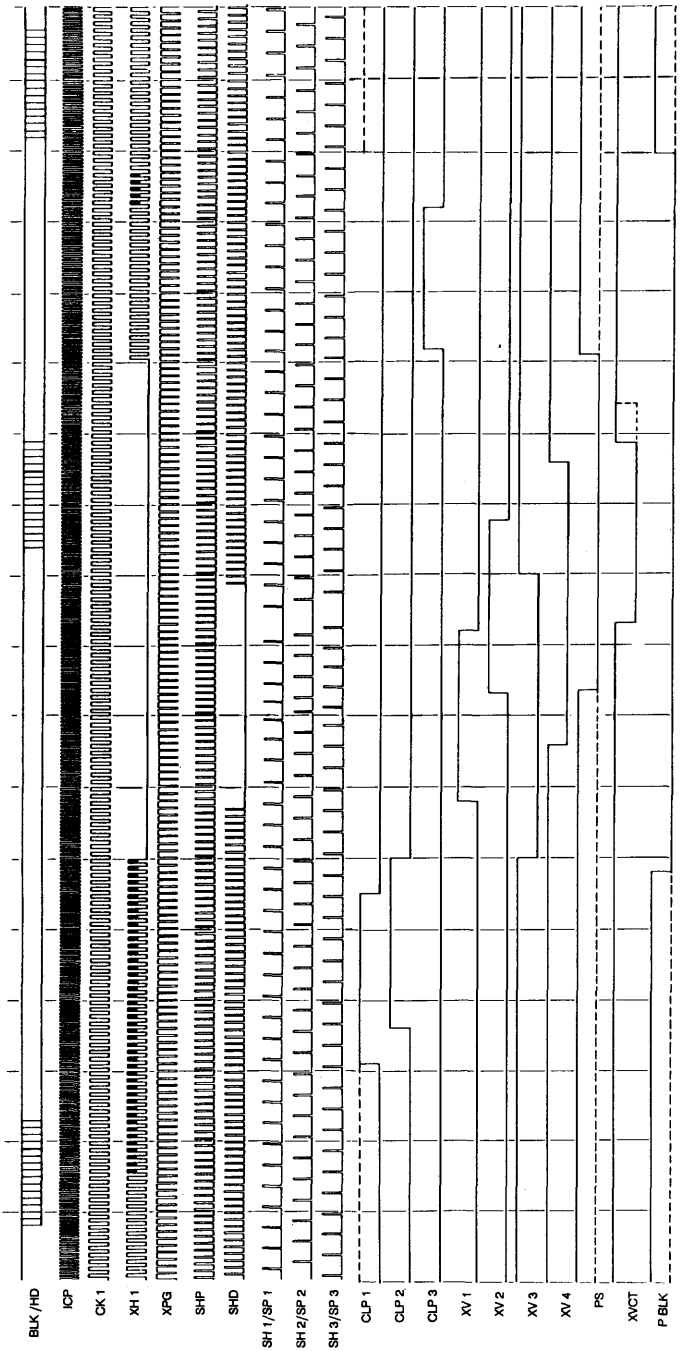
Application Circuit



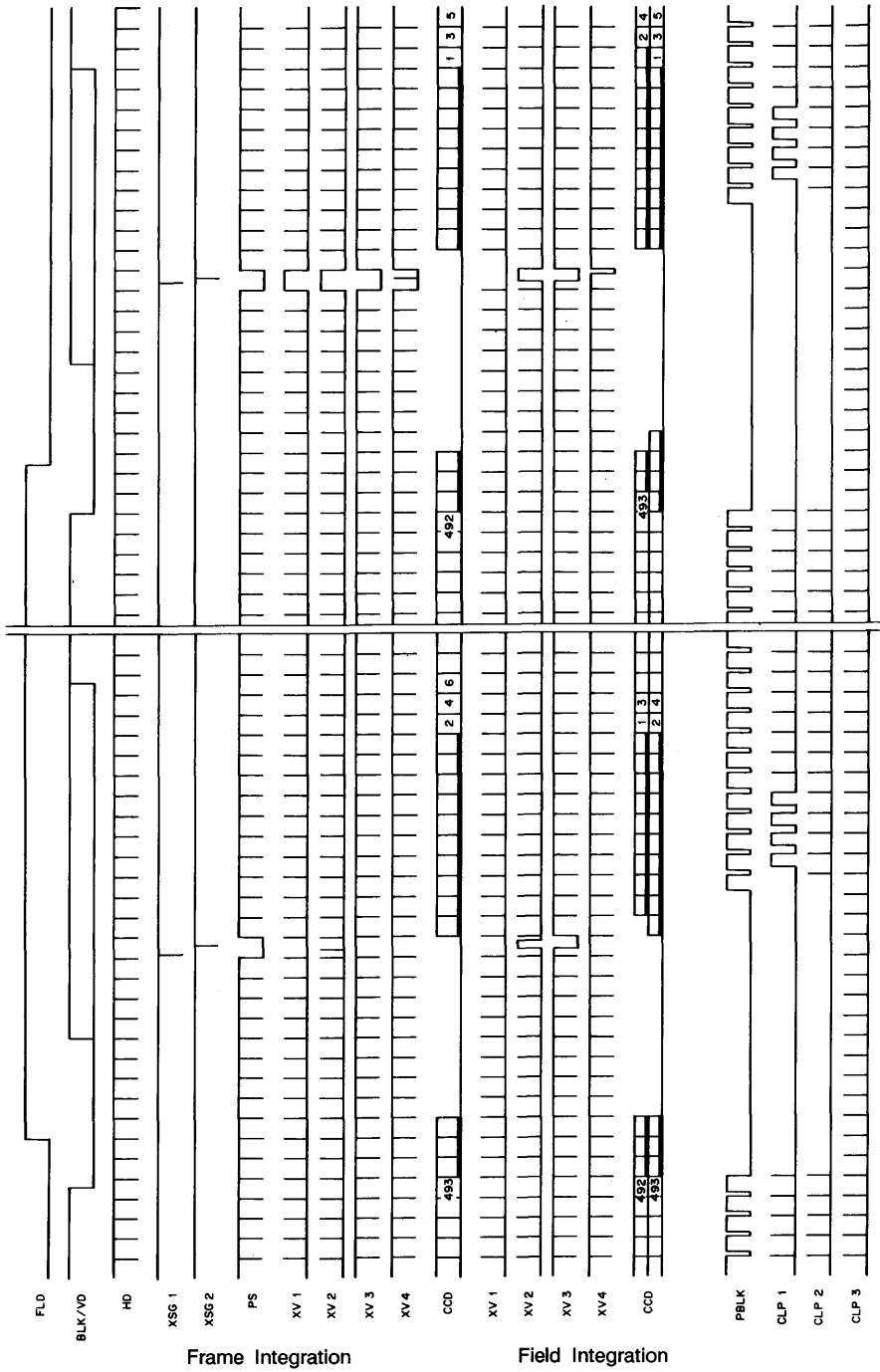
NTSC V Direction



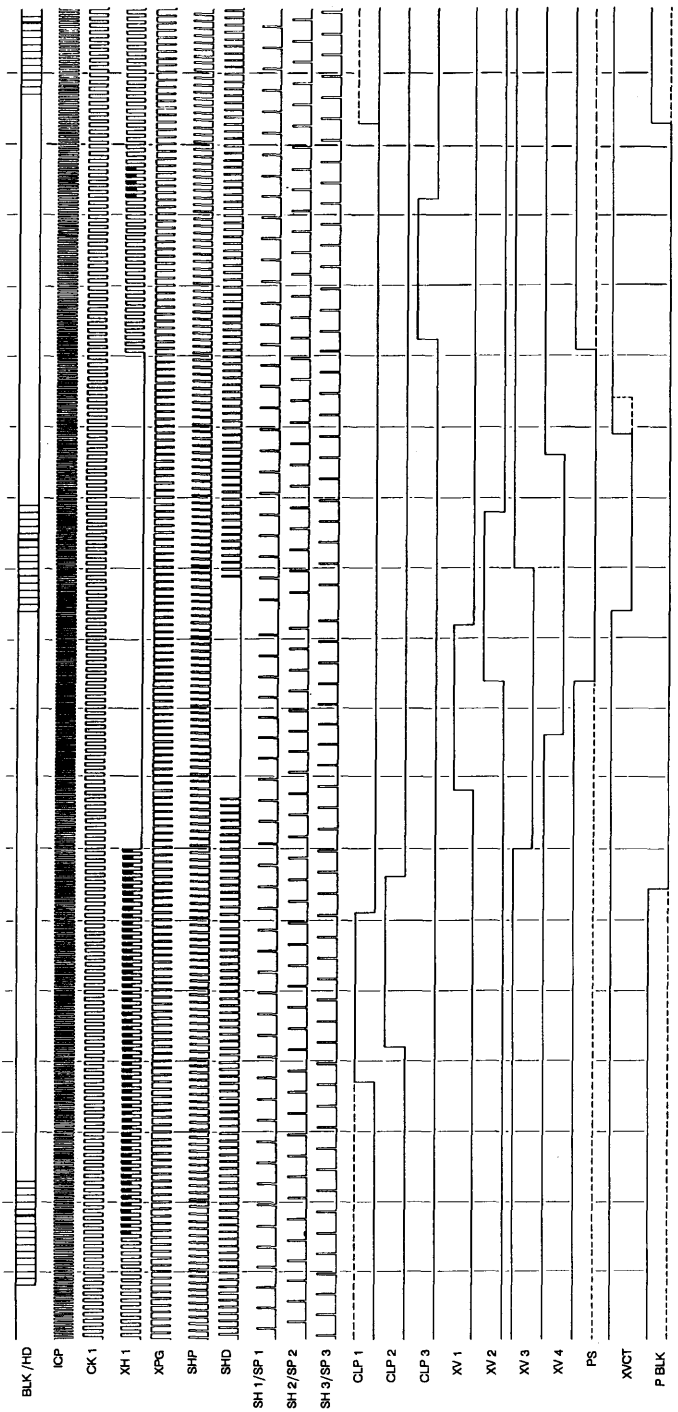
NTSC H Direction



PAL V Direction

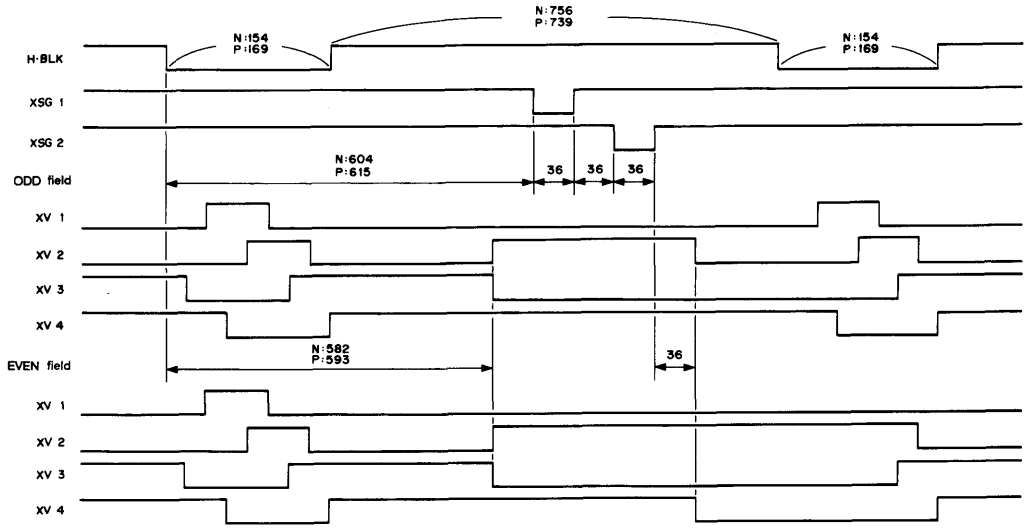


PAL H Direction

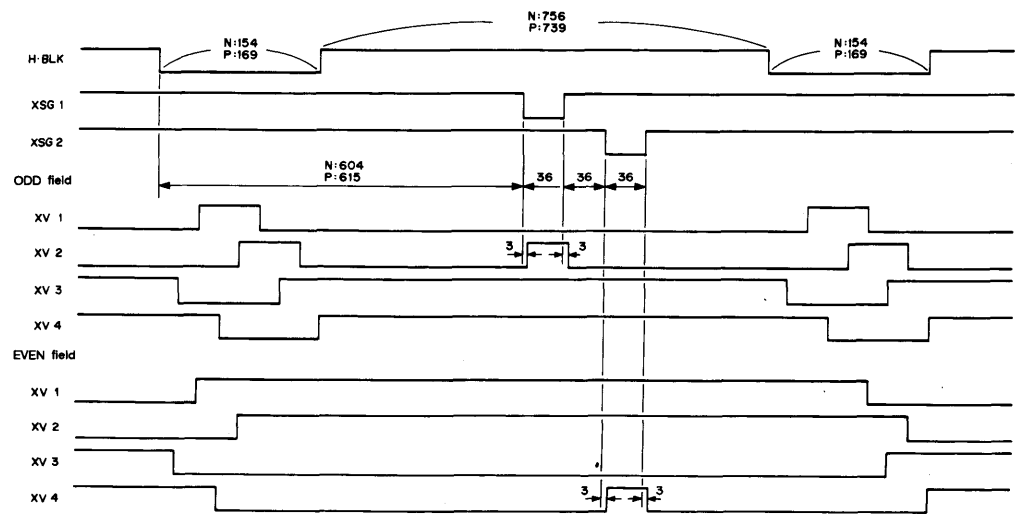


Readout Period

Field Integration mode



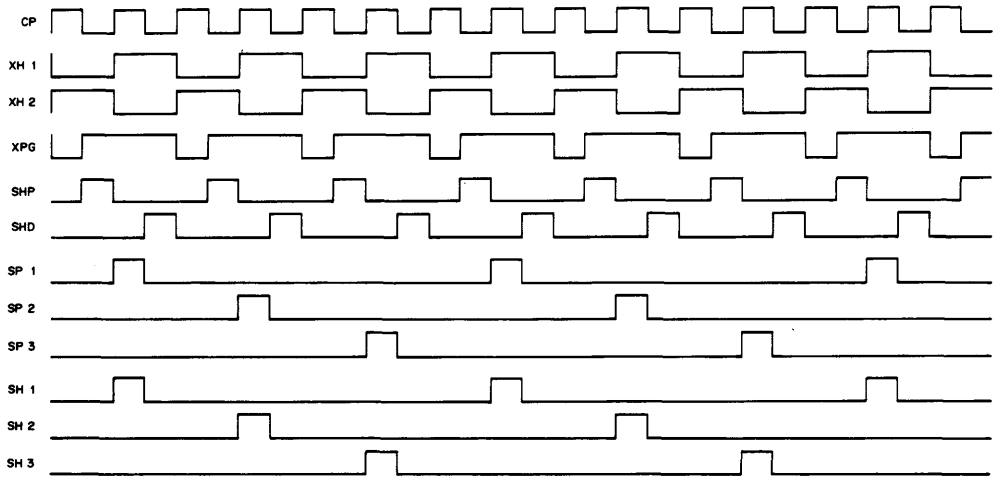
Frame Integration mode



N:NTSC
P:PAL

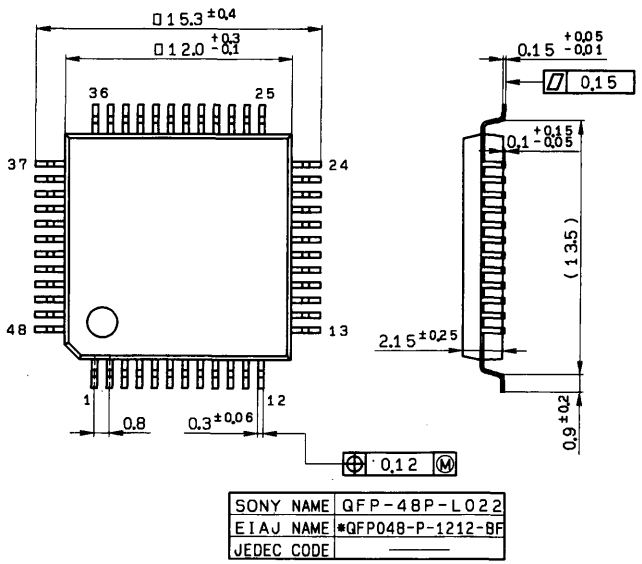
Note) Number: Clock (1 clock = 70ns)

H clock • Signal Processing Pulse Phase



Package Outline Unit: mm

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L022
EIAJ NAME	*QFP048-P-1212-BF
JEDEC CODE	———

CXD1141M

Timing setting for Electronic Shutter (CCD imager)

Description

The CXD1141M developed for CCD cameras is an LSI that sets the timing of electronic shutters.

Features

- Compatible with variable shutters (1/60 to 1/10000 sec)
- Compatible with flickerless
- Compatible with NSTC/PAL
- Mode setting compatible with serial/parallel

Function

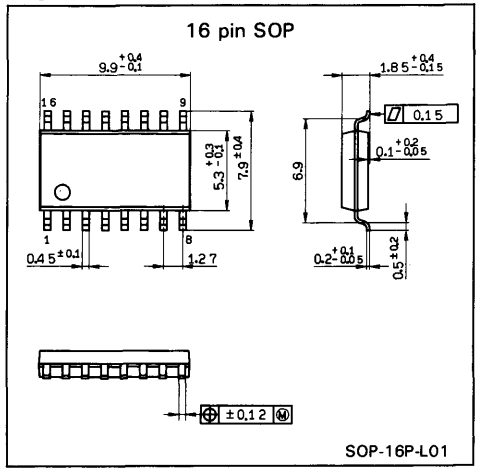
Sets the timing of electronic shutters.

Structure

Silicon gate CMOS

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

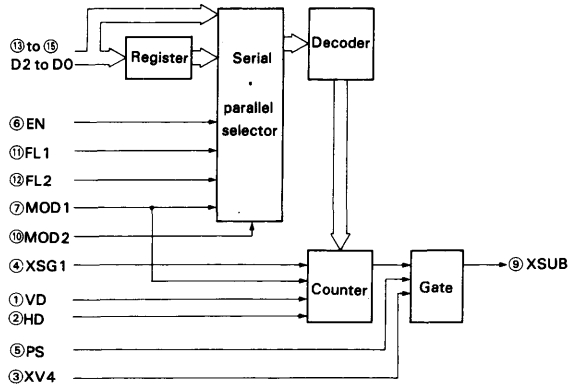
• Supply voltage	V_{DD}	Vss − 0.5* to + 7.0	V
• Input voltage	V_{IN}	Vss − 0.5* to V_{DD} + 0.5	V
• Output voltage	V_O	Vss − 0.5* to V_{DD} + 0.5	V
• Operating temperature	Topr	− 20 to + 75	°C
• Storage temperature	Tstg	− 55 to + 150	°C

* Vss = 0V

Recommended Operating Conditions

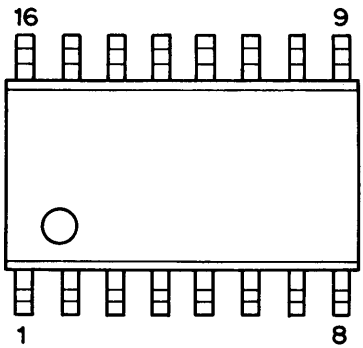
• Supply voltage	V_{DD}	4.5 to 5.5 (5.0V Typ.)	V
• Operating temperature	Topr	− 20 to + 75	°C

Block Diagram



70620-YA

Pin Configuration and Description (Top View)



No.	Symbol	I/O	Description
1	VD	I	Vertical drive pulse
2	HD	I	Horizontal drive pulse
3	XV4	I	Vertical scanning clock
4	XSG1	I	Sensor electric charge lead out pluse
5	PS	I	Power save pulse
6	EN	I	Enable signal L: Normal mode, H: Electronic shutter mode
7	MOD1	I	Mode switching L: PAL, H: NTSC
8	Vss	—	GND
9	XSUB	O	Electric charge sweep out pulse
10	MOD2	I	Mode switching L: serial input H: Parallel input
11	FL1	I	Mode switching L: flickerless H: Normal
12	FL2	I	Mode switching L: 60Hz H: 50Hz
13	D2	I	Shutter speed setting
14	D1	I	Shutter speed setting
15	D0	I	Shutter speed setting
16	V_{DD}	—	+5V

Electrical Characteristics

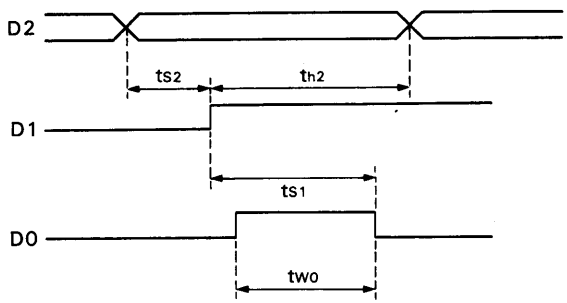
DC characteristics V_{DD} = 4.5 to 5.5V, Vss = 0V, Topr = −20 to +75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current		I_{DD}				2	mA
		I_{DDS}	Static state*1	0		0.1	mA
Output voltage	H level	V_{OH}	I_{OH} = −1.5mA	V_{DD} − 0.5		V_{DD}	V
	L level	V_{OL}	I_{OL} = 4.0mA	Vss		0.4	V
Input voltage	H level	V_{IH}		0.7V_{DD}			V
	L level	V_{IL}				0.3V_{DD}	V
Input threshold voltage	H level	V_{IH}		0.7V_{DD}	3.0		V
	L level	V_{IL}			2.0	0.3V_{DD}	V
	Hysteresis	Vh		0.5			V
Input leak current		I_{LI}	V_I = 0V *2	−20	−50	−120	μA

Note) *1 V_{DD} is applied to all input pins.
*2 Pull up resistance is provided to all input pins.

AC characteristics

For serial input mode



Item	Symbol	Min.	Typ.	Max.	Unit
D2 set up time with regards to D1 rising edge.	ts2	20			ns
D2 hold time with regards to D1 rising edge.	th2	20			ns
D1 rising edge set up time with regards to D0 Falling edge.	ts1	20			ns
D0 pulse width	two	20			ns

Input/Output Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

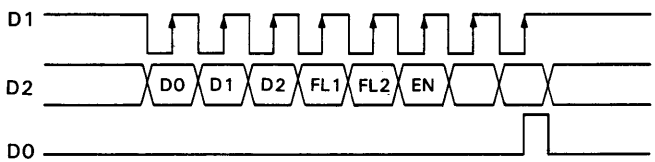
Testing conditions V_{DD} = V_I = 0V, fM = 1MHz

Mode setting

1) Parallel input mode (MOD2 = H)

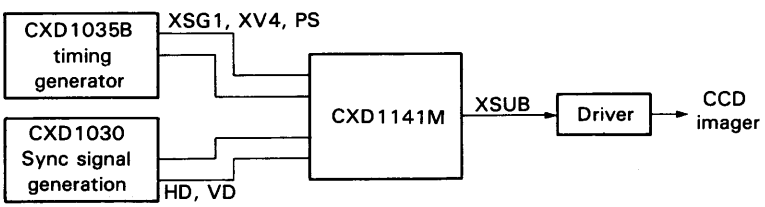
EN	MOD1	MOD2	FL1	FL2	D2	D1	D0	Shutter speed	Theoretical value
H	H	H	H		L	L	L	1/60	1/60
H	H	H	H		L	L	H	1/125	1/125
H	H	H	H		L	H	L	1/250	1/252
H	H	H	H		L	H	H	1/500	1/499
H	H	H	H		H	L	L	1/1000	1/1013
H	H	H	H		H	L	H	1/2000	1/2088
H	H	H	H		H	H	L	1/4000	1/4450
H	H	H	H		H	H	H	1/10000	1/10256
H	L	H	H		L	L	L	1/60	1/60
H	L	H	H		L	L	H	1/125	1/125
H	L	H	H		L	H	L	1/250	1/250
H	L	H	H		L	H	H	1/500	1/495
H	L	H	H		H	L	L	1/1000	1/1005
H	L	H	H		H	L	H	1/2000	1/2070
H	L	H	H		H	H	L	1/4000	1/4403
H	L	H	H		H	H	H	1/10000	1/10090
H	H		L	H				1/100	1/100
H	H		L	L				1/120	1/120
H	L		L	H				1/100	1/100
H	L		L	L				1/120	1/120
L								NORMAL	

2) Serial input mode (MOD2 = L)



D2 data is latched at register with the rising edge of D1 and shifted inside with the D0.

Application Circuit



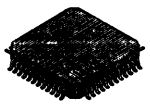
SONY® CXD1156Q/R

Timing Generator IC for ICX026/027

Description

CXD1156Q/R is a timing generator IC for CCD imagers ICX026AK/AL and ICX027AK/AL.

48pin QFP (Plastic)



48pin VQFP (Plastic)

Features

- NTSC/CCIR
- Field accumulation mode
- Color/Black and White mode
- 1/60 to 1/10,000 sec. variable speed, built-in electronic shutter.
- Built-in horizontal driver.
- Initialize operation at every field.

Functions

Timing generation for CCD imagers.

Structure

Silicon gate CMOS

Application

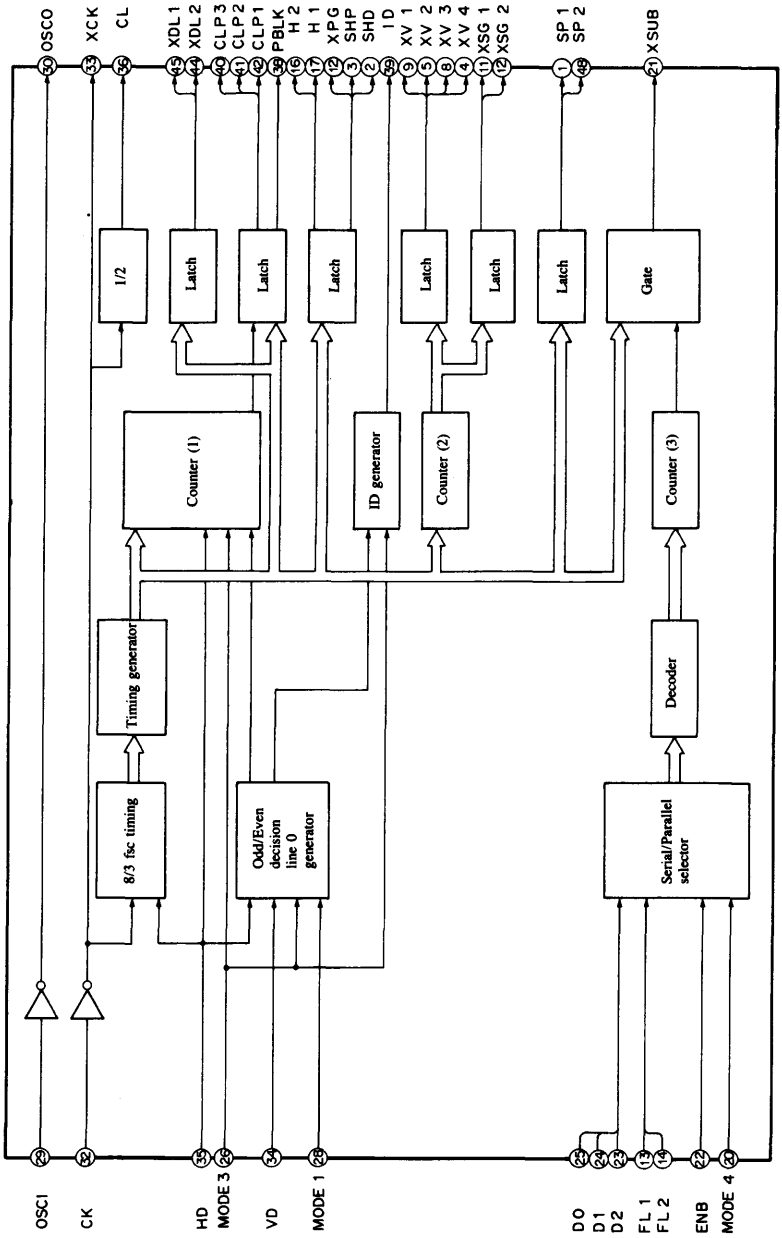
CCD camera system

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

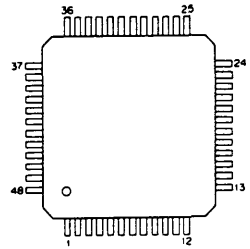
• Supply voltage	V_{DD}	$V_{SS}-0.5$ to $+7.0$	V
• Input voltage	V_I	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Output voltage	V_O	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Operating temperature	T_{opr}	-20 to $+75$	°C
• Storage temperature	T_{stg}	-55 to $+150$	°C

E89X12-YA

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	SP1	O	Color separation pulse ('L' in B/W mode)
2	SHD	O	Data sample hold pulse
3	SHP	O	Precharge level sample hold pulse
4	XV4	O	Vertical scanning clock
5	XV2	O	Vertical scanning clock
6	Vss	–	GND
7	TEST1	I	GND
8	XV3	O	Vertical scanning clock
9	XV1	O	Vertical scanning clock
10	XSG2	O	Sensor charge read out pulse
11	XSG1	O	Sensor charge read out pulse
12	XPG	O	Precharge gate pulse
13	FL1	I	Mode select L: Flicker less H: Normal, (pull up)
14	FL2	I	Mode select L: 60Hz H: 50Hz, (pull up)
15	Vss2	–	GND for driver
16	H2	O	Horizontal scanning clock
17	H1	O	Horizontal scanning clock
18	VDD2	–	+5V supply pin for driver
19	VDD	–	+5V
20	MODE4	I	Mode select L: Serial input H: Parallel input, (pull up)
21	XSUB	O	Discharge pulse
22	ENB	I	Enable signal L: Normal H: Electronic shutter (pull up)
23	D2	I	Shutter speed setting (schmitt input), (pull up)
24	D1	I	Shutter speed setting (schmitt input), (pull up)
25	D0	I	Shutter speed setting (schmitt input), (pull up)
26	MODE3	I	Mode select L: NTSC H: PAL., (pull down)
27	TEST2	I	GND
28	MODE1	I	Mode select L: Color H:B/W, (pull down)
29	OSCI	I	Ocsillation input oscillation frequency. NTSC: 28.6364 MHz CCIR: 28.3750 MHz
30	OSCO	O	Oscillation output
31	Vss	–	GND
32	CK	I	Duty control inverter input
33	XCK	O	Duty control inverter output

No.	Symbol	I/O	Description
34	VD	I	Vertical drive pulse
35	HD	I	Horizontal drive pulse
36	CL	O	4 fsc clock output (Sync generator clock input)
37	TEST0	I	GND
38	PBLK	O	Blanking cleaning pulse
39	ID	O	Line discrimination pulse
40	CLP3	O	Clamp pulse
41	CLP2	O	Clamp pulse
42	CLP1	O	Clamp pulse
43	V_{DD}	–	+5V
44	XDL2	O	Delay line pulse ('L' in B/W mode)
45	XDL1	O	Delay line pulse ('L' in B/W mode)
46	TEST3	I	GND
47	TEST4	I	GND
48	SP2	O	Color separation pulse ('L' in B/W mode)

Recommended Operating Conditions

Electrical characteristics (DC characteristics)

Item		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		V_{DD}	4.75	5.0	5.25	V
I/O voltage		V_I, V_O	V_{SS}		V_{DD}	V
Input voltage (Logical value) CMOS input cell		V_{IH}	0.7V_{DD}			V
		V_{IL}			0.3V_{DD}	
Schmitt trigger input voltage (D0, D1, D2)		V_{T+}	0.8V_{DD}			V
		V_{T-}			0.2V_{DD}	
		$V_{T+}-V_{T-}$	0.7	0.9		
Input rising, falling time		tr,tf	0		500	ns
Operating temperature		Ta	−20		+75	°C
Output voltage 1	I_{OH} = −2mA	V_{OH1}	*3			V
	I_{OL} = 4mA	V_{OL1}			0.4	V
*1 Output voltage 2	I_{OH} = −4mA	V_{OH2}	*3			V
	I_{OL} = 8mA	V_{OL2}			0.4	V
*2 Output voltage 3	I_{OH} = −8mA	V_{OH3}	*3			V
	I_{OL} = 8mA	V_{OL3}			0.4	V

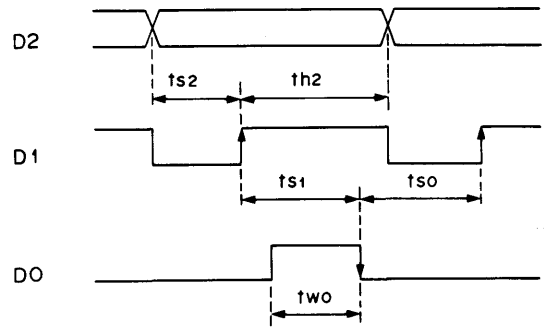
*1. Pin 12 (XPG).
*2. Pins 16 and 17 (H1,H2)
*3. V_{DD}−0.5

Oscillation I/O Electrical Characteristics (OSCI, OSCO, CK, XCK)

Item		Symbol	Min.	Typ.	Max.	Unit
Logical threshold value		V_{th}		$V_{DD}/2$		V
Input voltage		V_{IH}	0.7V_{DD}			V
		V_{IL}			0.3V_{DD}	V
Feedback resistor	$V_{IN} = V_{SS}$ or V_{DD}	R_{FB}	500k	2M	5M	Ω
Output voltage	$I_{OH} = -1mA$	V_{OH}	$V_{DD}/2$			V
	$I_{OL} = 1mA$	V_{OL}			$V_{DD}/2$	V

AC Characteristics

Serial input mode



Symbol	Item	MIN.	MAX.
ts2	D2 set up time vs. D1 rising edge	20nS	—
th2	D2 hold time vs. D1 rising edge	20nS	—
ts1	D1 rising edge set up time vs. D0 falling edge	20nS	—
tw0	D0 pulse width	20nS	50μS
ts0	D0 falling edge set up time vs. D1 rising edge	20nS	—

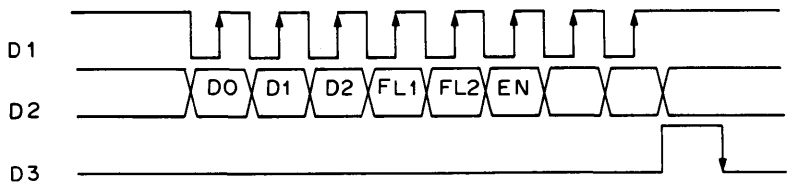
Mode Setting

1. Parallel input (mode 4 = 'H')

Table-1

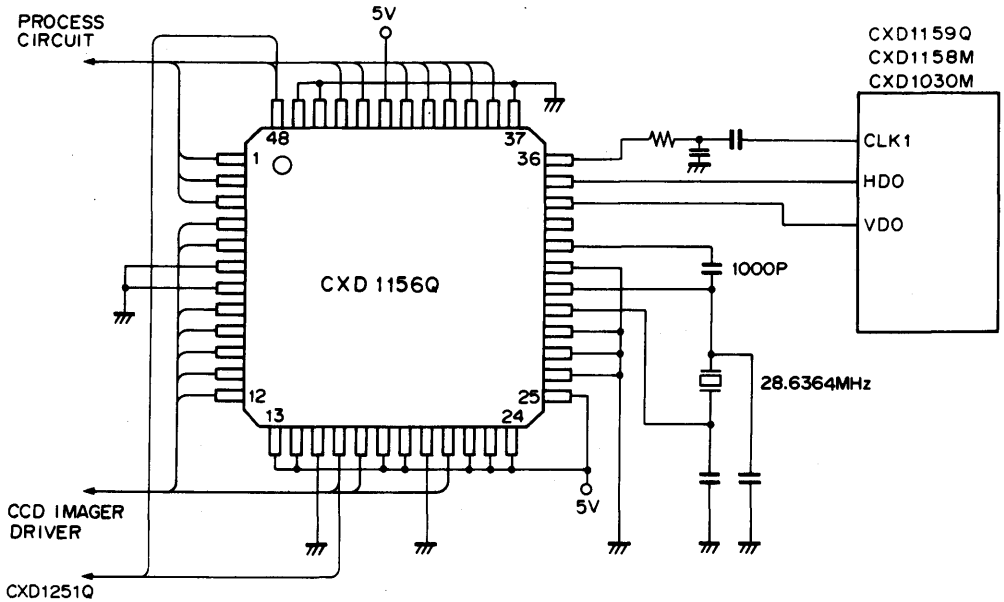
ENB	MODE 3	MODE 4	FL1	FL2	D2	D1	D0	Shutter speed
H	L	H	H		L	L	L	1/60
H	L	H	H		L	L	H	1/125
H	L	H	H		L	H	L	1/250
H	L	H	H		L	H	H	1/500
H	L	H	H		H	L	L	1/1000
H	L	H	H		H	L	H	1/2000
H	L	H	H		H	H	L	1/4000
H	L	H	H		H	H	H	1/10000
H	H	H	H		L	L	L	1/60
H	H	H	H		L	L	H	1/125
H	H	H	H		L	H	L	1/250
H	H	H	H		L	H	H	1/500
H	H	H	H		H	L	L	1/1000
H	H	H	H		H	L	H	1/2000
H	H	H	H		H	H	L	1/4000
H	H	H	H		H	H	H	1/10000
H	L		L	H				1/100
H	L		L	L				1/120
H	H		L	H				1/100
H	H		L	L				1/120
L								NORMAL

2. Serial input mode (mode 4 = 'L')



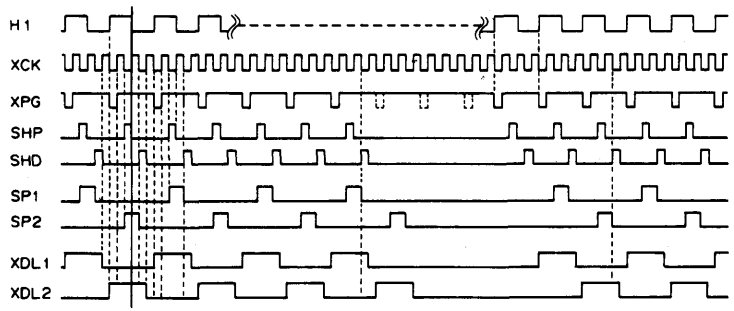
D2 data is latched by the register with the rising edge of D1, and taken inside with the falling edge of D0.

Application Circuit (NTSC mode, color mode)

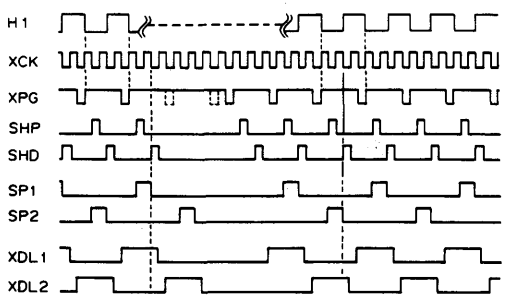


Timing Chart 1. [High speed timing]

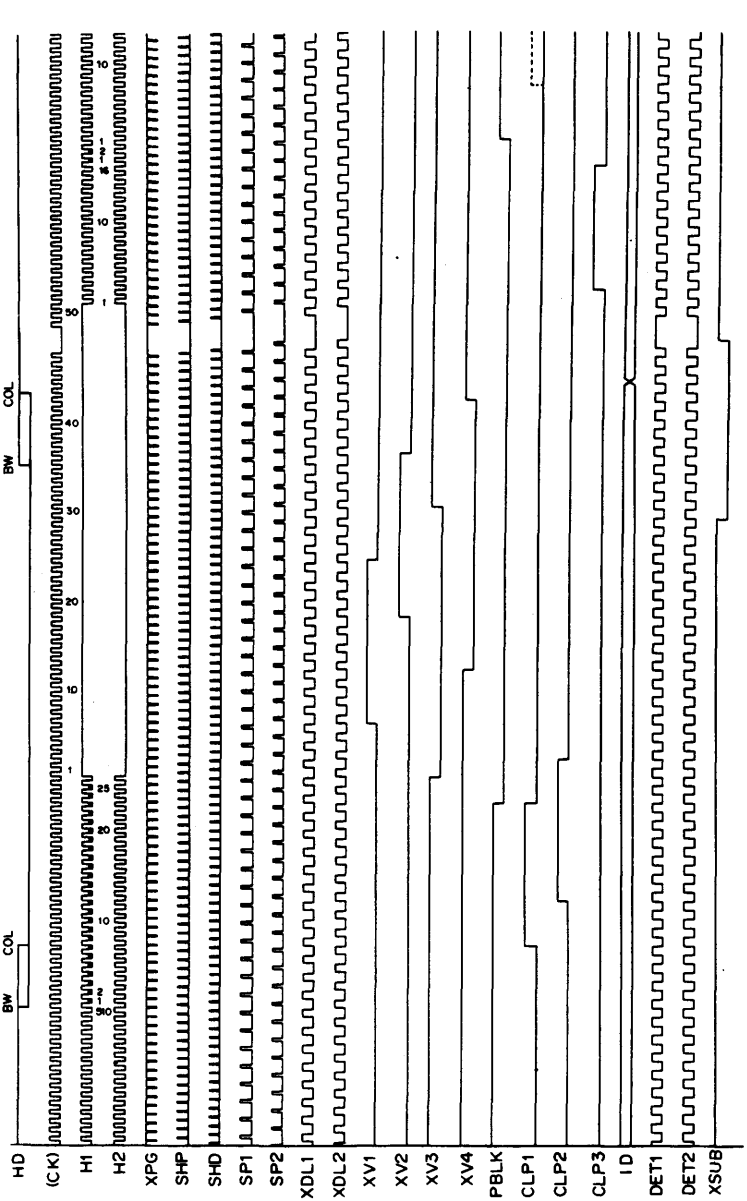
NTSC



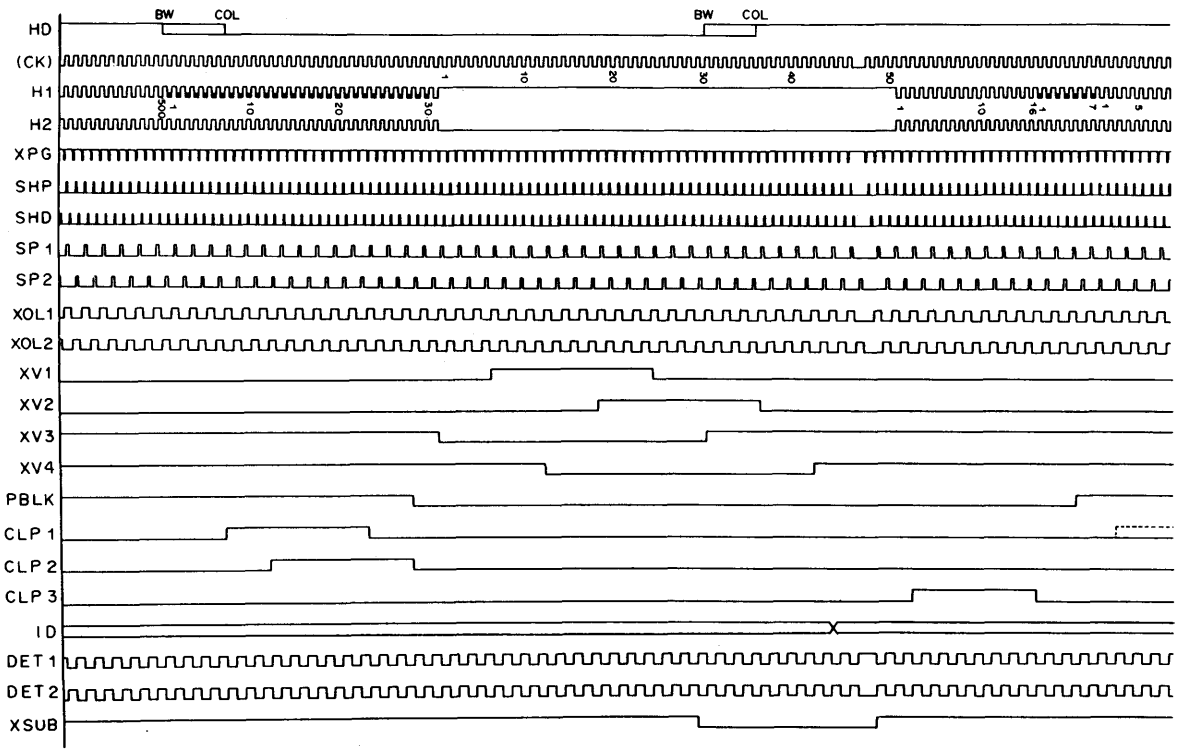
CCIR



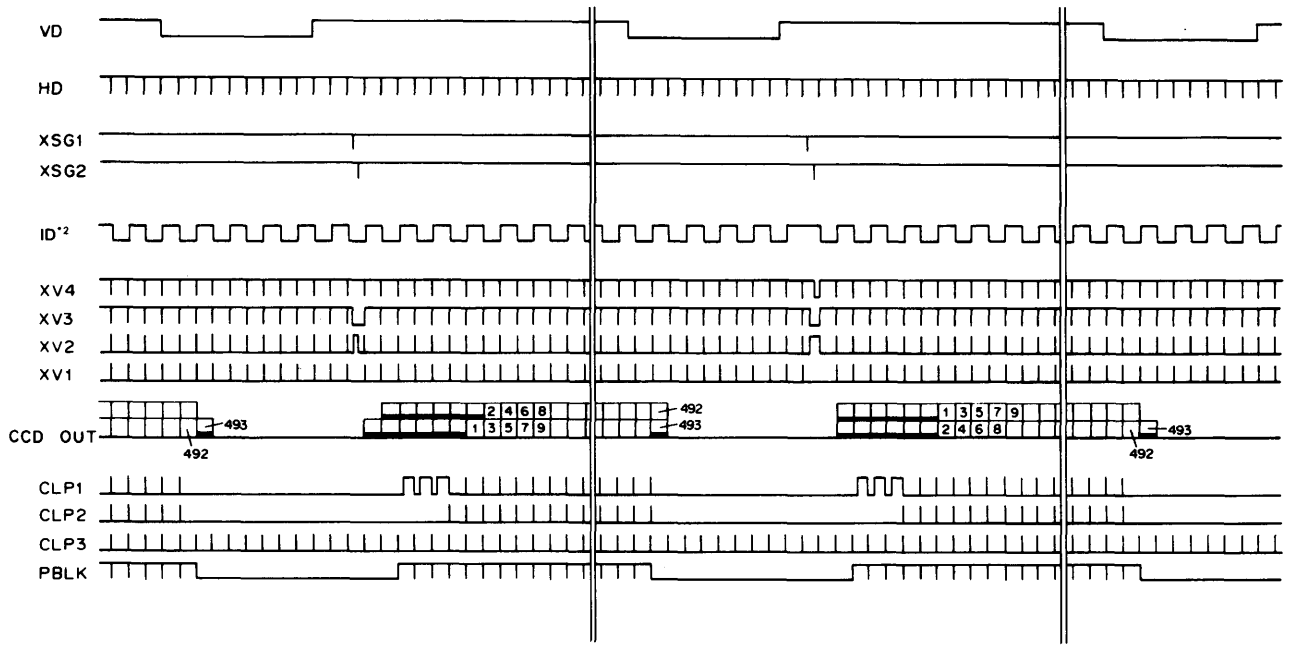
Timing Chart 2. [NTSC mode]



Timing Chart 3. [CCIR mode]

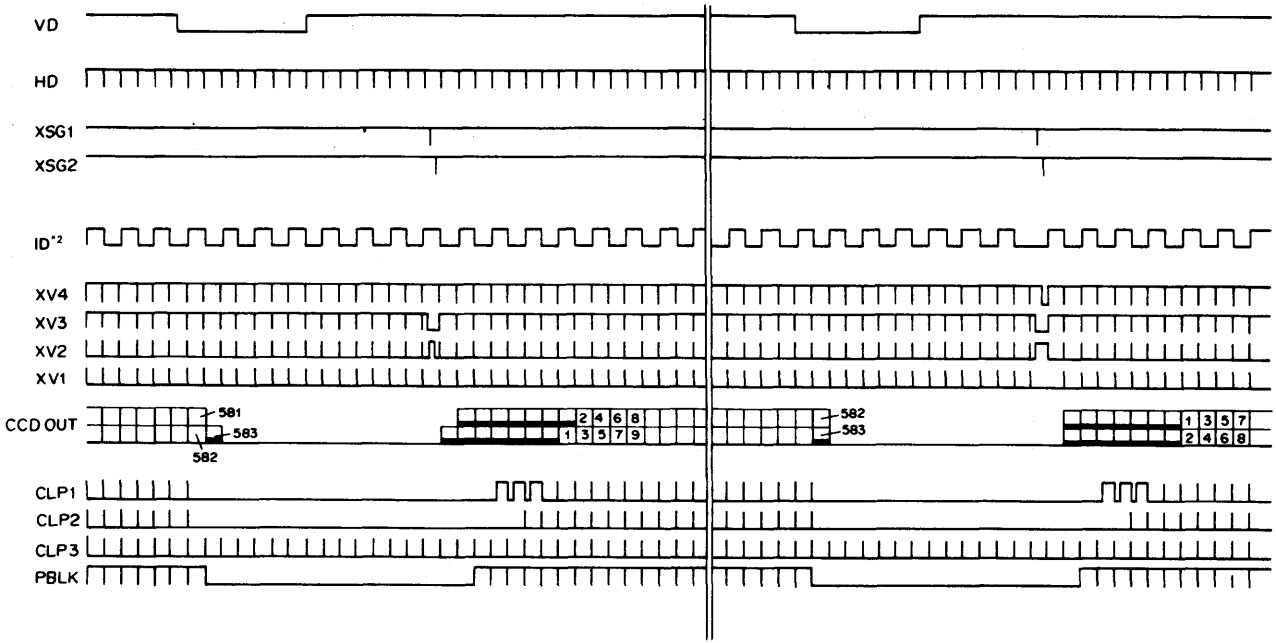


Timing Chart 4. [NTSC (Low speed timing) B/W mode][*1]



Note) ***1.** 1 H advance of the output signal to VD/HD in color mode.
***2.** 0 level in monochrome mode.

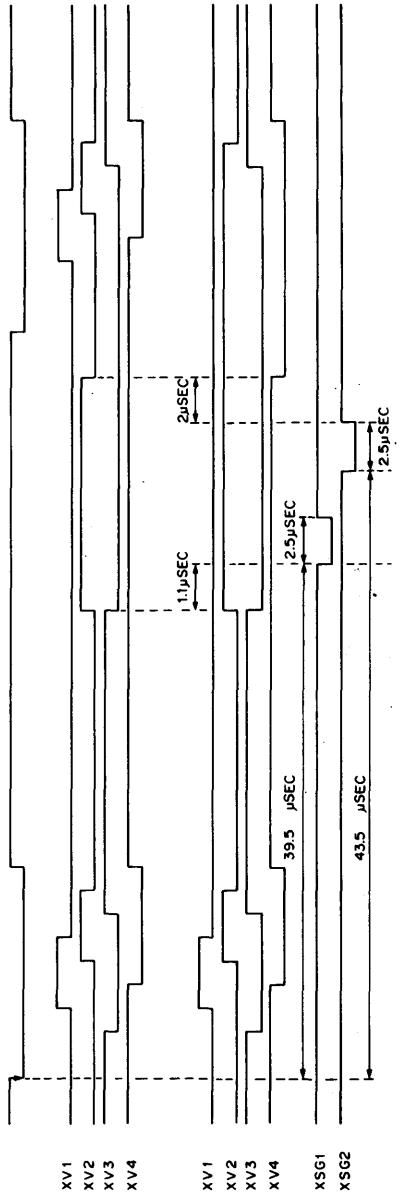
Timing Chart 5. [CCIR (Low speed timing)]*1



Note) ***1.** 1 H advance of the output signal to VD/HD in color mode.

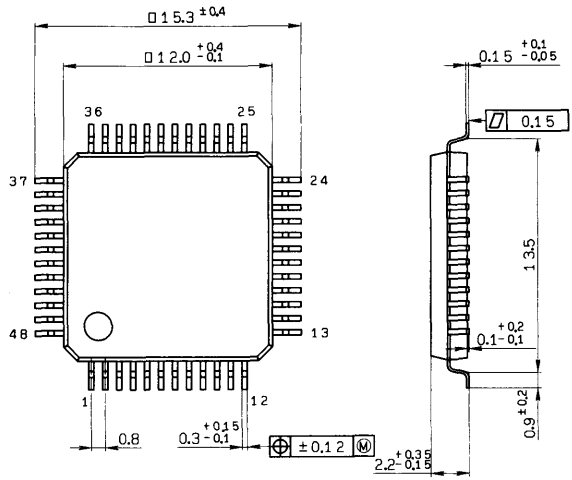
***2.** 0 level in monochrome mode.

Timing Chart 6. [XV1 to XV4 modulation]



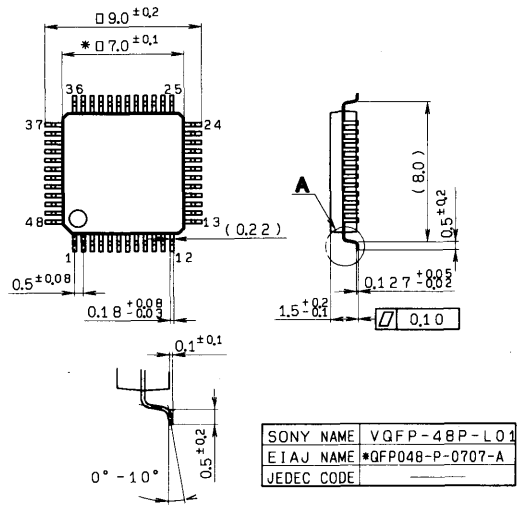
Package Outline Unit: mm

48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	

48pin VQFP (Plastic) 0.2g



SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	

Detaild diagram of **A**

Note) Dimensions marked with * do not include residual resin.

Timing Generator for Blemish Compensation

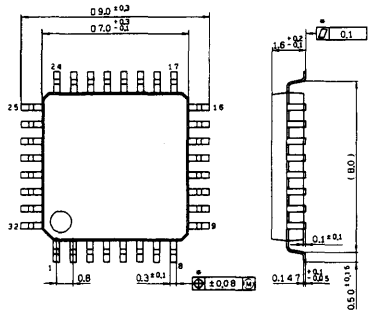
Description

CXD1251Q is a CMOS LSI IC used for blemish compensation in CCD imagers such as ICX026AK/AL, ICX022AK (NTSC), ICX027AK/AL, ICX024AK (PAL), CCD blemishes can be compensated at a rate of up to 10 per field.

Package Outline

Unit : mm

32 pin QFP (Plastic)



QFP-32P-L01

Features

- Generation of blemish compensation pulses.
- When used for blemish compensation in ICX 026AK/AL and ICX027AK/AL it is combined with scanning IC's CXD1156R (Q).
- For the blemish compensation in ICX022AK or 024AK it is combined with scanning IC CXD1149R.

Structure

CMOS LSI

Application

- Blemish compensation in CCD imagers

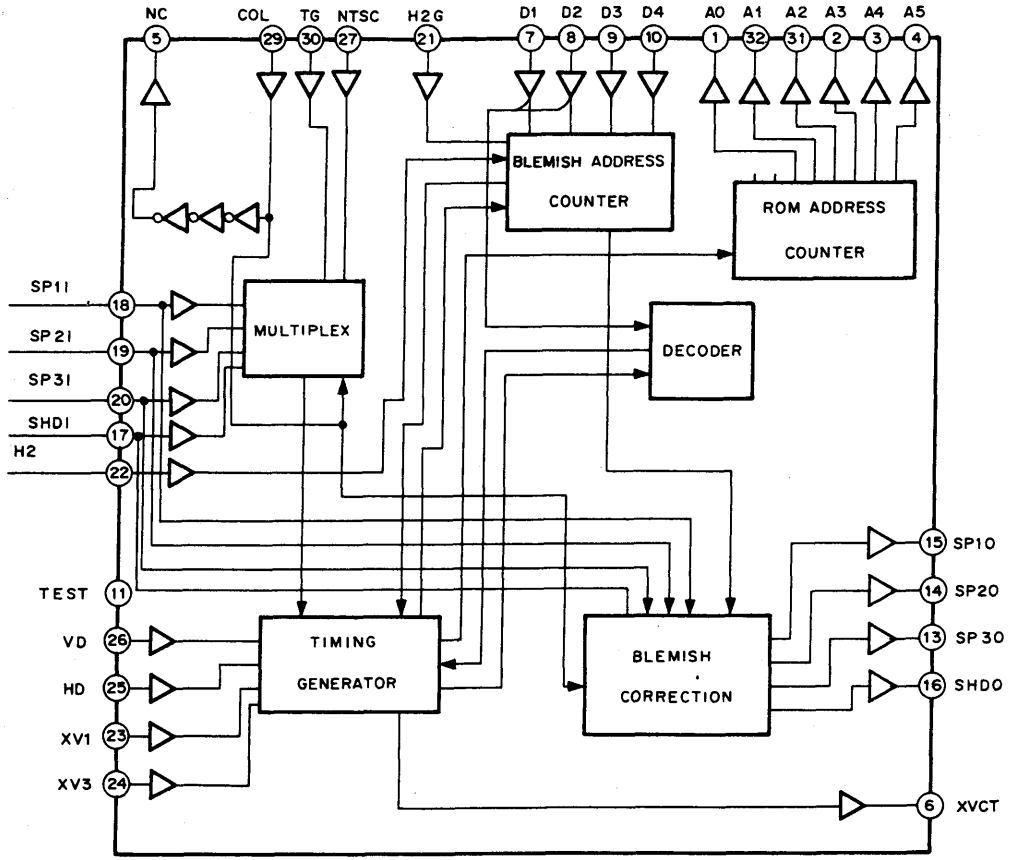
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	V_{SS} − 0.5 to + 7.0	V
• Input voltage	V_I	V_{SS} − 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} − 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	− 20 to + 75	°C
• Storage temperature	Tstg	− 55 to + 150	°C

Recommended Operating Conditions

• Supply voltage	V_{CC}	4.75 to 5.25	V
• Operating temperature	Topr	− 20 to + 75	°C

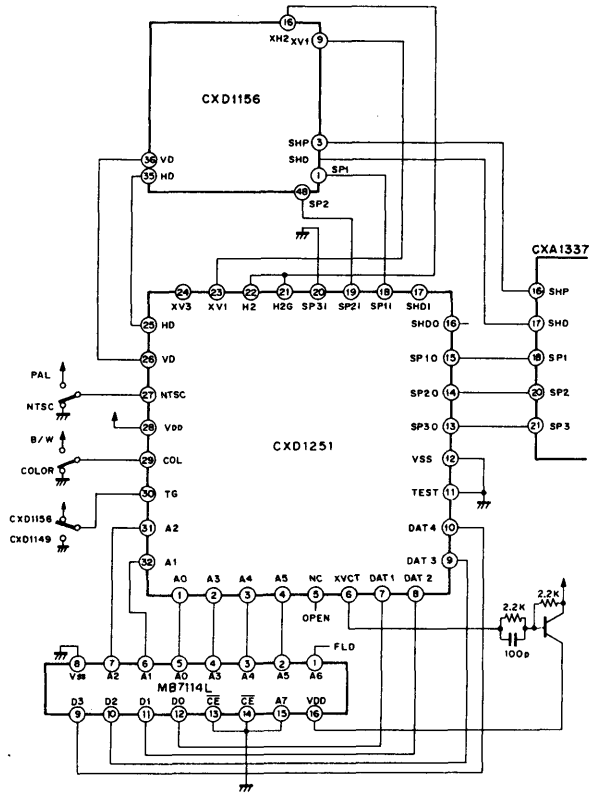
Block Diagram



Pin Description

No.	Symbol	I/O	Description
1	A0	O	Address output pin for external ROM
2	A3	O	Address output pin for external ROM
3	A4	O	Address output pin for external ROM
4	A5	O	Address output pin for external ROM
5	NC	—	
6	XVCT	O	Control output pin for external ROM supply
7	DAT1	I	Data input pin from external ROM
8	DAT2	I	Data input pin from external ROM
9	DAT3	I	Data input pin from external ROM
10	DAT4	I	Data input pin from external ROM
11	TEST	I	Test pin. Normally GND
12	V_{SS}	—	
13	SP3O	O	S/H pulse output pin for blemish compensation
14	SP2O	O	S/H pulse output pin for blemish compensation
15	SP1O	O	S/H pulse output pin for blemish compensation
16	SHDO	O	S/H pulse output pin for blemish compensation
17	SHDI	I	S/H pulse input pin for blemish compensation
18	SP1I	I	S/H pulse input pin for blemish compensation
19	SP2I	I	S/H pulse input pin for blemish compensation
20	SP3I	I	S/H pulse input pin for blemish compensation
21	H2G	I	CCD horizontal scanning clock input pin
22	H2	I	CCD horizontal scanning clock input pin
23	XV1	I	CCD vertical scanning clock input pin
24	XV3	I	CCD vertical scanning clock input pin
25	HD	I	Horizontal drive pulse input pin from sync generator IC
26	VD	I	Vertical drive pulse input pin from sync generator IC
27	NTSC	I	NTSC/PAL Mode select pin H : PAL L : NTSC
28	V_{DD}	I	Supply
29	COL	I	Color/B/W mode select pin H : B/W L : Color
30	TG	I	TG mode select pin H : 1149R L : 1156R
31	A2	O	Address output pin for external ROM
32	A1	O	Address output pin for external ROM

Peripheral Circuit (CXD1156 checkers in use)



Electrical Characteristics

DC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IHC}		0.7V_{DD}			V
	V_{ILC}				0.3V_{DD}	V
Input voltage	V_{IH}	SP1I, SP2I, SP3I, SHDI	2.8			V
	V_{IL}				0.6	V
Output voltage	V_{OH}	$I_{OH} = -2mA$	$V_{DD} - 0.5$			V
	V_{OL}	$I_{OL} = 4mA$			0.4	V

I/O capacity

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input pin	C_{IN}				9	pF
Output pin	C_{OUT}				11	pF

Connection Diagram for Respective Modes

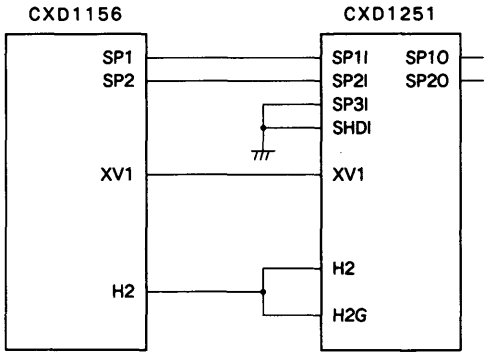


Fig. 1. With CXD1156 checkers in use

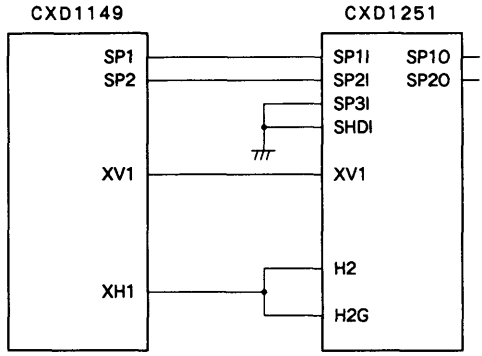


Fig. 2. With CXD1149 checkers in use

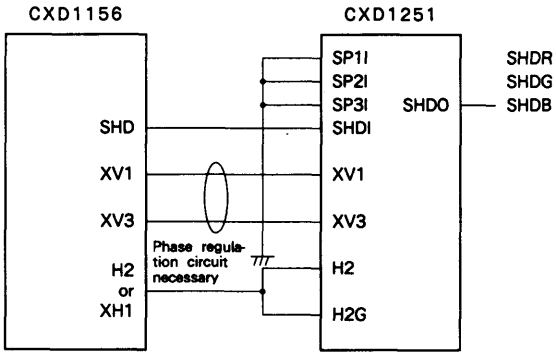


Fig. 3. CXD1156 : BW in use

SONY

CXD1255Q

Timing Signal Generator of CCD Camera Scanner (for ICX038AK/039AK)

Description

CXD1255Q is a CMOS-type LSI developed for use in the imager scanner for both ICX038AK/AL(NTSC) and ICX039AK/AL (PAL). This IC is used in conjunction with signal generators CXD1030M or CXD1158M.

48pin QFP (Plastic)

Features

- Generates pulses for driving imagers ICX038AK/AL and ICX039AK/AL
- Generates signal processing pulses for chequered coding
- NTSC (EIA)/PAL (CCIR) mode switchover.
- Field/frame accumulation
- Color and B/W mode
- Electronic shutter operation
- Built-in clock oscillation inverter

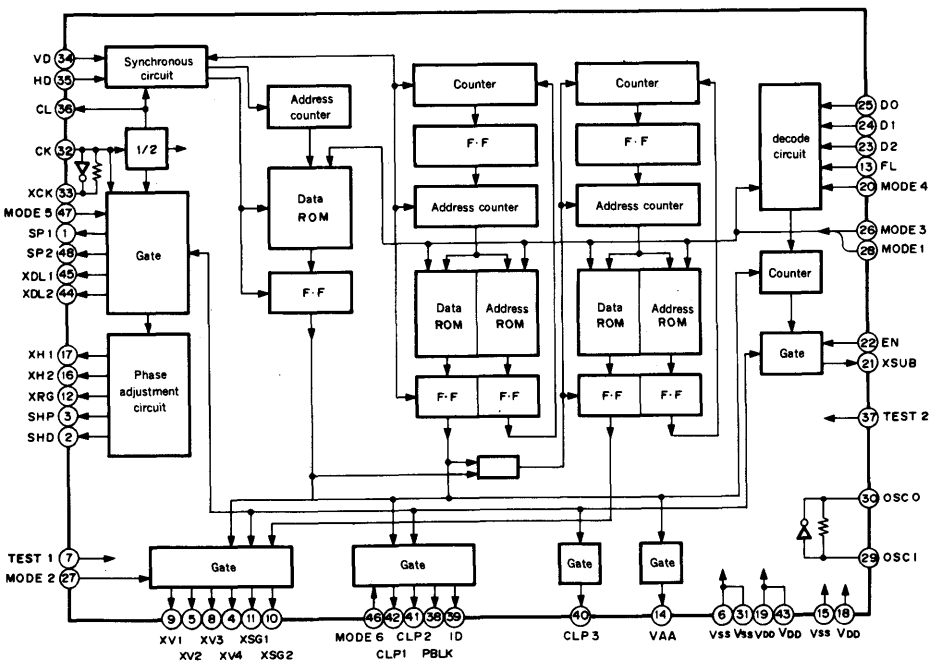
Applications

- CCD camera (NTSC/PAL)

Structure

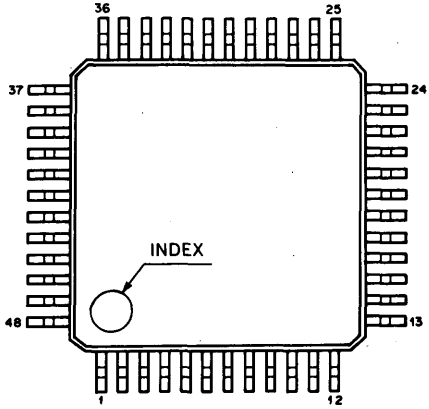
- Silicon gate CMOS

Block Diagram and Pin Configuration



E89219-HP

Pin Configuration (Top View)



Absolute Maximum Ratings (Ta=25°C)V_{SS}=0V

• Storage temperature	T_{stg}	−55 to +150	°C
• Operating temperature	T_{opr}	−20 to +75	°C
• Supply voltage	V_{DD}	V_{SS}−0.5 to +7.0	V
• Input voltage	V_I	V_{SS}−0.5 to V_{DD}+0.5	V
• Output voltage	V_O	V_{SS}−0.5 to V_{DD}+0.5	V

Recommended Operating Conditions

• Supply voltage	V_{DD}	+4.75 to +5.25	V

Pin Description

No.	Symbol	I/O	Description
1	SP1	O	Color separation S/H pulse (Note 1) L
2	SHD	O	CCD data output S/H pulse
3	SHP	O	CCD precharge level S/H pulse
4	XV4	O	Clock pulse for V register
5	XV2	O	Clock pulse for V register
6	V_{SS}	—	GND
7	TEST1	I	OPEN Pull-Up resistance
8	XV3	O	Clock pulse for V register
9	XV1	O	Clock pulse for V register
10	XSG2	O	Sensor charge Read out pulse
11	XSG1	O	Sensor charge Read out pulse
12	XRG	O	CCD output reset pulse
13	FL	I	Electronic shutter flickerless, L: Flickerless, H: Normal
14	VAA	O	Vertical blanking cleaning pulse

No.	Symbol	I/O	Description
15	V_{SS}	—	GND
16	XH2	O	Clock pulse for H register
17	XH1	O	Clock pulse for H register
18, 19	V_{DD}	—	Power supply
20	MODE4	I	Input switchover of electronic shutter speed,L: Serial input, H: parallel input
21	XSUB	O	Sensor discharge pulse
22	EN	I	Electronic shutter ON/OFF, L: Shutter OFF, H: Shutter ON
23	D2	I	Electronic shutter speed switchover input
24	D1	I	Electronic shutter speed switchover input
25	D0	I	Electronic shutter speed switchover input
26	MODE3	I	NTSC/PAL switchover, L: NTSC, H: PAL
27	MODE2	I	Field/frame accumulation switchover, L: Field H: Frame
28	MODE1	I	(Note 2)
29	OSCI	I	Oscillation inverter input
30	OSCO	O	Oscillation inverter output
31	V_{SS}	—	GND
32	CK	I	Duty controlling inverter input
33	XCK	O	Duty controlling inverter output
34	VD	I	Vertical sync signal input
35	HD	I	Horizontal sync signal input
36	CL	O	Sync Generator clock output
37	TEST2	I	GND Pull-Down resistance
38	PBLK	O	Pre-blanking pulse
39	ID	O	Line identification pulse (Note 1) L
40	CLP3	O	Clamp pulse
41	CLP2	O	Clamp pulse
42	CLP1	O	Clamp pulse
43	V_{DD}	—	Power Supply
44	XDL2	O	Clock pulse for delay line (Note 1) SHDP
45	XDL1	O	Clock pulse for delay line (Note 1) L
46	MODE6	I	PBLK control pulse, L: Narrow H: Wide (Note 2)
47	MODE5	I	(Note 2)
48	SP2	O	Color separation S/H pulse (Note 1) L

Note 1) B/W mode output
Note 2) See Operation (p.5) for MODE1, 5, and 6 switchover.

Electrical Characteristics

DC characteristics

V_{DD}=5V±5%, V_{SS}=0V, T_{opr}=−20to+75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH}		0.7V_{DD}			V
	L level	V_{IL}				0.3V_{DD}	V
Input voltage (FL,EN,D0 to 2) * Schmitt trigger	H level	V_{T+}		0.8V_{DD}			V
	L level	V_{T-}				0.2V_{DD}	V
	Hysteresis	$V_{T+}-V_{T-}$		0.7	0.9		V
Output voltage	H level	V_{OH}	I_{OH}=−2mA	V_{DD}−0.5			V
	L level	V_{OL}	I_{OL}=4mA			0.4	V
Output voltage (Oscillation cell) (OSCO, XCK)	H level	V_{OH}	I_{OH}=−1mA	V_{DD}/2			V
	L level	V_{OL}	I_{QL}=1mA			V_{DD}/2	V
Input leak current			V_I=0V to V_{DD}	−10		10	μA
Oscillation cell feedback resistance		R_{FB}		500K	2M	5M	Ω

I/O capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
output pin	C_{OUT}			11	pF

Test condition: V_{DD}=V_I=0V, f=1MHz

Operation

CXD1255Q is provided with input pins for the setting of various modes. Related input pins are pulled up or pulled down beforehand inside the IC. Should an input pin be left open a certain mode is selected. (The pull up/down resistance value is approx. 100kΩ.)

<For color usage>

Pin	No.	Preset	Description	
			Input: "H"	Input: "L"
MODE1	28	L	Normal: "L"	
MODE2	27	L	Normal: "L"	
MODE3	26	L	PAL	NTSC
MODE4	20	H	(Electronic shutter speed setting)	
			Parallel input	Serial input
MODE5	47	L	Normal: "L"	
MODE6	46	L	(PBLK control pulse width switchover)	
			Wide	Narrow
EN	22	H	Electronic shutter ON	OFF
FL	13	H	Electronic shutter Normal	Flickerless
D2	23	H	Electronic shutter speed control (described later in detail)	
D1	24	H		
D0	25	H		

〈For black-and-white usage〉

Pin	No.	Preset	Description	
			Input: "H"	Input: "L"
MODE1	28	L	Normal: "H"	
MODE2	27	L	Frame accumulation	Field accumulation
MODE3	26	L	PAL	NTSC
MODE4	20	H	(Electronic shutter speed setting) Parallel input	Serial input
MODE5	47	L	Normal "H"	
MODE6	46	L	Normal "H"	
EN	22	H	Electronic shutter ON	OFF
FL	13	H	Electronic shutter Normal	Flickerless
D2	23	H	Electronic shutter speed control (described later in detail)	
D1	24	H		
D0	25	H		

Operating conditions are shown in timing charts:

- NTSC vertical timing chart
- NTSC horizontal timing chart
- PAL vertical timing chart
- PAL horizontal timing chart

Electronic shutter speed control

	External pin							Internal register								Shutter speed XSUB ㉑
	P/S	EN	CRNT	FL	D2	D1	D0			EN	FL2	FL1	D2	D1	D0	
	↑ ⑳	↑ ㉒	↓ ㉖	↑ ⑬	↑ ㉓	↑ ㉔	↑ ㉕	D7	D6	D5	D4	D3	D2	D1	D0	
Parallel mode P/S=H	H	H		H	L	L	L									1/60 Note)
	H	H		H	L	L	H									1/125
	H	H		H	L	H	L									1/250
	H	H		H	L	H	H									1/500
	H	H		H	H	L	L									1/1000
	H	H		H	H	L	H									1/2000
	H	H		H	H	H	L									1/4000
	H	H		H	H	H	H									1/10000
	H	H	L	L												1/100
	H	H	H	L												1/120
	H	L														H
Serial mode P/S=L FL=H EN=H	L	H		H						H		H	L	L	L	1/60 Note)
	L	H		H						H		H	L	L	H	1/125
	L	H		H						H		H	L	H	L	1/250
	L	H		H						H		H	L	H	H	1/500
	L	H		H						H		H	H	L	L	1/1000
	L	H		H						H		H	H	L	H	1/2000
	L	H		H						H		H	H	H	L	1/4000
	L	H		H						H		H	H	H	H	1/10000
	L	H	H	H						H	H	L				1/100
	L	H	H	H						H	L	L				1/120
	L	H	L	H						H	H	L				1/100
	L	H	L	H						H	L	L				1/120
	L	H		H						L						H
Serial mode parallel CTL P/S=L	L	H	L	L												1/100
	L	H	H	L												1/120
	L	L														H

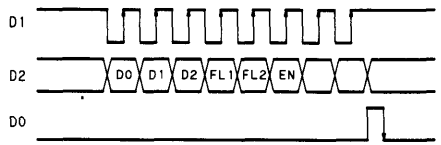
MODE 3 CR/NT
MODE 4 P/S

Abbreviations P : Parallel input S : Serial input
CR : PAL NT : NTSC

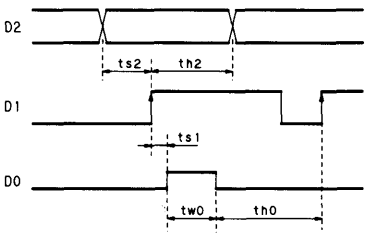
Note) 1/30 at accumulating NTSC frame.

AC Characteristics

In serial input mode (MODE4=L)



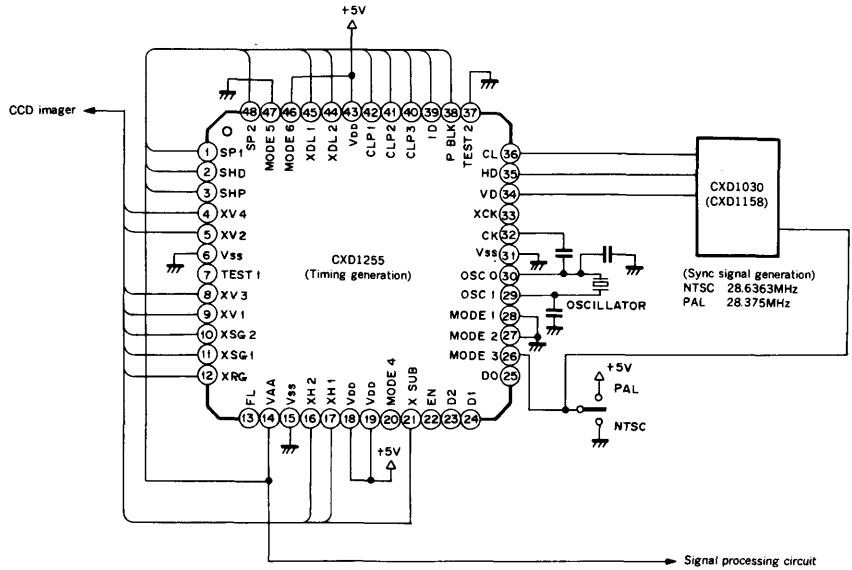
Mode setting in serial input



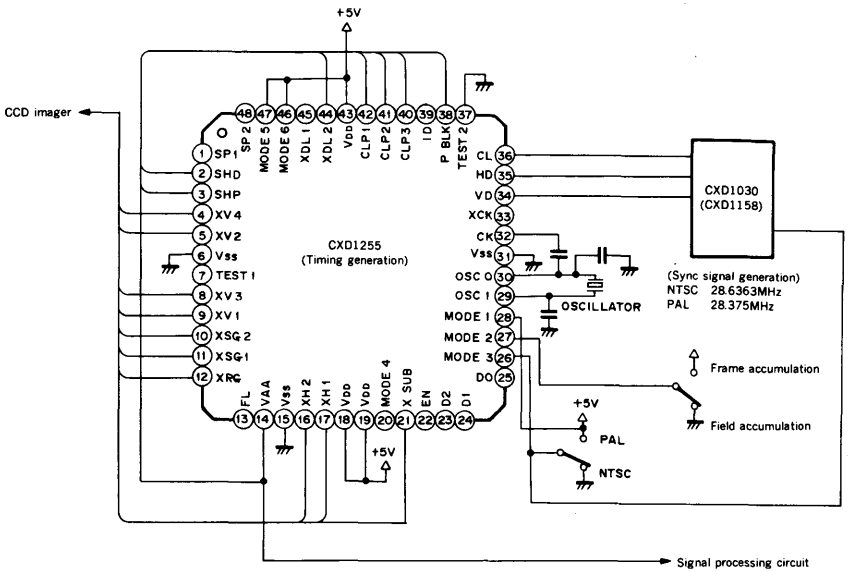
Symbol	Item	MIN
ts2	D2 set up time vs. D1 raising	20ns
th2	D2 hold time vs. D1 raising	20ns
ts1	D1 raising set up time vs. D0 raising	20ns
tw0	D0 pulse width	20ns
th0	D1 raising timing vs. D0 falling	20ns

Applicaiton circuit

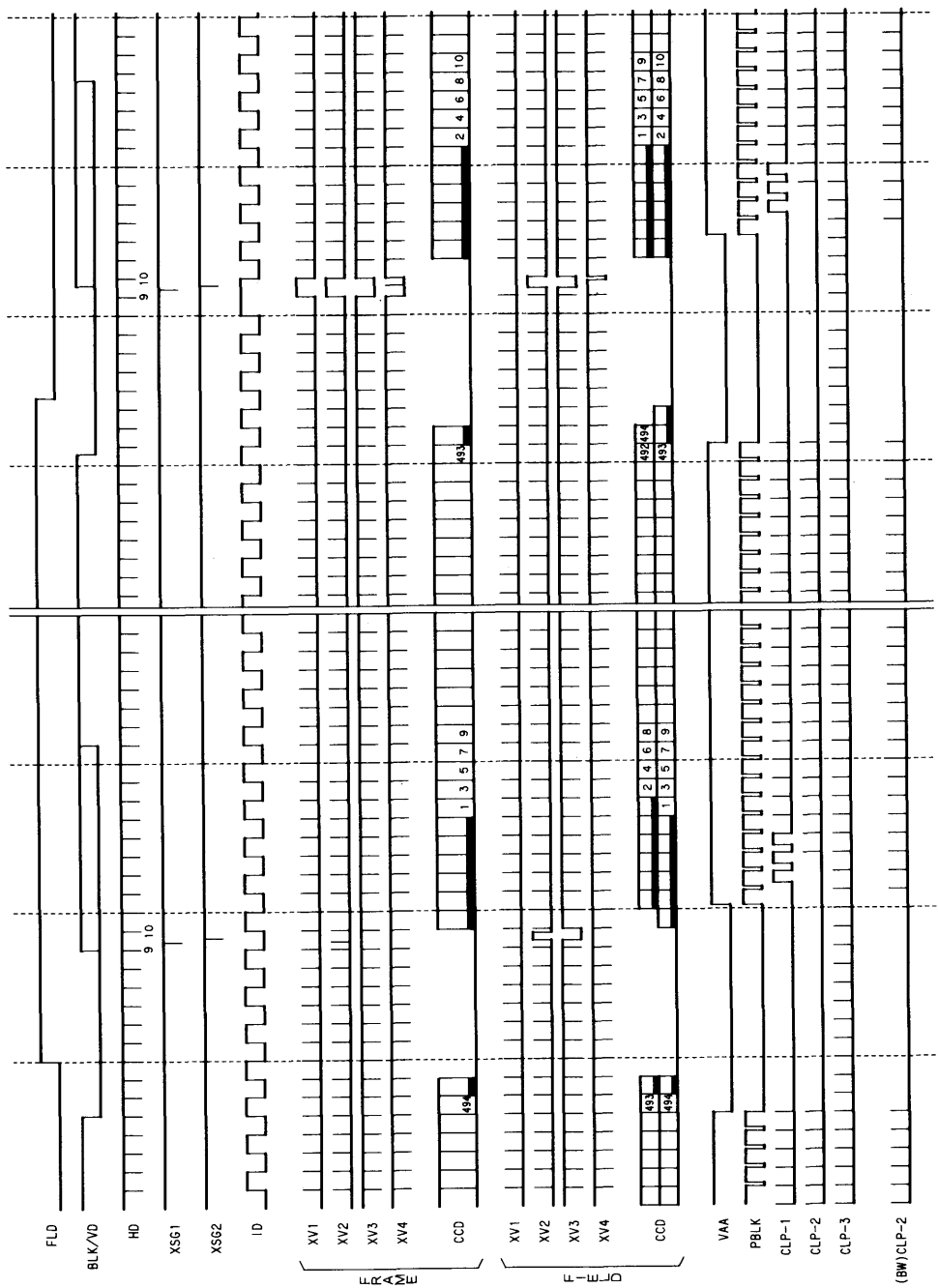
<Color mode>



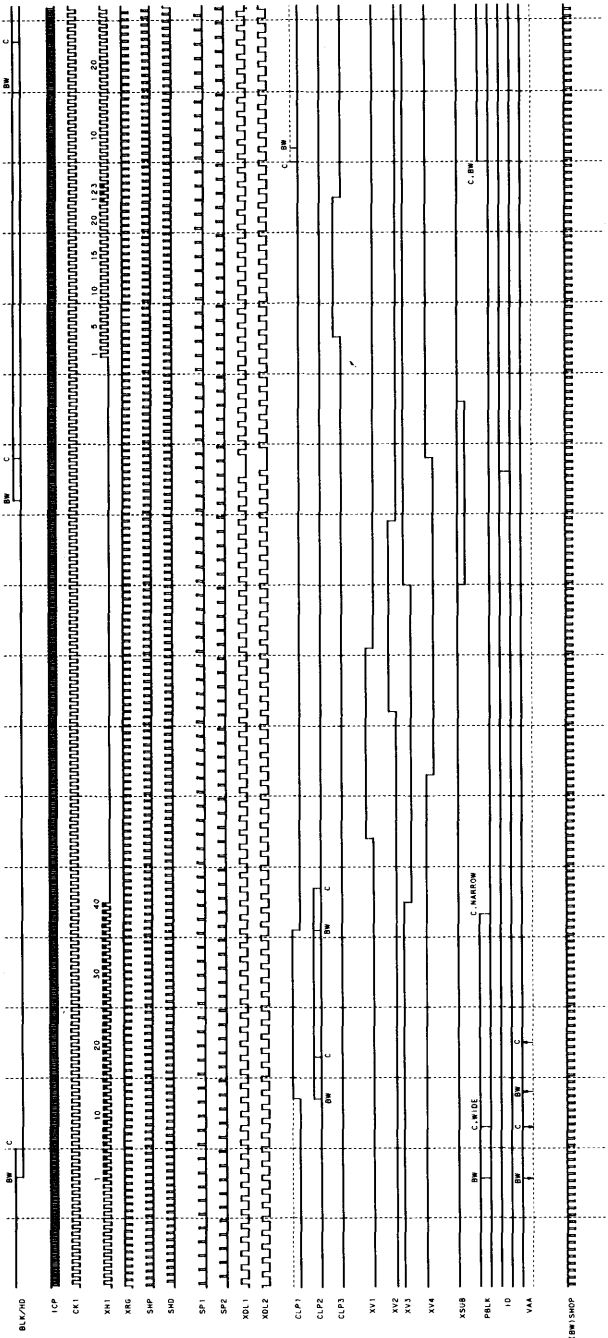
<B/W mode>



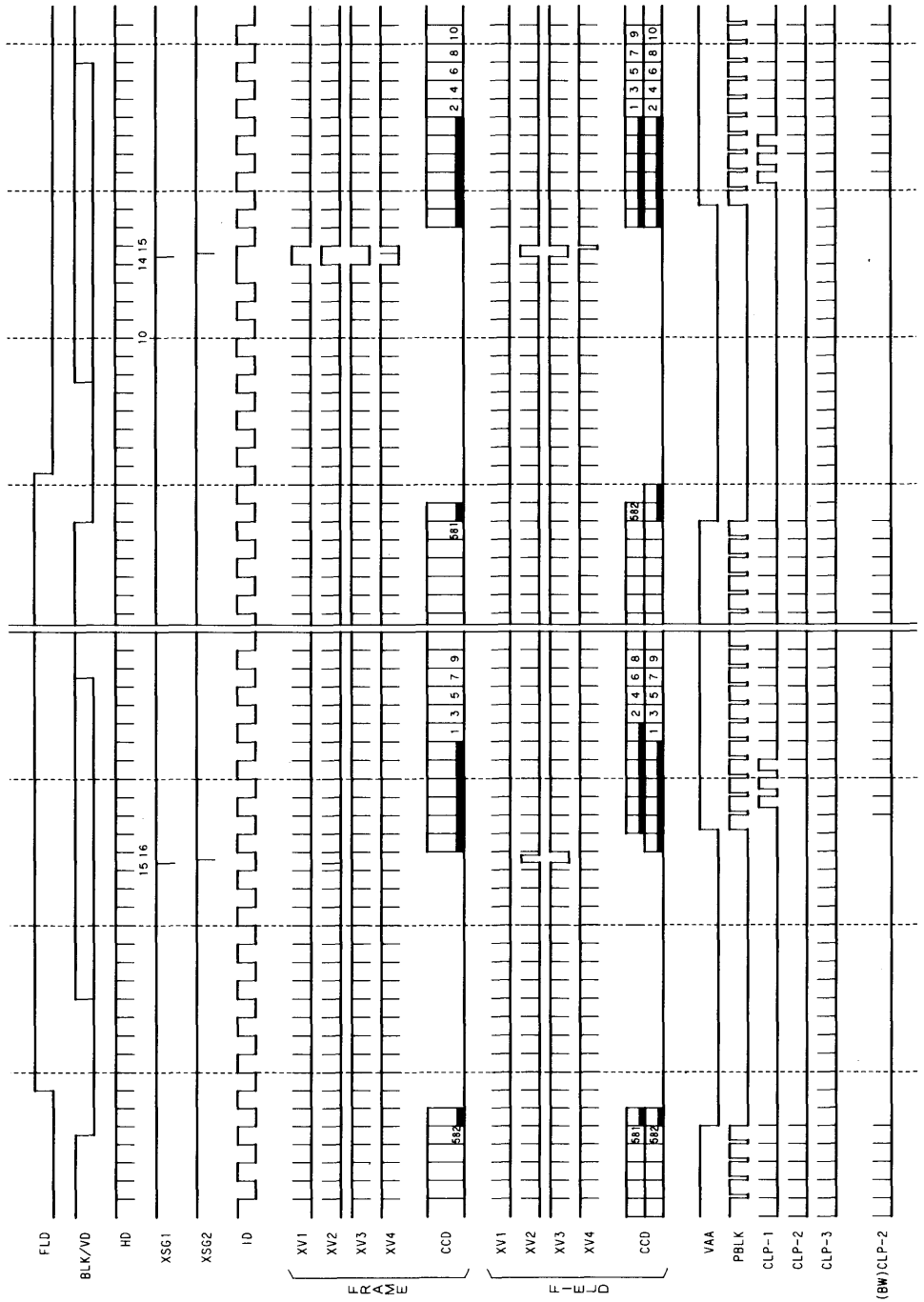
NTSC (EIA) Vertical



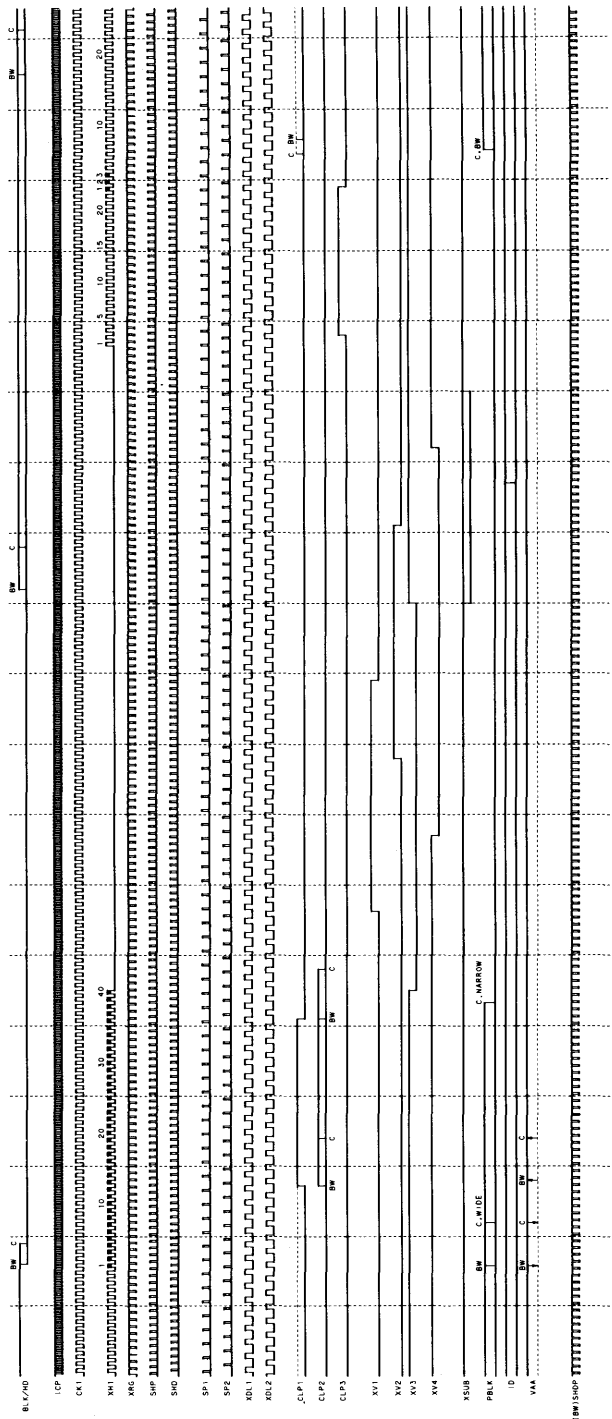
NTSC (EIA) Horizontal



PAL (CCIR) Vertical

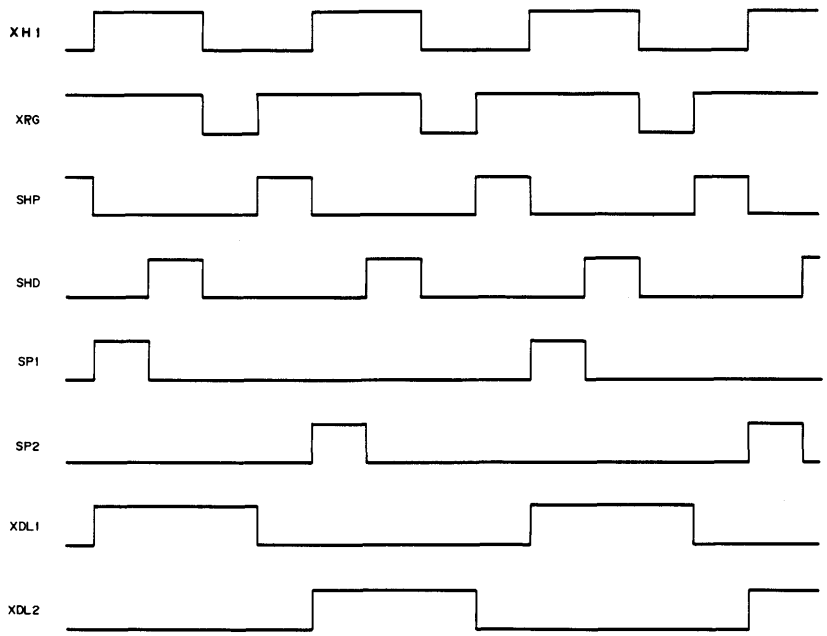


PAL (CCIR) Horizontal

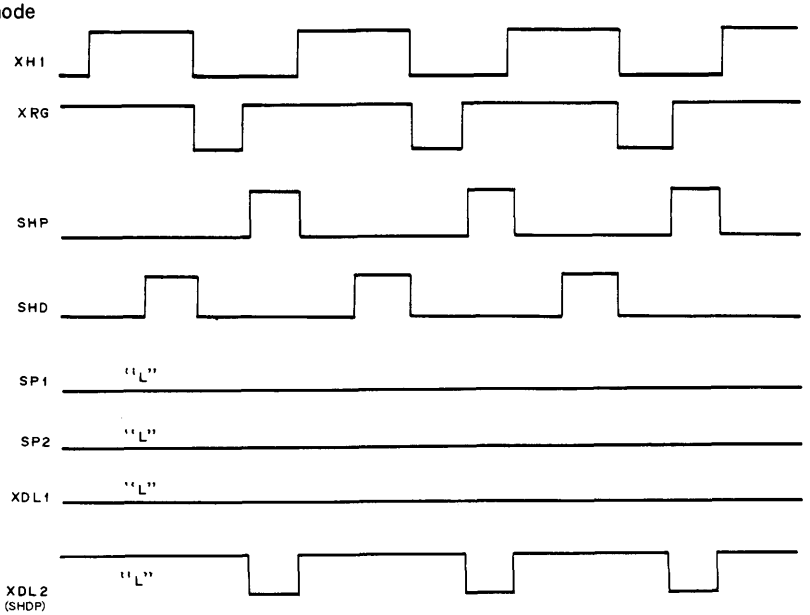


High-speed clock detailed timing

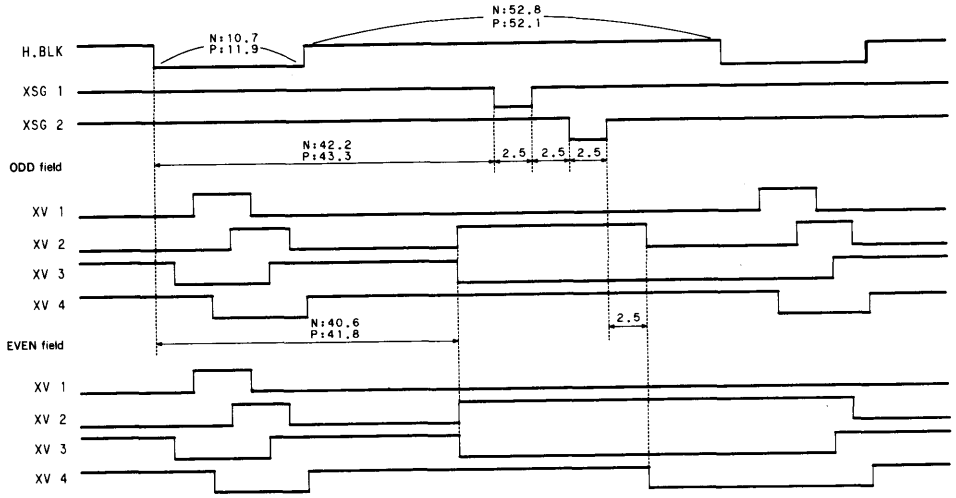
1. Color mode



2. B/W mode



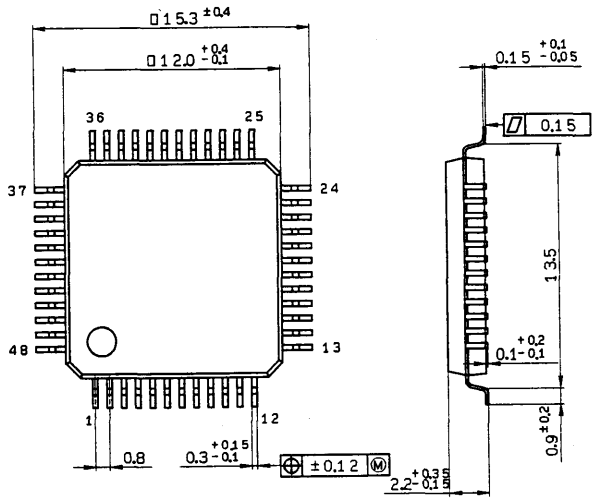
Readout period extension chart



Unit: μS

Package Outline Unit: mm

48pin QFP (Plastic) 0.6g



QFP-48P-L04

SONY

CXB0026AM

CCD Driver

Description

CXB0026AM is a special version of CXB0026M with the following improvements:

1) High frequency operation ability.
2) Improved output voltage amplitude (voltage usage ratio).

Other specifications match those of CXB0026M.

Features

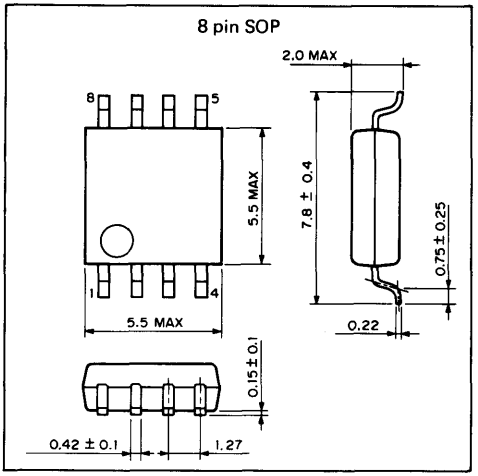
- High frequency operation ability.
- Improved output voltage amplitude.
- TTL compatible input.
- High output current drive.
- 2.0 mW low consumption when input at low level.

Structure

Bipolar silicon monolithic IC

Package Outline

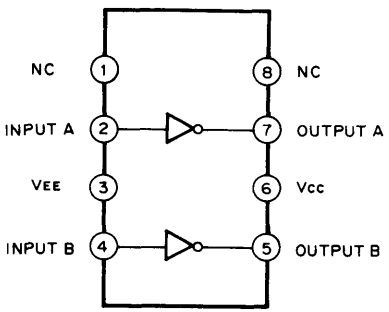
Unit: mm



Absolute Maximum Ratings (Ta=25°C)

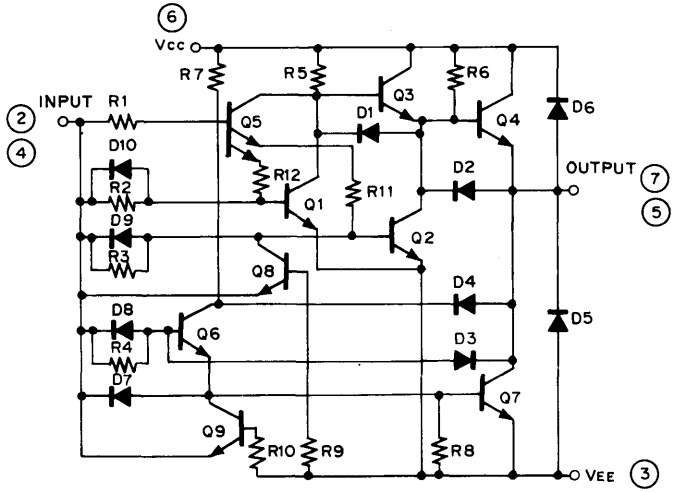
• Supply voltage	V_{CC-EE}	22	V
• Input current	I_I	100	mA
• Input voltage	V_I	V_{EE}+5.5	V
• Instant output current	Iopk	±1.5	A
• Junction temperature	T_J	+150	°C
• Operating temperature	Ta	0 to 70	°C
• Storage temperature	Tstg	−65 to 150	°C
• Allowable power dissipation (Ta=70°C, PC Board Mount)	P_D	400	mW

Pin Configuration



70847A-ST

Equivalent Circuit



Electrical Characteristics

Ta=0 to 70°C, $V_{CC}-V_{EE}$=10 to 20V, C_L=1000 pF, Ta=25°C (Typ.)

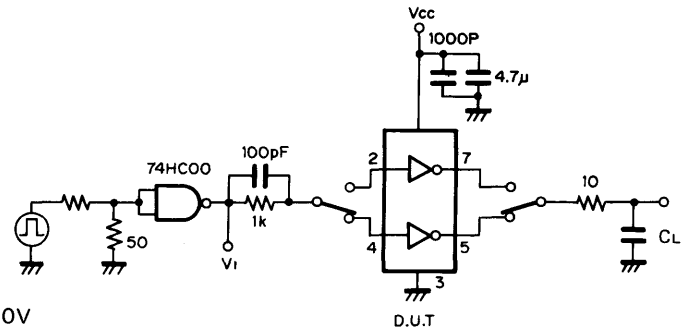
Item	Symbol	Min.	Typ.	Max.	Unit
H level input voltage $V_O=V_{EE}+1.0$ Vdc	V_{IH}	$V_{EE}+2.0$	$V_{EE}+1.5$	–	V
H level input current $V_I-V_{EE}=2.4$ Vdc, $V_O=V_{EE}+1.0$ Vdc	I_{IH}	–	10	15	mA
L level input $V_O=V_{CC}-1.0$ Vdc	V_{IL}	–	$V_{EE}+0.6$	$V_{EE}+0.4$	V
L level input current $V_I-V_{EE}=0$ Vdc, $V_O=V_{CC}-1.0$ Vdc	I_{IL}	–	−0.005	−10	mA
Output voltage at L level input $V_I-V_{EE}=0.4$ Vdc	V_{OH}	$V_{CC}-1.0$	$V_{CC}-0.7$	–	V
Output voltage at H level input $V_I-V_{EE}=2.4$ Vdc	V_{OL}	–	$V_{EE}+0.5$	$V_{EE}+1.0$	V
Supply current at ON (1 circuit) $V_{CC}-V_{EE}=20$ Vdc, $V_I-V_{EE}=2.4$ Vdc	I_{CCL}	–	30	40	mA
Supply current at OFF (1 circuit) $V_{CC}-V_{EE}=20$ Vdc, $V_I-V_{EE}=0$ Vdc	I_{CCH}	–	10	100	μA

Switching Characteristics

V_{CC}=7V, V_{EE}=0V, Ta=25°C, C_L=270P

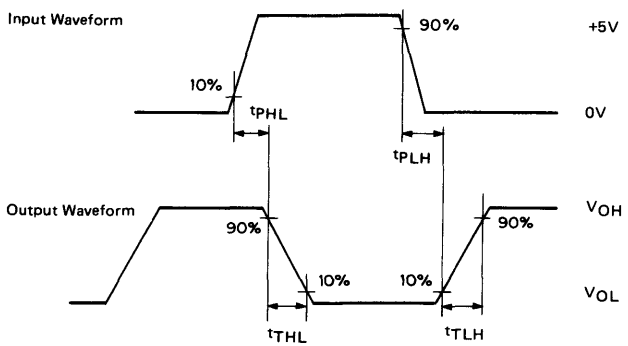
Item	Symbol	Min.	Typ.	Max.	Unit
Clock level	$V_{OH}-V_{OL}$	$V_{CC}-0.5$	–	V_{CC}	V
Propagation time (H→L)	t_{PHL}	4.75	–	6.75	ns
Propagation time (L→H)	t_{PLH}	–	–	14	ns
Transition time (H→L)	t_{THL}	–	–	11	ns
Transition time (L→H)	t_{TLH}	–	–	17	ns

Characteristics Test Circuit



* V_I=5.0V
f=14 MHz
$t_{TLH}=t_{THL}\leqq 8$ns
Duty 50%

I/O Waveforms



SONY CX20180/CXA1180N

Vertical Clock Driver for CCD Imager

Description

CX20180 and CXA1180N are ICs which have been developed as a large capacitor drive for the vertical clock driver, etc. of the CCD imager. These are provided with the functions of incorporating almost all of the circuit necessary to the vertical clock driver of the CCD imager.

Features

- Low power consumption : 76 mW during CCD imager pick up ICX021 drive.
- High efficiency power supply : Obtains the almost same amplitude of power supply voltage
- Built-in interference suppression circuit : Suppression voltage approximately 0.4V.
- Built-in almost all functions necessary to vertical driver circuits.
  1. Provided with 4 independent CCD imager driver blocks.
  2. Provided with inverter block for generating read out pulse.
  3. Provided with inverter block for generating negative voltage.
  4. Provided with saving circuit power consumption.

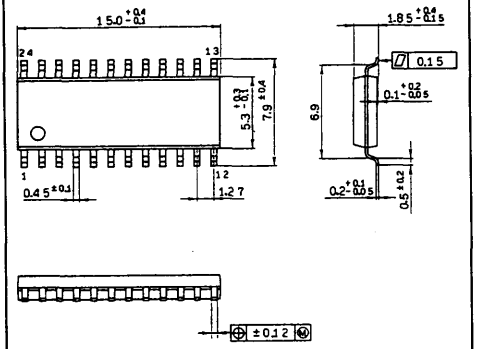
Structure

Bipolar silicon monolithic IC

Package Outline

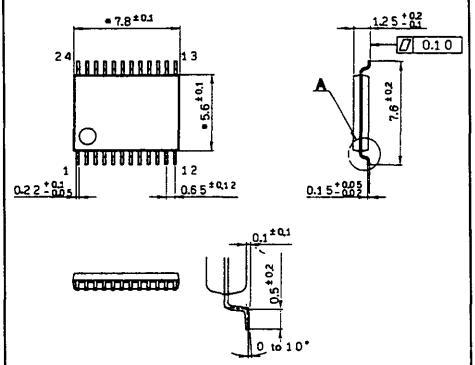
Unit : mm

CX20180 24 pin SOP (Plastic)



SOP-24P-L01

CXA1180N 24 pin VSOP (Plastic)



VSOP-24P-L01

Absolute Maximum Ratings (Ta = 25°C)

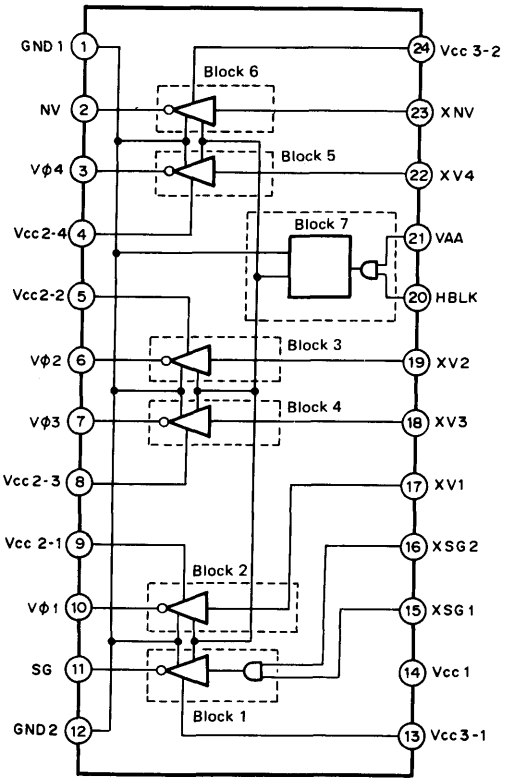
• Input step bias voltage	V_{CC1}	6	V
• Output step bias voltage	V_{CC2-1}	25	V
	V_{CC2-2}	25	V
	V_{CC2-3}	25	V
	V_{CC2-4}	25	V
	V_{CC3-1}	25	V
	V_{CC3-2}	25	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	CX20180 830 mW	CXA1180N 560 mW

Recommended Operating Conditions

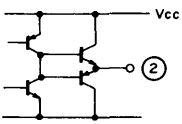
• Input step bias voltage	V_{CC1}	4.5 to 5.5	V
• Output step bias voltage	V_{CC2-1}	5.5 to 23	V
	V_{CC2-2}	5.5 to 23	V
	V_{CC2-3}	5.5 to 23	V
	V_{CC2-4}	5.5 to 23	V
	V_{CC3-1}	5.5 to 23	V
	V_{CC3-2}	5.5 to 23	V

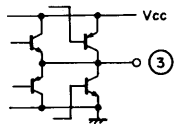
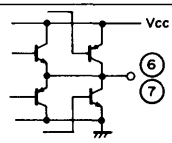
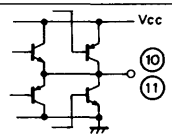
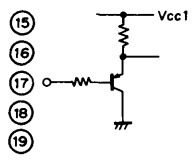
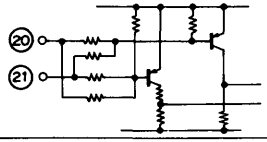
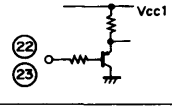
80846 – ST

Block Diagram and Pin Configuration (Top View)



Pin Description and Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1	GND1		Ground
2	NV		Drive signal output of negative voltage generating circuit.

No.	Symbol	Equivalent circuit	Description
3	V φ 4		Output of imager drive circuit 4.
4	Vcc2-4		Output stage bias power supply of imager drive circuit 4.
5	Vcc2-2		Output stage bias power supply of imager drive circuit 2.
6	V φ 2		Output of imager drive circuit 2.
7	V φ 3		Output of imager drive circuit 3.
8	Vcc2-3		Output stage bias power supply of imager drive circuit 3.
9	Vcc2-1		Output stage bias power supply of imager drive circuit 1.
10	V φ 1		Output of imager drive circuit 1.
11	SG		Output of inverter for generating read out pulse.
12	GND2		Ground
13	Vcc3-1		Output stage bias power supply of inverter for generating read out pulse.
14	Vcc1		Power supply of respective input stage and bias circuit.
15	XSG1		Input 1 of inverter for generating read out pulse.
16	XSG2		Input 2 of inverter for generating read out pulse.
17	XV1		Input of imager drive circuit 1.
18	XV3		Input of imager drive circuit 3.
19	XV2		Input of imager drive circuit 2.
20	HBLK		Input 1 of power saving circuit.
21	VAA		Input 2 of power saving circuit.
22	XV4		Input of imager drive circuit 4.
23	XNV		Input of drive circuit of negative voltage generating and rectifier circuit.
24	Vcc3-2		Power supply of drive circuit of negative voltage generating and rectifier circuit.

Electrical Characteristics (Ta = 25 °C)

DC characteristics

During open state of output Pin.

Measuring condition (See the DC Characteristics Test Circuit.)

$V_{CC}1 = 5V$ $V_{CC}2\text{-}4 = 11V$
$V_{CC}2\text{-}1 = 11V$ $V_{CC}3\text{-}1 = 11V$
$V_{CC}2\text{-}2 = 11V$ $V_{CC}3\text{-}2 = 11V$
$V_{CC}2\text{-}3 = 11V$

Item	Symbol	Test condition	Input H			Input L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input current of XV1, XV2, XV3, XV4 or XNV	$I_{IN}XV$			0.10	15	−15	−2.5		μA
Input current of XSG1	$I_{IN}XSG1$	XSG2···H		0.03	15	−15	−2.5		μA
Input current of XSG2	$I_{IN}XSG2$	XSG1···L		0.03	15	−15	−2.5		μA
Input current of HBLK or VAA	$I_{IN}HBLK$ $I_{IN}VAA$	VAA···L during HBLK···H VAA···H during HBLK···L		55	100	−500	−300		μA
Input voltage H level			4.95						V
Input voltage L level	$V_{IN\ H}$							0.05	V

Item	Symbol	Test condition	Ouput H			Ouput L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output clip level	$V_{O\ CLP}$			11.1	11.45	−0.47	−0.38		V

(See the Test Circuit)

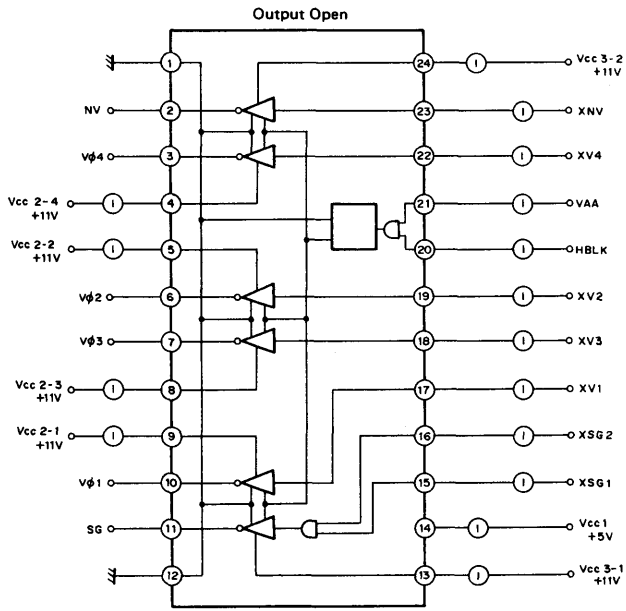
Item (Consumption current)	Symbol	HBLK···L VAA···L				BLK···H VAA···H				Unit	Remarks
		Input H		Input L		Input H		Input L			
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
$V_{CC}2\text{-}1$ or $V_{CC}2\text{-}2$	$I_{CC}2\text{-}1$ $I_{CC}2\text{-}2$	2.0	2.5	2.3	3.0	3.4	4.5	0.5	1.0	mA	Input indicates XV1 or XV2
$V_{CC}2\text{-}3$ or $V_{CC}2\text{-}4$ or $V_{CC}3\text{-}1$	$I_{CC}2\text{-}3$ $I_{CC}2\text{-}4$ $I_{CC}3\text{-}1$	2.0	2.5	2.3	3.0	0.5	1.0	3.4	4.5	mA	Input indicates XV3 or XV4 or XSG1 or XSG2
$V_{CC}3\text{-}2$	$I_{CC}3\text{-}2$	1	100	200	300	1	100	300	500	μA	Input indicates XNV
$V_{CC}1$	$I_{CC}1$	2.0	2.7	3.8	4.8	1.2	1.6	3.1	3.9	mA	Input indicates all input pins except HBLK and VAA

Characteristics during CCD imager ICX021 drive

$V_{CC}1 = 5V$, $V_{CC}2 = 7.5V$, $V_{CC}3 = 11V$ (See the Characteristics Test Circuit during the operating)

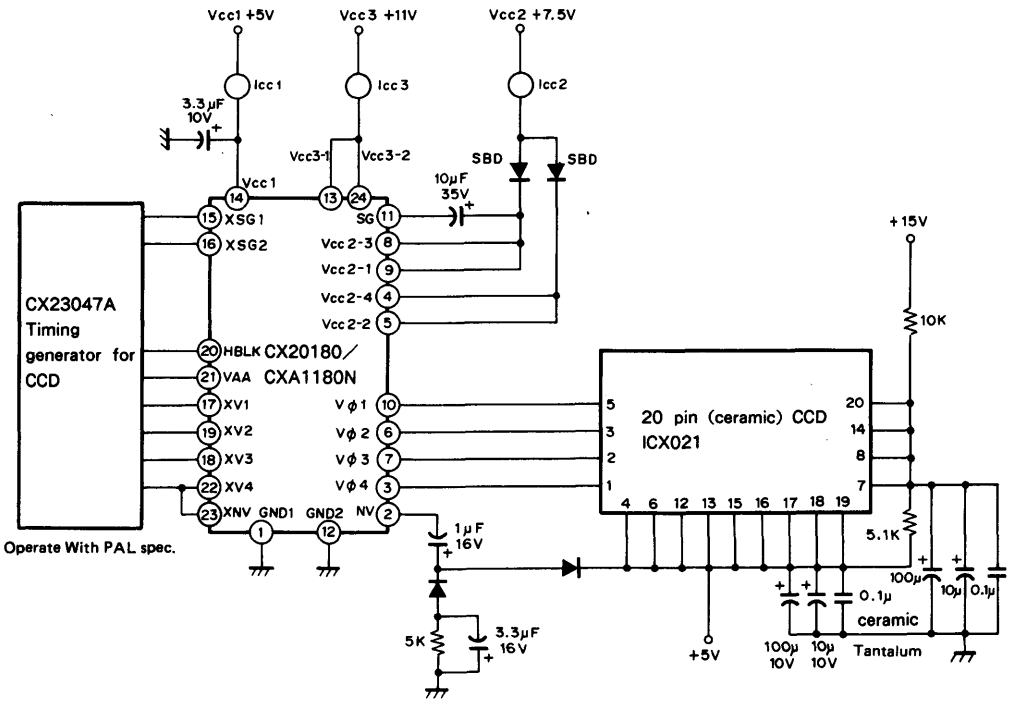
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Subsequent to XV1 becoming H level, the V φ 1 output level after T1 sec	$V\phi 1_L$	T1 = 590 ns		0.22	0.4	V
Subsequent to XV2 becoming H level, the V φ 2 output level after T1 sec	$V\phi 2_L$	T1 = 530 ns		0.22	0.4	V
Subsequent to XV3 becoming H level, the V φ 3 output level after T1 sec	$V\phi 3_L$	T1 = 590 ns		0.22	0.4	V
Subsequent to XV4 becoming H level, the V φ 4 output level after T1 sec	$V\phi 4_L$	T1 = 500 ns		0.1	0.4	V
Subsequent to XV1 becoming L level, the V φ 1 output level after T2 sec	$V\phi 1_H$	T2 = 1.47 μs	6.8	7.2		V
Subsequent to XV2 becoming L level, the V φ 2 output level after T2 sec	$V\phi 2_H$	T2 = 1.18 μs	6.8	7.2		V
Subsequent to XV3 becoming L level, the V φ 3 output level after T2 sec	$V\phi 3_H$	T2 = 1.24 μs	6.8	7.2		V
Subsequent to XV4 becoming L level, the V φ 4 output level after T2 sec	$V\phi 4_H$	T2 = 1.17 μs	6.8	7.2		V
Current consumption $V_{CC}1$	$I_{CC}1$		1.4	2.0	2.5	mA
Current consumption $V_{CC}2$	$I_{CC}2$		5.0	7.0	9.0	mA
Current consumption $V_{CC}3$	$I_{CC}3$		1.0	1.5	2.0	mA

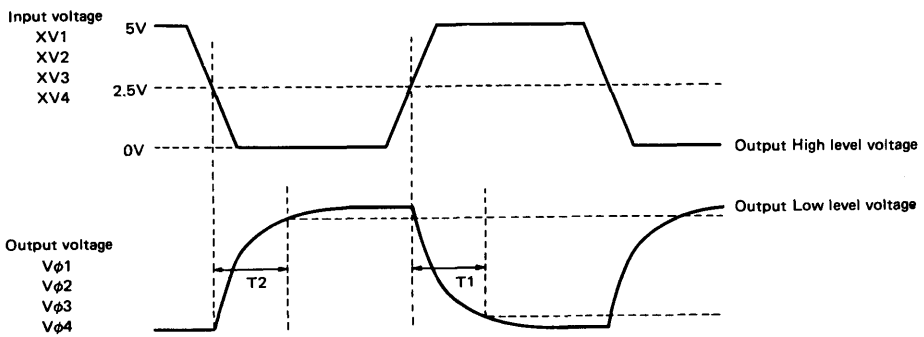
DC Characteristics Test Circuit



Electrical Characteristics Test Circuit

(During CCD Imager ICX021 drive)





Standard Circuit Designing Material

DC characteristics

When right circuit has been constructed

DC current during all inputs have been set to "L"

Icc1 = 3.8 mA

Icc2 = 9.2 mA

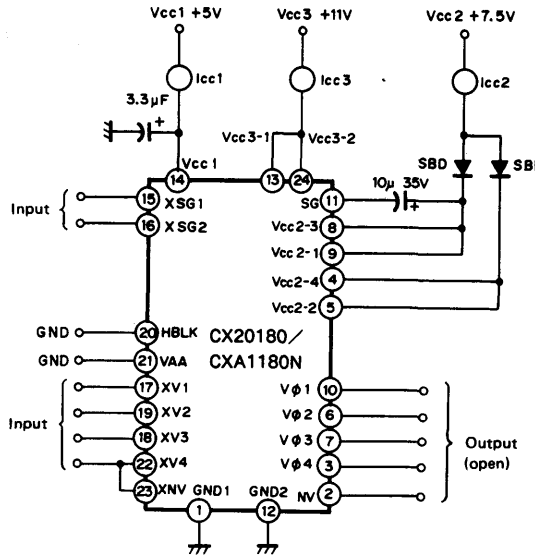
Icc3 = 2.5 mA

DC current during all inputs have been set to "H"

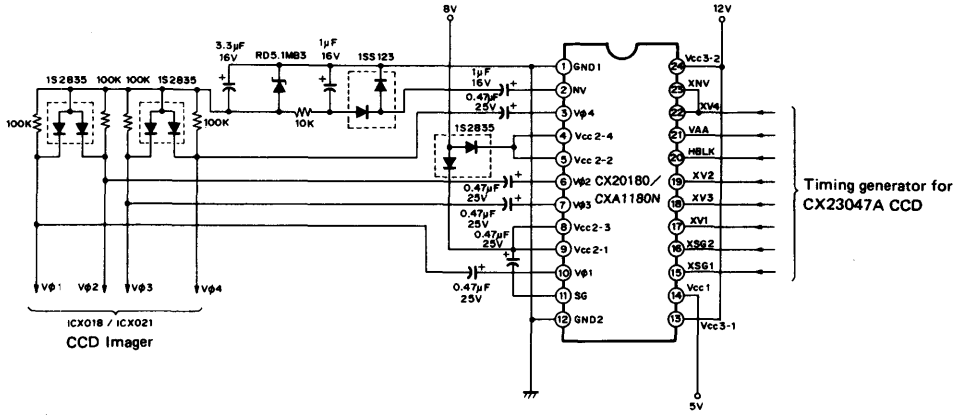
Icc1 = 2.0 mA

Icc2 = 8.0 mA

Icc3 = 2.0 mA



Application Circuit



Operation

CX20180 and CXA1180N are composed of 7 blocks necessary to the V clock driver, and these are compact and enable to drive of the CCD imager with low power consumption. (See the Block Diagram.)

Block 1, SG2 input inverter circuit

Inverter which has 2 input AND Gate as the input, and it is a block used to produce read out pulse outside of the IC.

Block 2 to 5 inverter circuit

Inverter which has 4 entirely identical circuit compositions, and these actually drive the CCD imagers. These drive circuits build-in interference suppressed circuits so as not to accept interference due to junction capacity among phases of the CCD.

Block 6 negative voltage generating circuit

Output pulse of this block is rectified and made into negative voltage with the external circuit, and applied to signals of blocks 2 to 5.

Block 7 power save mode and normal mode

Performs switchover of Power save mode * and Normal mode * of blocks 1 to 6. Input is of 2 input AND gate.

***Power save mode and normal mode**

This IC supplies output stage drive current during blanking period only as low power consumption is realized when used to drive CCD imager. Effective use of electrical power is exercised by saving the output stage drive current during other periods. Power save mode is a mode in which the output stage drive current is saved, and Normal mode is defined as a mode in which the general drive current is flowed fully.

Power save mode
HBLK··· "H" VAA··· "H"
Normal mode
HBLK··· "L" VAA··· "L"
HBLK··· "H" VAA··· "L"
HBLK··· "L" VAA··· "H"
Bias circuit is built-in.

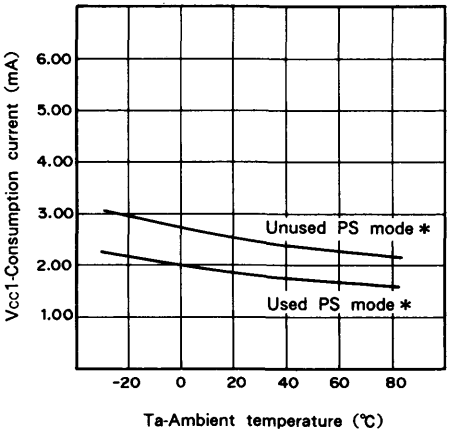
Note on Use

- Special care should be taken for the following points on printed circuit board design.
  During CCD image device driving, a large inrush current flows.
  1. Connect the grounding pin of IC and the grounding pattern of printed circuit board in the shortest distance.
  2. Connect the decoupling capacitor and the grounding pattern of printed circuit board in the shortest distance.

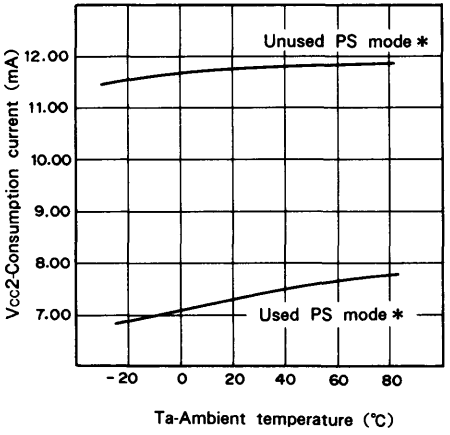
- Driving condition
  1. A general purpose CMOS IC can be used to drive this IC. The input current is maximum 500 μA.
  2. Wiring of the input signal line of the drive should be made as short as possible to keep it away from the effect of stray capacitance.
  3. There may be a possibility of ringing due to the inductance of the line, if wiring of the output signal line is long. In the event that, countermeasure for it should be performed by inserting resistors in series to the signal line, etc.
  4. There may be possibility of causing an operational error, if there is a voltage difference between the CMOS IC which drive this IC and the bias voltage of $V_{CC}1$ of this IC, therefore, the $V_{CC}1$ and the CMOS IC Bias should use the same power supply.

Characteristics during CCD imager ICX021 drive. (See the Electrical Characteristics Test Circuit)

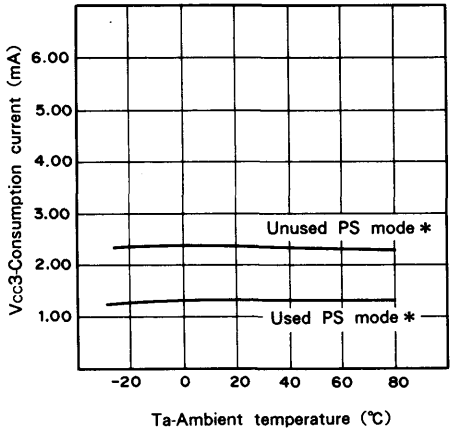
$V_{CC}1$ consumption current vs. Ambient temperature



$V_{CC}2$ consumption current vs. Ambient temperature

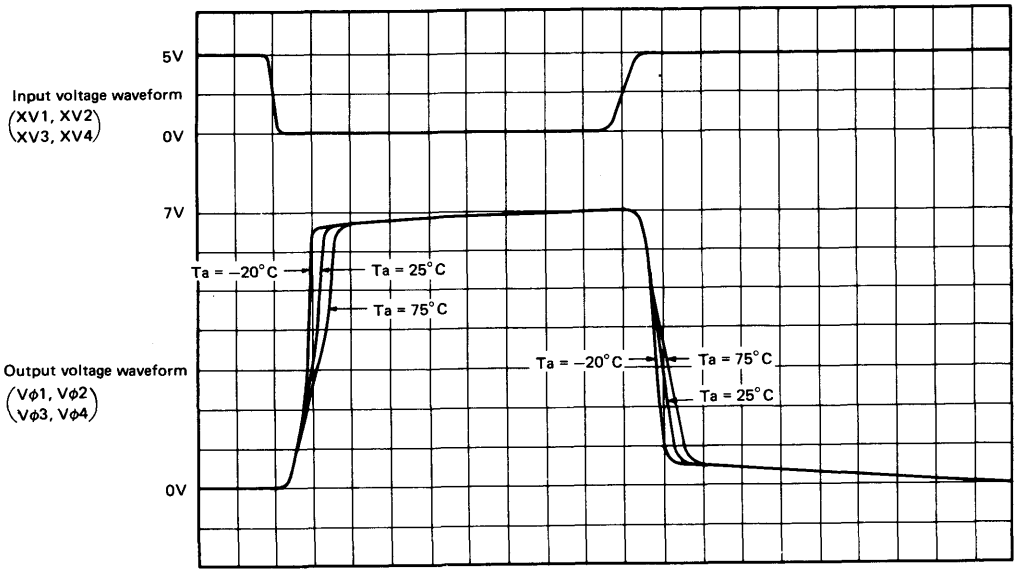


$V_{CC}3$ consumption current vs. Ambient temperature

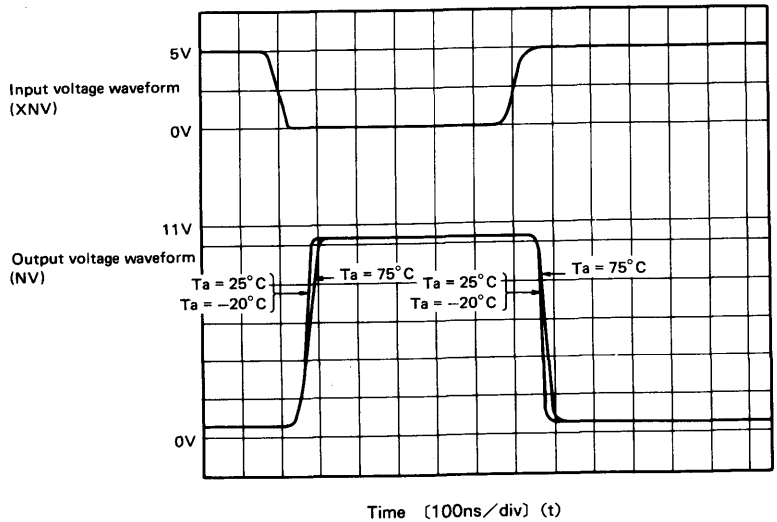


*) P.S mode : See power save mode.

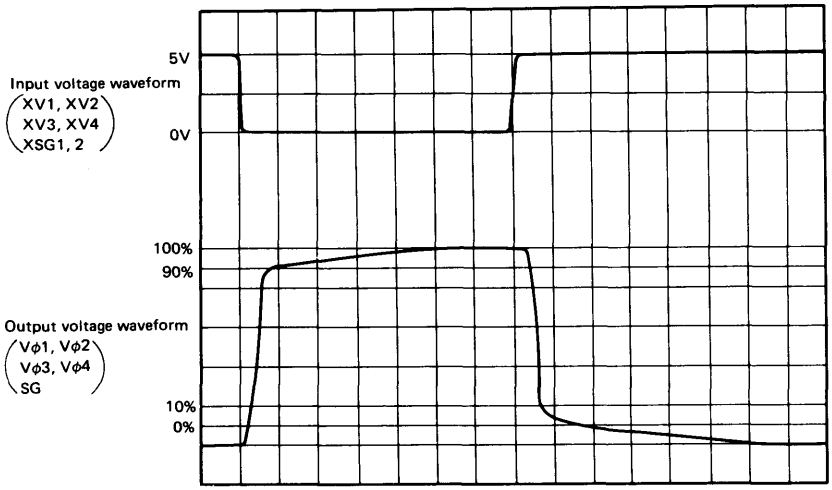
Temperature characteristics of rising and falling waveforms of output voltage V φ 1, V φ 2, V φ 3 and V φ 4



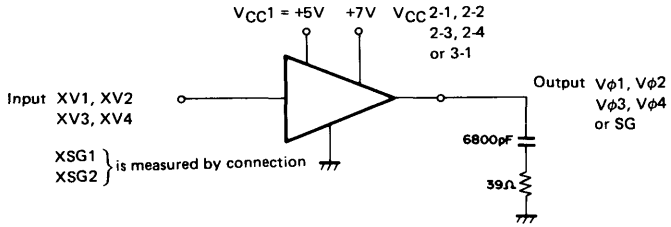
Temperature characteristics of rising and falling waveforms of NV output voltage



Rising and falling waveforms of V φ 1, V φ 2, V φ 3 and V φ 4 SG output voltage at capacity load (Normal mode)



Test Circuit



SONY

CXA1065M

Vertical clock driver for CCD imagers

Description

The CXA1065M is a bipolar IC developed to drive the vertical shift register of CCD imagers (ICX022 etc.).

It is composed of seven drivers that can drive large capacitors with wide voltage amplitude. A suppressing function of coupling between phases reduces blooming and smear to make this IC ideal for vertical clock driving of CCD imaging devices.

Features

- Almost all functions required for vertical clock driving of CCD imager are provided.
- Negative voltage source is not needed.
- Suppressing function of coupling between phases.
- Wide output amplitude — Output voltage amplitude is almost equal to supply voltage.
- Wide operating voltage range −5.5 to +25 V
- Low power consumption with the built-in power-saving circuit — 116 mW Typ. when the ICX022 equivalent circuit load is driven.

Structure

Silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

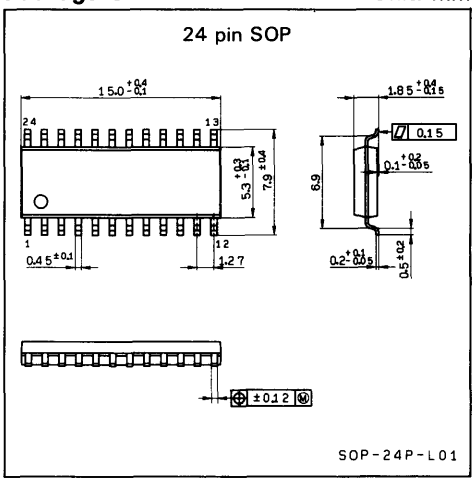
• Supply voltage	$V_{CC}1$	6	V
	$V_{CC}2$-1	27	V
	$V_{CC}2$-2	27	V
	$V_{CC}2$-3	27	V
	$V_{CC}2$-4	27	V
	$V_{CC}3$	27	V
	$V_{CC}4$	27	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	560	mW

Recommended Operating Conditions

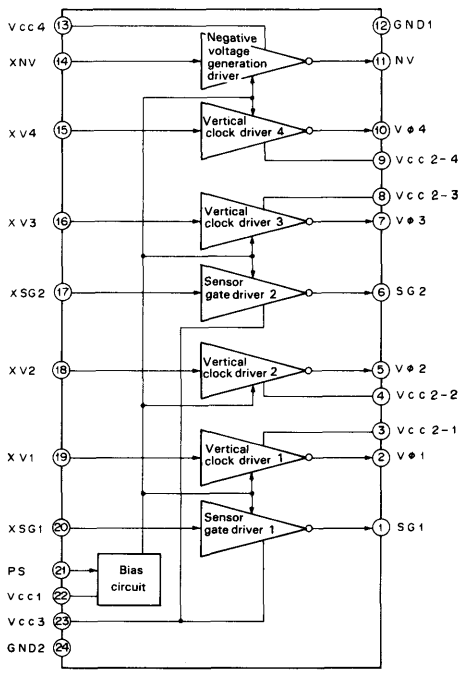
$V_{CC}1$	4.5 to 5.5	V
$V_{CC}2$-1	5.5 to 25	V
$V_{CC}2$-2	5.5 to 25	V
$V_{CC}2$-3	5.5 to 25	V
$V_{CC}2$-4	5.5 to 25	V
$V_{CC}3$	5.5 to 25	V
$V_{CC}4$	5.5 to 25	V

Package Outline

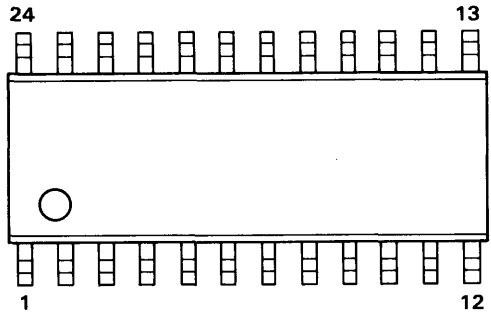
Unit: mm



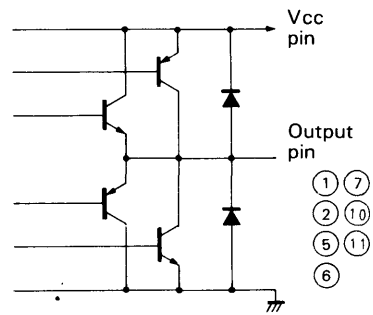
Block Diagram

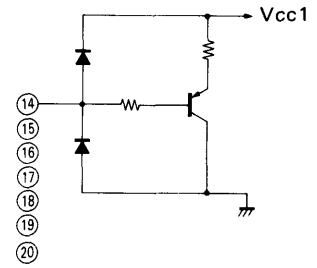
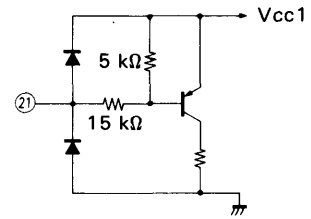


Pin Configuration (Top View) and Description



No.	Symbol	Description	Equivalent circuit
		Function of each driver is inverter. Truth table: Input L → Output H; Input H → Output L	
1	SG1	Sensor gate driver 1	Output pins
2	Vφ1	Vertical clock driver 1	
5	Vφ2	Vertical clock drivr 2	
6	SG2	Sensor gate driver 2	
7	Vφ3	Vertical clock driver 3	
10	Vφ4	Vertical clock driver 4	
11	NV	Negative voltage generation driver	
3	Vcc2-1	Vertical clock driver 1	Vcc pins
4	Vcc2-2	Vertical clock driver 2	
8	Vcc2-3	Vertical clock driver 3	
9	Vcc2-4	Vertical clock driver 4	
13	Vcc4	Negative voltage generation driver	
23	Vcc3	Sensor gate driver 1, 2	
12	GND1	GND	
24	GND2		



No.	Symbol	Description		Equivalent circuit
14	XNV	Negative voltage generation driver	Input pin	
15	XV4	Vertical clock driver 4		
16	XV3	Vertical clock driver 3		
17	XSG2	Sensor gate driver 2		
18	XV2	Vertical clock driver 2		
19	XV1	Vertical clock driver 1		
20	XSG1	Sensor gate driver 1		
21	PS	Input pin for the power-saving signal (For the power-saving function, refer to the Description of Functions.)		
22	Vcc1	Power supply of the bias circuit.		

Electrical Characteristics

DC characteristics

Ta = 25°C

V_{CC1} = 5V, $V_{CC2\text{-}1}$ = 12V, $V_{CC2\text{-}2}$ = 12V, $V_{CC2\text{-}3}$ = 12V, $V_{CC2\text{-}4}$ = 12V, V_{CC3} = 12V, V_{CC4} = 12V

With outputs open

Parameter			Symbol	Input condition (Blank 0V H 5V)								Min.	Typ.	Max.	Unit
				PS	XV1	XV2	XV3	XV4	XSG1	XSG2	XNV				
Input current into PS pin		Input current low level	I_{ILPS}									−500	−270		μA
		Input current high level	I_{IHPS}	H									0.03	15	μA
Input current into 7 drivers	Input current low level	XV1	I_{ILXV1}									−15	−2.5		μA
		XV2	I_{ILXV2}												
		XV3	I_{ILXV3}	H											
		XV4	I_{ILXV4}	H											
		XSG1	I_{ILXSG1}	H											
		XSG2	I_{ILXSG2}	H											
		XNV	I_{ILXNV}												
	Input current high level	XV1	I_{IHXV1}		H								0.03	15	μA
		XV2	I_{IHXV2}			H									
		XV3	I_{IHXV3}				H								
		XV4	I_{IHXV4}					H							
		XSG1	I_{IHXSG1}						H						
		XSG2	I_{IHXSG2}							H					
		XNV	I_{IHXNV}								H				
Input voltage	Low level		V_{IL}											0.05	V
	High level		V_{IH}									4.95			V

Parameter		Symbol	Input condition (Blank 0V, H 5V)								Min.	Typ.	Max.	Unit
			PS	XV1	XV2	XV3	XV4	XSG1	XSG2	XNV				
DC supply cuttent of bias circuit at V_{CC1}	PS: L All inputs: L	$I_{CC1\ LL}$									1.5	3.5	5.5	mA
	PS: L All inputs: H	$I_{CC1\ LH}$		H	H	H	H	H	H	H	0.5	1.7	3.0	mA
	PS: H All inputs: L	$I_{CC1\ HL}$	H								1.5	3.2	5.0	mA
	PS: H All inputs: H	$I_{CC1\ HH}$	H	H	H	H	H	H	H	H	0.5	1.3	2.5	mA
DC supply current of vertical clock driver 1 at $V_{CC2\text{-}1}$	PS: L XV1: L	$I_{CC2\text{-}1\ LL}$									0.5	2.0	3.0	mA
	PS: L XV1: H	$I_{CC2\text{-}1\ LH}$		H										
	PS: H XV1: L	$I_{CC2\text{-}1\ HL}$	H								0.1	0.5	1.0	mA
	PS: H XV1: H	$I_{CC2\text{-}1\ HH}$	H	H							1.5	3.2	5.0	mA
DC supply current of vertical clock driver 2 at $V_{CC2\text{-}2}$	PS: L XV2: L	$I_{CC2\text{-}2\ LL}$									0.5	2.0	3.0	mA
	PS: L XV2: H	$I_{CC2\text{-}2\ LH}$			H									
	PS: H XV2: L	$I_{CC2\text{-}2\ HL}$	H								0.1	0.5	1.0	mA
	PS: H XV2: H	$I_{CC2\text{-}2\ HH}$	H		H						1.5	3.2	5.0	mA
DC supply current of vertical clock driver 3 at $V_{CC2\text{-}3}$	PS: L XV3: L	$I_{CC2\text{-}3\ LL}$									0.5	2.0	3.0	mA
	PS: L XV3: H	$I_{CC2\text{-}3\ LH}$				H								
	PS: H XV3: L	$I_{CC2\text{-}3\ HL}$	H								1.5	3.2	5.0	mA
	PS: H XV3: H	$I_{CC2\text{-}3\ HH}$	H			H					0.1	0.5	1.0	mA
DC supply current of vertical clock driver 4 at $V_{CC2\text{-}4}$	PS: L XV4: L	$I_{CC2\text{-}4\ LL}$									0.5	2.0	3.0	mA
	PS: L XV4: H	$I_{CC2\text{-}4\ LH}$					H							
	PS: H XV4: L	$I_{CC2\text{-}4\ HL}$	H								1.5	3.2	5.0	mA
	PS: H XV4: H	$I_{CC2\text{-}4\ HH}$	H				H				0.1	0.5	1.0	mA
DC supply current of sensor gate drivers 1, 2 at V_{CC3}	PS: L XSG1, 2: L	$I_{CC3\ LL}$									1.0	4.0	6.0	mA
	PS: L XSG1, 2: H	$I_{CC3\ LH}$						H	H					
	PS: H XSG1, 2: L	$I_{CC3\ HL}$	H								3.0	6.4	10.0	mA
	PS: H XSG1, 2: H	$I_{CC3\ HH}$	H					H	H		0.1	0.7	1.4	mA
DC supply current of negative voltage generation driver at V_{CC4}	XNV: L	$I_{CC4\ L}$									0.5	2.0	3.0	mA
	XNV: H	$I_{CC4\ H}$								H				

Characteristics when CXA1065M drives the equivalent circuit of CCD imager, ICX022

Supply current

$Ta = 25°C$, $V_{CC1} = 5V$, $V_{CC2} = 10.6V$, $V_{CC3} = 13.4V$, $V_{CC4} = 10.6V$
The CXD1035B (timing generator) is used as the input signal source.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current at V_{CC1}	I_{CC1}		0.5	1.9	3.0	mA
Supply current at V_{CC2}	I_{CC2}		3.0	7.1	8.5	mA
Supply current at V_{CC3}	I_{CC3}		0.2	0.8	1.5	mA
Supply current at V_{CC4}	I_{CC4}		0.5	2.0	3.0	mA

Output waveform of each driver

$Ta = 25°C$, $V_{CC1} = 5V$, $V_{CC2} = 10V$, $V_{CC3} = 13.4V$, $V_{CC4} = 10.6V$
The CXD1035B (timing generator) is used as the input signal source.

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Output waveform of negative voltage generation driver	Falling edge voltage	V_{NVL}	Voltage at NV at 350ns after XNV rising edge	0.05	0.71	1.15	V
	Rising edge voltage	V_{NVH}	Voltage at NV at 350ns after XNV falling edge	9.45	10.13	10.55	V
	L level voltage	V_{NVLL}	Voltage at NV at 2100ns after rising edge of XNV	−0.08	−0.02	0.04	V
	H level voltage	V_{NVHH}	Voltage at NV at 2100ns after at XNV falling edge	10.52	10.58	10.64	V

Parameter			Symbol	Condition	Min.	Typ.	Max.	Unit
Output waveforms of vertical clock drivers 1, 2, 3, 4	L level voltage	Vφ1	$V_{\phi 1L}$	Voltage at Vφ1 at 490ns after XV1 rising edge	0.06	0.32	0.80	V
		Vφ2	$V_{\phi 2L}$	Voltage at Vφ2 at 490ns after XV2 rising edge		0.35		
		Vφ3	$V_{\phi 3L}$	Voltage at Vφ3 at 490ns after XV3 rising edge		0.45		
		Vφ4	$V_{\phi 4L}$	Voltage at Vφ4 at 490ns after XV4 rising edge		0.47		
	H level voltage	Vφ1	$V_{\phi 1H}$	Voltage at Vφ1 at 1050ns after XV1 falling edge	9.91	9.98	10.06	V
		Vφ2	$V_{\phi 2H}$	Voltage at Vφ2 at 1050ns after XV2 falling edge				
		Vφ3	$V_{\phi 3H}$	Voltage at Vφ3 at 1050ns after XV3 falling edge				
		Vφ4	$V_{\phi 4H}$	Voltage at Vφ4 at 1050ns after XV4 falling edge				
	L coupling voltage	Vφ1	$V_{\phi 1LL}$	Voltage at Vφ1 at 280ns after XV2 rising edge	−0.58	−0.29	0.01	V
		Vφ2	$V_{\phi 2LL}$	Voltage at Vφ2 at 280ns after XV3 rising dege	−0.55	−0.34	−0.12	V
		Vφ3	$V_{\phi 3LL}$	Voltage at Vφ3 at 280ns after XV4 rising dege	−0.60	−0.37	−0.13	V
		Vφ4	$V_{\phi 4LL}$	Voltage at Vφ4 at 280ns after XV1 rising dege	−0.60	−0.42	−0.23	V
	H coupling voltage	Vφ1	$V_{\phi 1HH}$	Voltage at Vφ1 at 280ns after XV2 falling edge	10.16	10.46	10.62	V
		Vφ2	$V_{\phi 2HH}$	Voltage at Vφ2 at 280ns after XV3 falling edge		10.45		
		Vφ3	$V_{\phi 3HH}$	Voltage at Vφ3 at 280ns after XV4 falling edge		10.37		
		Vφ4	$V_{\phi 4HH}$	Voltage at Vφ4 at 280ns after XV1 falling edge		10.44		
	L coupling amplitude	Vφ1	$V_{\phi 1L\text{-}LL}$	$V_{\phi 1L} - V_{\phi 1LL}$	0.14	0.61	1.07	V
		Vφ2	$V_{\phi 2L\text{-}LL}$	$V_{\phi 2L} - V_{\phi 2LL}$	0.25	0.68	1.10	V
		Vφ3	$V_{\phi 3L\text{-}LL}$	$V_{\phi 3L} - V_{\phi 3LL}$	0.36	0.81	1.26	V
		Vφ4	$V_{\phi 4L\text{-}LL}$	$V_{\phi 4L} - V_{\phi 4LL}$	0.44	0.88	1.32	V
Output waveforms of sensor gate drivers 1, 2	Falling edge voltage	SG1	V_{SG1L}	Voltage at SG1 at 350ns after XSG1 rising edge	0.14	0.84	1.46	V
		SG2	V_{SG2L}	Voltage at SG2 at 350ns after XSG2 rising edge		0.88		
	Rising edge voltage	SG1	V_{SG1H}	Voltage at SG1 at 350ns after XSG1 falling edge	11.94	12.74	13.26	V
		SG2	V_{SG2H}	Voltage at SG2 at 350ns after XSG2 falling edge		12.59		
	L level voltage	SG1	V_{SG1LL}	Voltage at SG1 at 1330ns after XSG1 rising edge	−0.11	0.00	0.11	V
		SG2	V_{SG2LL}	Voltage at SG2 at 1330ns after XSG2 rising edge				
	H level voltage	SG1	V_{SG1HH}	Voltage at SG1 at 1330ns after XSG1 falling edge	13.25	13.36	13.47	V
		SG2	V_{SG2HH}	Voltage at SG2 at 1130ns after XSG2 falling edge				

Electrical Characteristics Test Circuit 1

DC characteristics testing

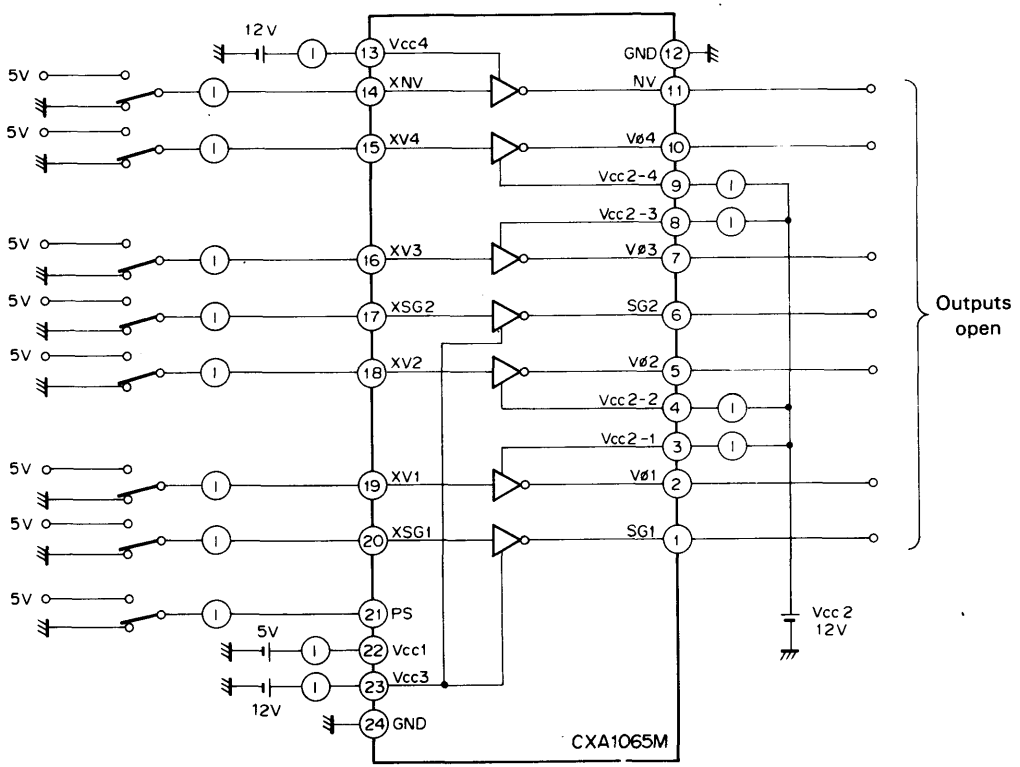


Fig. 1

Electrical Characteristics Test Circuit 2

Supply current testing when CXA1065M drives the equivalent circuit of CCD Imager, ICX022.

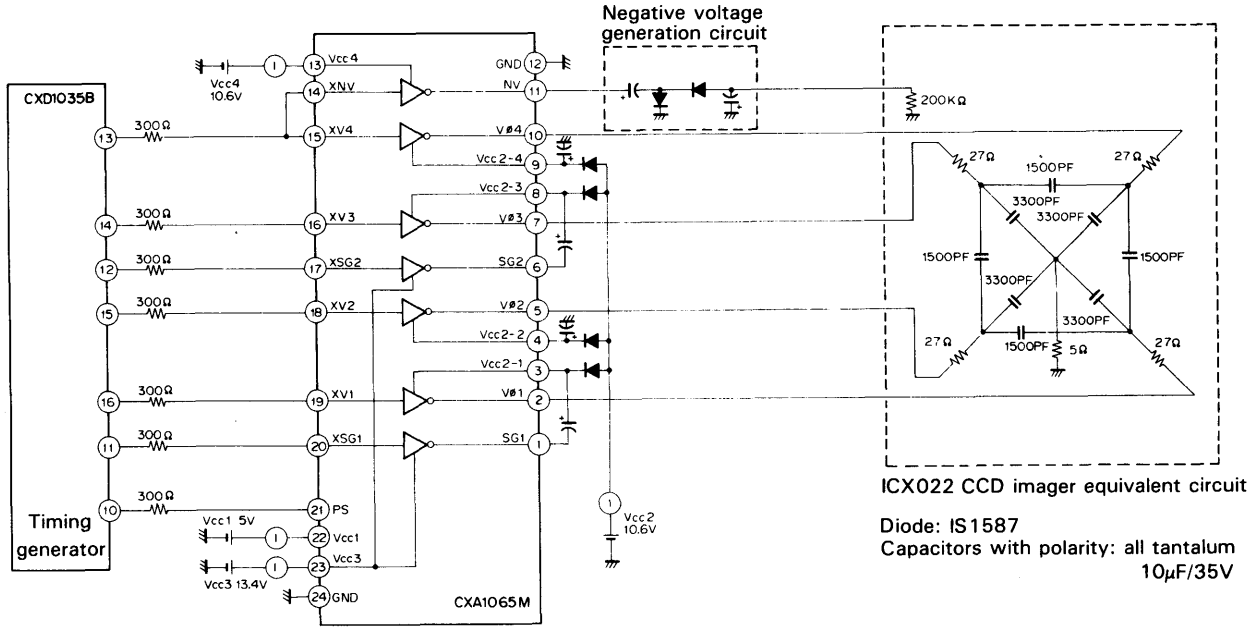


Fig. 2

Electrical Characteristics Test Circuit 3

Waveforms Testing

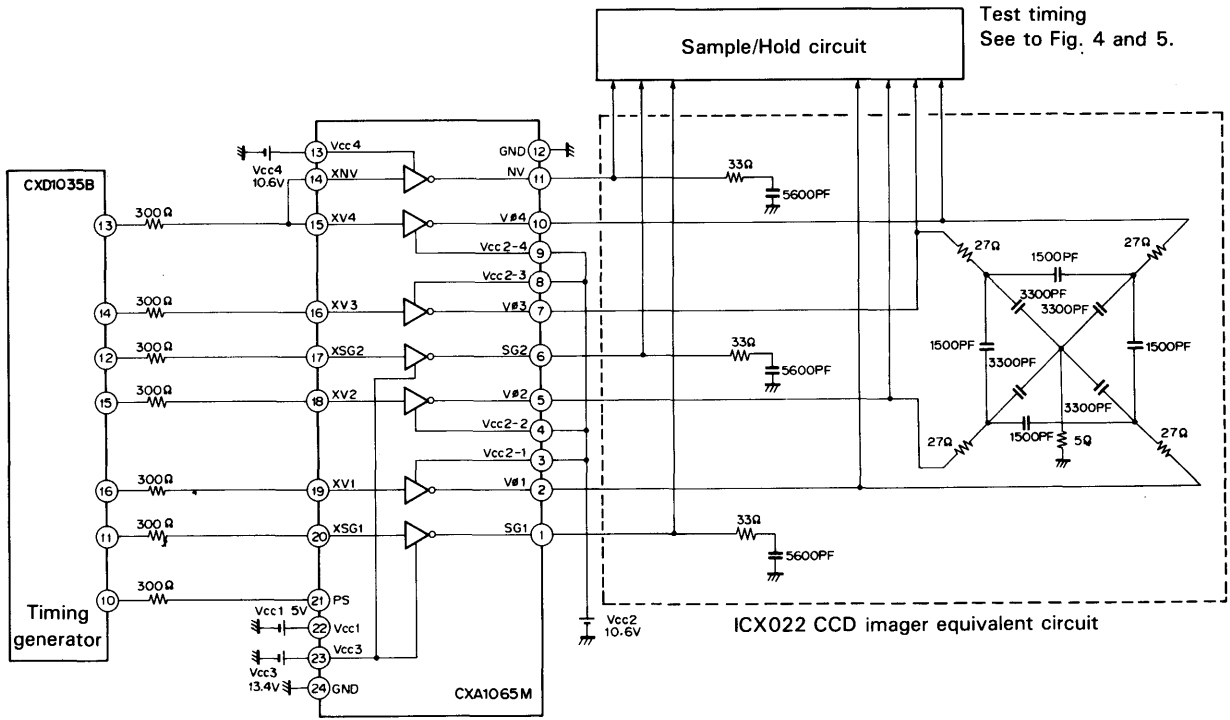


Fig. 3

Timing Chart

Waveform testing of 4-phase vertical clock drivers

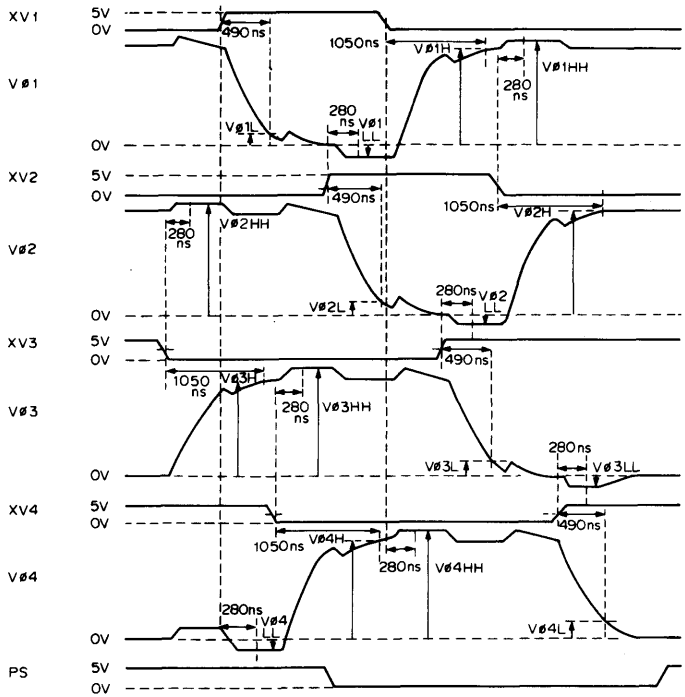


Fig. 4

Waveform testing of sensor gate drivers and negative voltage generation drivers

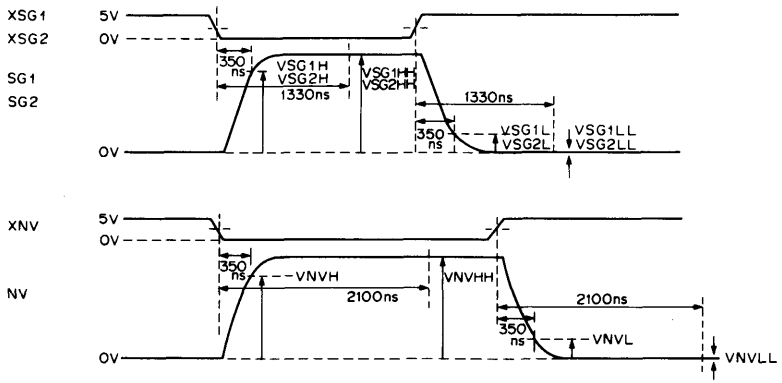


Fig. 5

Description of Operation

Description of functions and operation of the CXA1065M internal circuits

The CXA1065M is composed of a bias circuit and seven drivers.

Apply a voltage of 5 V to the Vcc1 terminal of the bias circuit. This circuit not only determines the DC bias for the seven drivers, but also has a power-saving function which reduces the power consumptions of four vertical clock drivers and two sensor gate drivers.

Directly connect the output of a CMOS IC to the input pins of the seven drivers. (Signal level, H: 5V, L: 0V) The output signal of each driver is inverted with low output impedance and wide amplitude. The output H level voltage of each driver is almost equal to the bias voltage of output stage and the L level output voltage is almost equal to the ground level. (See Fig. 6.)

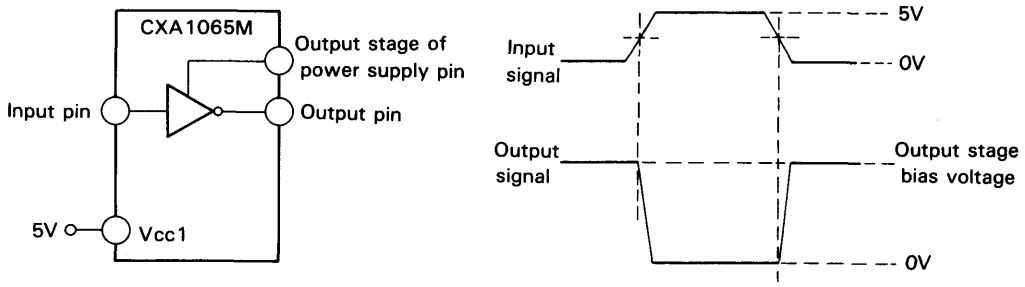


Fig. 6

The 4-phase clock drivers have a suppressing function of the coupling between phases when a CCD imager is driven. This function is suppress coupling voltage from other phases through the imager junction capacitances.

*Power-saving function

The CCD imaging device is equivalently, capacitive load.

Then a large driving ability is required only in the transient period of the output, and there is no need for such a large ability in other periods. The DC bias of the 4-phase clock drivers and 2 sensor gate drivers is changed by the input signal at the PS pin with appropriate timing, to reduce bias current when a large driving ability is not needed and achieve low power consumption.

Reference data: Typical values of supply current when the ICX022 equivalent circuit is driven (See Fig. 2)

	Using power-saving function	Not using power-saving function (PS pin fixed at 0V)
Supply current at Vcc1	1.9 mA	2.3 mA
Supply current at Vcc2	7.1 mA	12.7 mA
Supply current at Vcc3	0.8 mA	3.3 mA
Supply current at Vcc4	2.0 mA	2.0 mA

Description of Operation (CCD imager (ICX022) vertical clock driving system)

(For further information on the driving system of the CCD imager, refer to the specifications.)

Connect the output pin of the CXD1035B (CMOS IC) which is the CCD camera scanning timing generator, to the respective pins (Pin 14 through 21) of CXA1065M.

Clamp the output signal of the 4-phase vertical clock driver to the low level and input it to the vertical shift register transfer clock pin of the CCD imager.

Rectify the output signal of the negative voltage generation driver to obtain two reference voltage (negative voltages) for the low-level clamp. These two voltages are provided to compensate the clamping loss which may occur from the difference in duty between the 4-phase vertical clock drive signals. (When stable low-level clamp reference voltage supply is available with in the equipment, the rectifying circuit for the negative voltage is no more required.)

With the system shown in Fig. 8, the H level voltage of V clock level of the 4-phase vertical clock drive signals after the low-level clamp, is kept at 0 V even if Vcc4 is varied. This is because the circuit is designed to keep the low-level clamp reference voltage equal to the output voltage amplitude of the vertical clock drivers.

To obtain one of the readout clock pulse signals: The output signal of sensor gate driver 1 is used to modulate the output bias voltage of vertical clock driver 1.

To obtain the other signal: The output signal of sensor gate driver 2 used to modulate the output bias voltage of vertical clock driver 3.

If no source of high DC voltage is available in the equipment, the output signal for negative voltage generation driver can be utilized to generate the CCD imager substrate voltage. (See Fig. 7.)

Substrate voltage generation circuit

When maximum DC power supply in the equipment is +15V

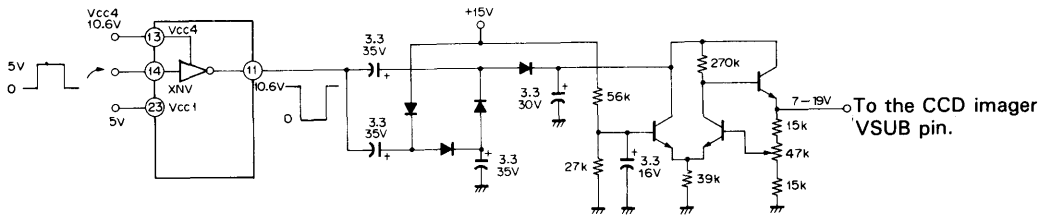
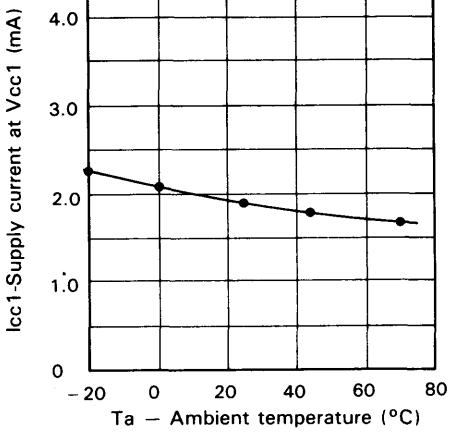


Fig. 7

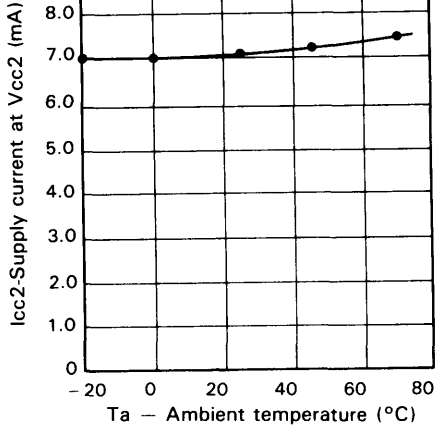
Performance Curves

Supply current when the ICX022 equivalent circuit is driven (Refer to the Test Circuit in Fig. 2).

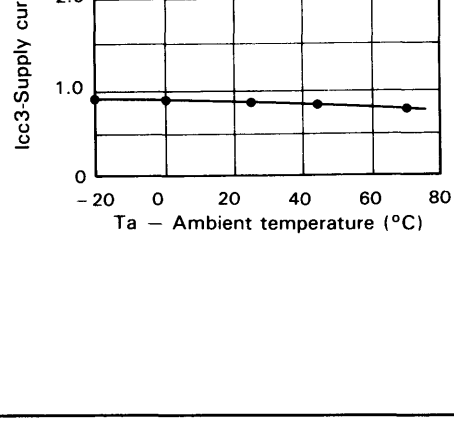
Supply current at Vcc1 vs. Ambient temperature



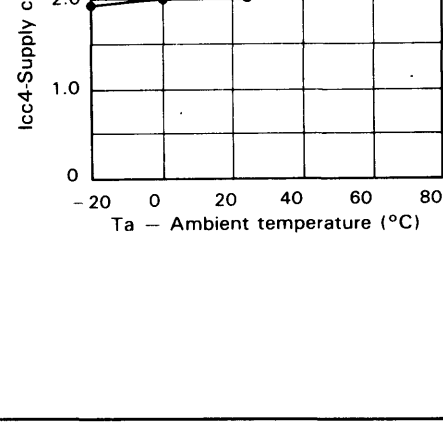
Supply current at Vcc2 vs. Ambient temperature



Supply current at Vcc3 vs. Ambient temperature



Supply current at Vcc4 vs. Ambient temperature



Notes on Application

- A large current flow through the power supply pin or the GND pin during the transient period of the output signal. Therefore, the GND pin must be grounded at a point within 1 cm from the pin. In addition, set the by-pass capacitor of the power supply pin within 1 cm from the pin.
- A conventional CMOS IC suffices as the input signal source of this IC (with an input current of Max. 500μA). To obtain the sharp CCD imager driving signal, minimize the length of the signal line.
- With an elongated signal line between the output pin of this IC and the input pin of the CCD imager, the inductance of the line may cause linking. To avoid this, shorten the line or insert a resistance in series to dump the linking.
- If the signal line between the output pin of this CMOS IC and input pin of this IC is too long, stray capacitance is large. In this case input signal of this IC is dull then sharp CCD imager driving signal is not obtained.

SONY

CXD1250M

Vertical Clock Driver of CCD Imager

Description

CXD1250M is a clock driver developed for the vertical register drive of ICX026/027.

Features

- 4-channel vertical clock driver and 1 channel substrate driver are built-in.

Structure

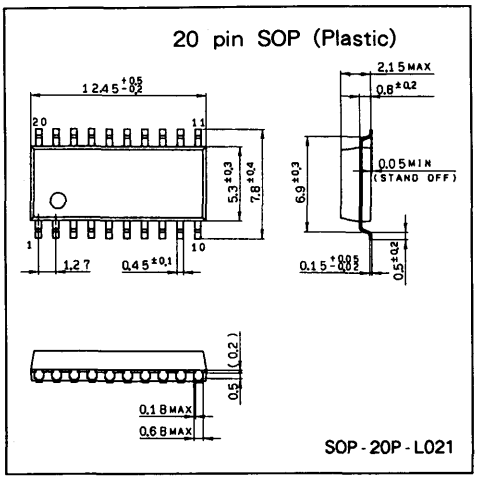
CMOS

Application

- CCD camera

Package Outline

Unit : mm



Absolute Maximum Ratings (Ta = 25°C)

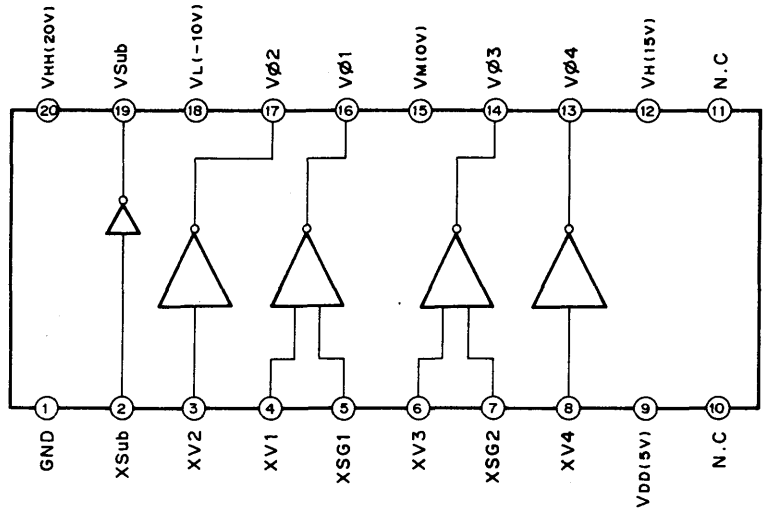
• Supply voltage	V_{DD}	$V_L - 0.3$ to $V_L + 35.0$	V
	V_M	$V_L - 0.3$ to $V_L + 35.0$	V
	V_H	$V_L - 0.3$ to $V_L + 35.0$	V
	V_{HH}	$V_L - 0.3$ to $V_L + 35.0$	V
• Input voltage	V_I	$V_L - 0.3$ to $V_{DD} + 0.3$	V
• Output voltage	MV φ (pins 11, 13)	$V_L - 0.3$ to $V_M + 0.3$	V
• Output voltage	HV φ (pins 14, 16)	$V_L - 0.3$ to $V_H + 0.3$	V
• Output voltage	HHV φ (pin 19)	$V_L - 0.3$ to $V_{HH} + 0.3$	V
• Operating temperature	Topr	− 25 to + 85	°C
• Storage temperature	Tstg	− 40 to + 125	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	$V_L + 15.0$	V
	V_M	$V_L + 10.0$	V
	V_H	$V_L + 25.0$	V
	V_{HH}	$V_L + 30.0$	V
• Operating temperature	Topr	− 20 to + 75	°C

80639 − ST

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	GND	—	GND
2	XSub	I	Output control (VSub)
3	XV2	I	Output control ($V_{\phi 2}$)
4	XV1	I	Output control ($V_{\phi 1}$)
5	XSG1	I	Output control ($V_{\phi 1}$)
6	XV3	I	Output control ($V_{\phi 3}$)
7	XSG2	I	Output control ($V_{\phi 2}$)
8	XV4	I	Output control ($V_{\phi 4}$)
9	V_{DD}	—	Power supply (5V)
10	NC	—	
11	NC	—	
12	V_H	—	Power supply (15V)
13	$V_{\phi 4}$	O	Output (2 level : V_M, V_L)
14	$V_{\phi 3}$	O	Output (3 level : V_H, V_M, V_L)
15	V_M	—	Power supply (0V)
16	$V_{\phi 1}$	O	Output (3 level : V_H, V_M, V_L)
17	$V_{\phi 2}$	O	Output (2 level : V_M, V_L)
18	V_L	—	Power supply (− 10V)
19	VSub	O	Output (2 level : V_{HH}, V_L)
20	V_{HH}	—	Power supply (20V)

Truth Table

Input				Output		
XV1 • 3	XSG1 • 2	XV2 • 4	XSub	V φ 1 • 3	V φ 2 • 4	VSub
L	H	X	X	V_M	X	X
H	H	X	X	V_L	X	X
X	X	L	X	X	V_M	X
X	X	H	X	X	V_L	X
X	X	X	L	X	X	V_{HH}
X	X	X	H	X	X	V_L
L	L	H	X	V_H	V_L	X
H	L	X	X	Z	X	X

X : Don't Care
Z : High Impedance

DC Characteristics (Ta = 25°C)

Item	Symbol	Test condition	Power supply	Min.	Typ.	Max.	Unit
"H" level input voltage	V_{IH}		$V_{DD} = 5$ $V_L = -10$ $V_M = 0$ $V_H = 15$ $V_{HH} = 20$	3.5	—	—	V
"L" level input voltage	V_{IL}			—	—	1.5	V
"L" level output voltage	$V_{\phi L}$	$I_{\phi L} = 20\ \mu A$		—	−10	−9.9	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M} = -20\ \mu A$		—	0.0	0.1	V
"M" level output voltage	$V_{\phi M}$	$I_{\phi M} = 20\ \mu A$		−0.1	0.0	—	V
"H" level output voltage	$V_{\phi H}$	$I_{\phi H} = -20\ \mu A$		14.9	15	—	V
"HH" level output voltage	$V_{\phi HH}$	$I_{\phi HH} = -20\ \mu A$		19.9	20	—	V
Input current	Ii			—	1.0	—	μA
Power supply current*	I_M			—	4.5	5.0	mA
Power supply current*	I_{DD}			—	0.3	0.5	mA
Power supply current*	I_H			—	0.1	0.2	mA
Power supply current*	I_{HH}			—	0.05	0.1	mA

*Supply current at operation (See the Test Circuit)

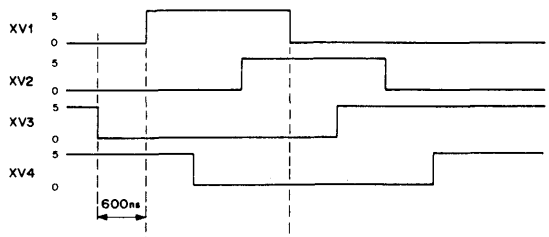
Switching Characteristics

(See the Test Circuit Ta = 25℃, V_{HH} = 20V, V_H = 15V, V_M = 0V, V_L = − 10V, V_{DD} = 5V)

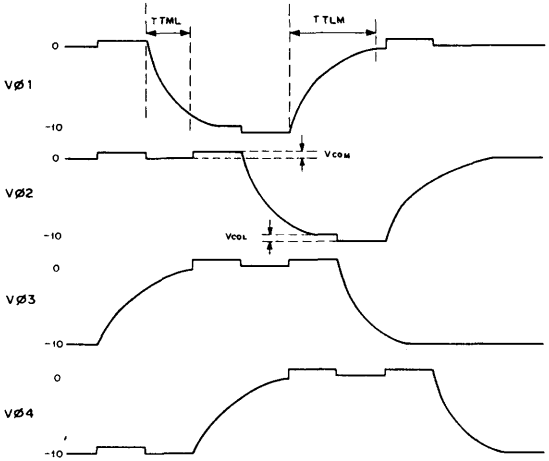
Item	Symbol	Conditions	Max.	Min.	Unit
Output current	I_L	V φ 1 to 4 = − 9.5V	− 25		mA
Output current	I_{M1}	V φ 1 to 4 = − 0.5V		10	mA
Output current	I_{M2}	V φ 1, 3 = 0.5V	− 9		mA
Output current	I_H	V φ 1, 3 = 14.5V		12	mA
Output current	I_{SL}	VSub = − 9.5V	− 12		mA
Output current	I_{SH}	VSub = − 19.5V		7	mA
Rise time $V_L \rightarrow V_M$	T_{TLM}	V φ 1 to 4 = − 0.5V After input transient	1000		ns
Fall time $V_M \rightarrow V_L$	T_{TML}	V φ 1, 3 = − 9.5V After input transient	500		ns
Rise time $V_M \rightarrow V_H$	T_{TMH}	V φ 1, 3 = 14V After input transient	1000		ns
Fall time $V_H \rightarrow V_M$	T_{THM}	V φ 1, 3 = 1V After input transient	1000		ns
Rise time $V_L \rightarrow V_{HH}$	T_{TLHH}	VSub = 17V After input transient	200		ns
Fall time $V_{HH} \rightarrow V_L$	T_{THHL}	VSub = − 7V After input transient	200		ns
Coupling amplitude (middle level)	V_{COM}	V φ 1 to 4	0.5		V
Coupling amplitude (low level)	V_{COL}	V φ 1 to 4	0.5		V

Input Waveform

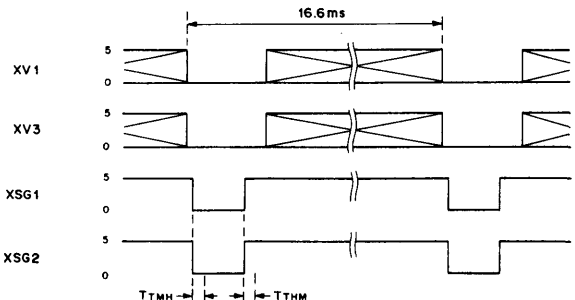
(Repeat Cycle 15.7kHz)



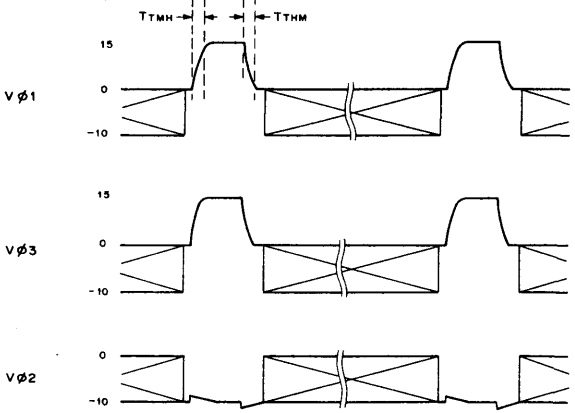
Output Waveform

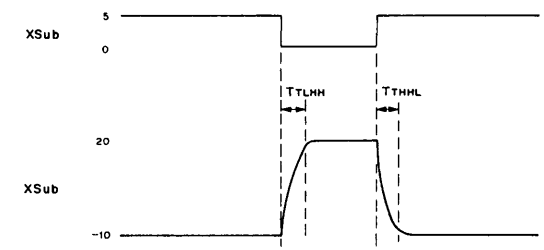


Input waveform

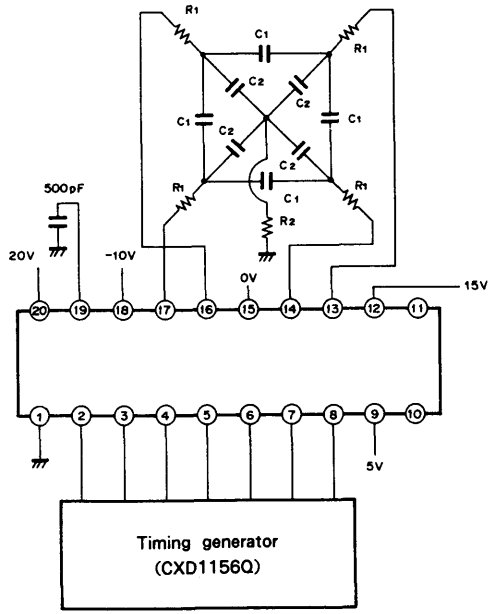


Output waveform





Test Circuit



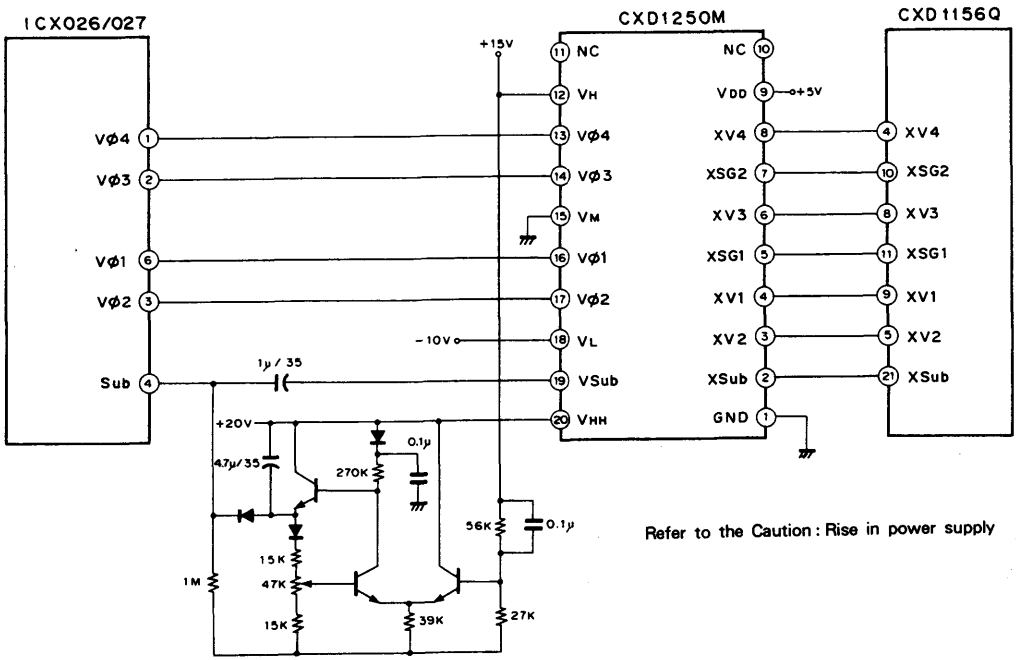
R1 ; 27Ω

R2 ; 5Ω

C1 ; 1500pF

C2 ; 3300pF

Application Circuit

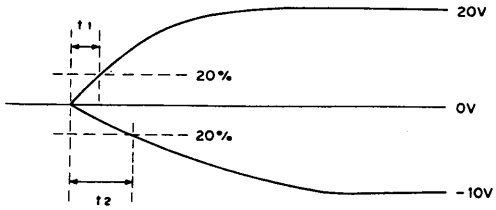


Refer to the Caution : Rise in power supply

Caution : Rise in Power Supply

When the substrate driver is in use, be careful not to let the CCD imager (ICX026/027) Sub (pin 4) turn into negative voltage.

To this end, raise the −10V and +20V supplies at the application circuit under the following conditions.



$t_2 > t_1 \geqq 10ms$

Signal Processing IC for Video Camera

5) Signal Processing IC for Video Camera

Type	Application	Function	Page
CXA1310AQ	Monochrome camera	Single Chip Processing for CCD Monochrome camera	451
CX20053	Sample hold	CDS, color separation, color mix correction, γ correction, blanking, white clip, pedestal setting	465
CX20055	Encoder	Aperture correction, blank cleaning, white clip, chroma mod, fader, finder, switcher, 75Ω driver	484
CX20056	Auto iris, auto white balance	Iris drive, RB line seq. signal separation, auto white balance, low light alarm	503
CX20151	Matrix	Color differential, signal forming, luminance signal forming, multiplexer	521
CX23039	1H delay line×4	1H delay line × 4, S/H, delay line driver	546
CXA1337Q-Z/R	Sample hold	CDS,AGC, Color separation, chroma suppress	559
CXA1338Q-Z/R	Signal processing	From color compensation (Mg, G, Cy, Ye) interleave coding, R, G, B sythetic and Y signal processing	577
CXA1339Q-Z/R	Matrix	Matrix, white balance, γ correction, negative/positive inversion	598
CXA1072Q-Z/R	Encoder	Aperture, auto-corrier balance, negative-positive reverse, fader, chroma suppression, BLK cleaning	616
CXL1503M CXL1505M	For matrix 1H delay line Signal Processing	1H CMOS-CCD delay line × 4	640
CXL1504M	Luminous signal 1H delay line	1H CMOS-CCD delay line	648
CXA1270N	Vertical outline compensation	Signal generation during, Vertical Outline Compensation	656
CX20095A CX20186	Video output	6dB amp, video driver, bilateral video driver	664

SONY®

CXA1310AQ

Single Chip Processing for CCD Monochrome Camera

Description

The CXA1310AQ is designed to perform the basic signal processing in CCD monochrome cameras through a single chip. This bipolar IC is most suitable for compact usage and low power consumption.

32 pin QFP (Plastic)

Features

- Processing from CCD output to 75 Ω video output with a single chip
- Wide variable AGC (4 to 32dB Typ.)
- Built-in operational amplifier for AGC loop
- 75 Ω line capacitance minimized using sag compensation function
- Variable white clip level realize wide dynamic range (140IRE)

Structure

Bipolar silicon monolithic IC

Applications

CCD monochrome camera

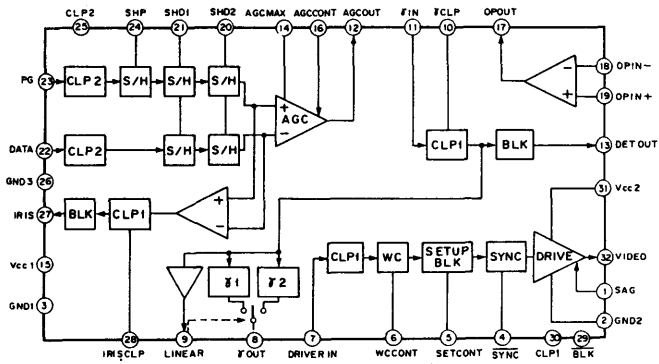
Absolute Maximum Ratings (Ta = 25°C)

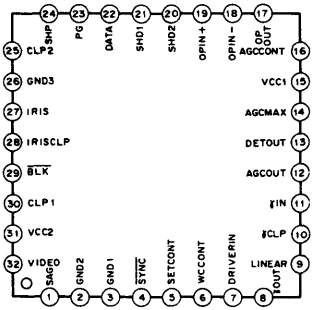
• Supply voltage	Vcc	7	V
• Storage voltage	Tstg	−65 to +150	°C
• Operating temperature	Topr	−20 to +75	°C
• Allowable power dissipation	P_D	500	mW

Operating Conditions

Supply voltage	Vcc	4.75 to 5.25	V

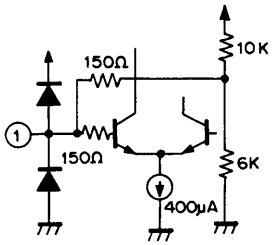
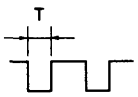
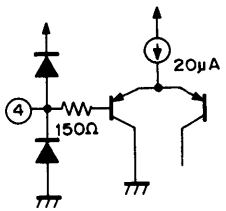
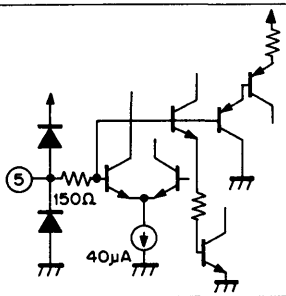
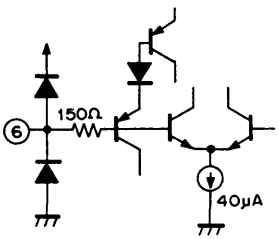
Block Diagram and Pin Configuration



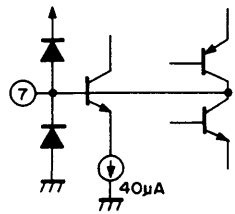
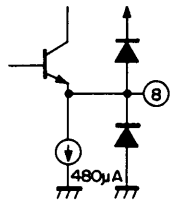
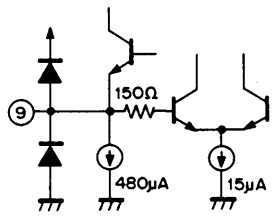
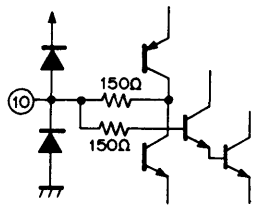


E89910 – ST

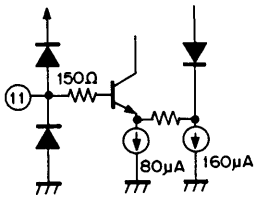
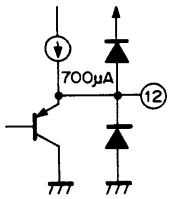
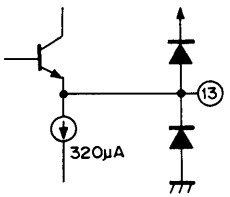
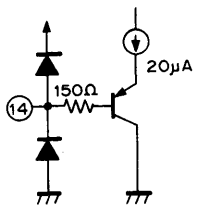
Pin Description

No.	Symbol	I/O signal	Equivalent circuit	Description
1	SAG	Inputs VIDEO OUT through capacitor		Input pin of sag compensation signal
2	GND2	*GND		GND for driver and IRIS
3	GND1	*GND		GND for other than driver and sample hold and IRIS
4	$\overline{\text{SYNC}}$	 * HI : 4.5V and above LO : 0.5V and below T : 5 μs		Sync pulse input pin (active at LO)
5	SET CONT	*GND *2 to 3.5V *Vcc		Set up level adjusting pin Turns to preset mode 1 Control mode Turns to preset mode 2
6	WC CONT	*GND *2 to 3.5V		White clip level adjusting pin Preset mode Control mode

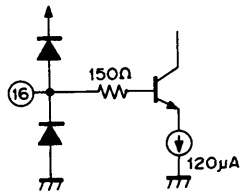
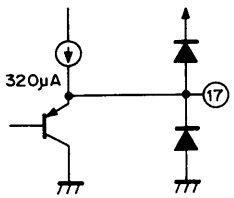
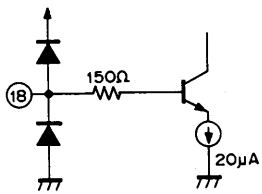
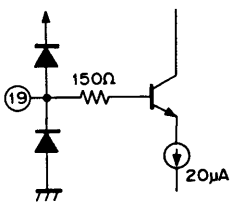
*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
7	DRIVER IN	Inputs γ OUT through capacitor or LINEAR		Input pin to driver
8	γ OUT	 DC 2V		Gamma compensation signal output pin. Outputs γ 1 when Pin 9 at OPEN outputs γ 2 when Pin 9 turned to 5V
9	LINEAR	 DC 1.8V * Vcc		Linear signal (γ-OFF signal) output pin Pin 8 output signal turns to γ 2 output
10	γ CLP			Capacitor connecting pin for gamma input clamp

*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
11	γ IN	 Input DC permissible range *DC2 to 3V		Input pin of the gamma compensation circuit
12	AGC OUT	 Vpp MAX 1300mV Vpp TYP 500mV DC 2.55V		Output pin of signal passed through AGC
13	DET OUT	 MAX 1500mV TYP 500mV DC 2V		Output pin of AGC detection signal
14	AGC MAX	*DC		Maximum gain setting pin of AGC amplifier
15	V_{CC1}	*5V		Power supply for other than driver and IRIS

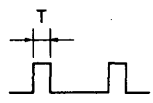
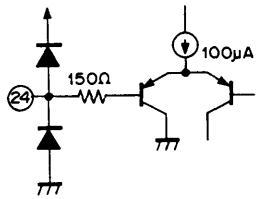
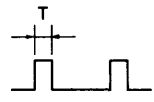
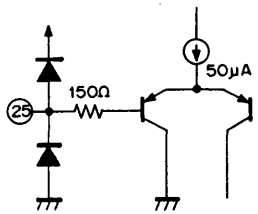
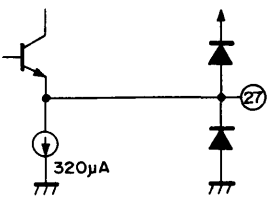
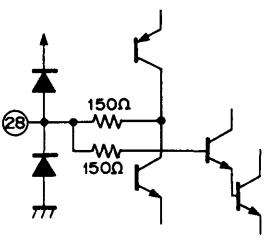
*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
16	AGC CONT	*DC		Gain control pin of AGC amplifier
17	OP OUT			Output pin of the operational amplifier
18	OP IN −			Inverted input pin of the operational amplifier
19	OP IN +			Non inverted input pin of the operational amplifier (AGC detection signal input pin)

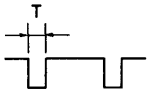
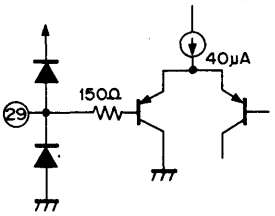
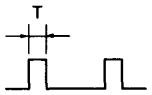
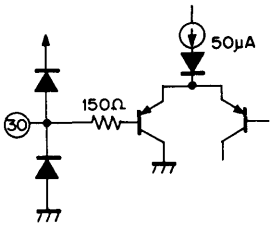
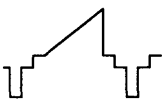
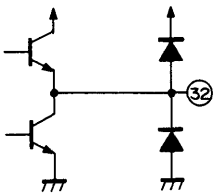
*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
20	SHD2	T * HI : 4.5V and above LO : 0.5V and below T : 15ns and above	150Ω, 100μA, 20	Input pin of the sample hold pulse (active at HI)
21	SHD1	T * HI : 4.5V and above LO : 0.5V and below T : 15ns and above	150Ω, 100μA, 21	Input pin of the sample hold pulse (active at HI)
22	DATA	① ② ①MAX 800mV ②MAX 800mV	150μA, 22	CCD signal input pin
23	PG	① ② ①MAX 800mV ②MAX 800mV	150μA, 23	CCD signal input pin

*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
24	SHP	 * HI : 4.5V and above LO : 0.5V and below T : 15ns		Input pin of the sample hold pulse (active at HI)
25	CLP2	 * HI : 4.5V and above LO : 0.5V and below T : 2 µs		CLP2 pulse input pin (active at HI)
26	GND3	*GND		Sample hold GND
27	IRIS	 DC 1.3V		Output pin of the IRIS control signal
28	IRIS CLP			Capacitor connecting pin for IRIS output clamp

*External applied voltage

No.	Symbol	I/O signal	Equivalent circuit	Description
29	$\overline{BLK}$	 * HI : 4.5V and above LO : 0.5V and below T : 11 µs		BLK pulse input pin (active at LO)
30	CLP1	 * HI : 4.5V and above LO : 0.5V and below T : 2 µs		CLP1 pulse input pin (active at HI)
31	Vcc2	*5V		Driver and IRIS power supply
32	VIDEO	 BLK level 1.5V		VIDEO signal output pin

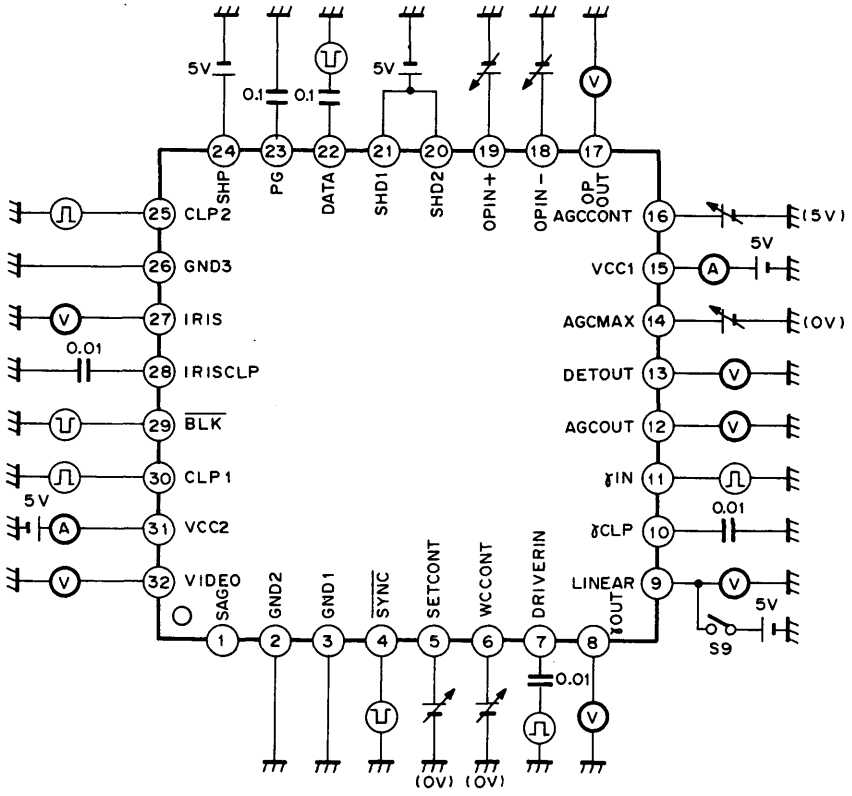
*External applied voltage

Electrical Characteristics (Ta = 25℃, Vcc = 5V, See Electrical Characteristics Test Circuit)

No.	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Current consumption	Icc	Current value of Vcc1 and Vcc2 AGC CONT = 1.5V	30	45	60	mA
2	Min. value of AGC MAX	MAX	GAIN between DATA input and AGC OUT DATA input = 100mV AGC MAX = 4V, AGC CONT = 1.5V	—	18	20	dB
3	Min. value of AGC CONT	AG1	GAIN between DATA input and AGC OUT DATA input = 500mV, AGC CONT = 5V	—	4	6	dB
4	Max. value of AGC CONT	AG2	GAIN between DATA input and AGC OUT DATA input = 30mV, AGC CONT = 1.5V	30	32	—	dB
5	AGC CONT 10dB	AG3	GAIN between DATA input and AGC OUT DATA input = 320mV, AGC CONT = 3.55V	8	10	12	dB
6	AGC OUT DC	ADC	DC output level of AGC OUT	2.25	2.55	2.85	V
7	γ 1 output level	γ 1	Test value of γ 1 output level γ IN input = 500mV	530	630	730	mV
8	γ 2 output level	γ 2	Test value of γ 2 output level γ IN input = 500mV, S9 ON	580	680	780	mV
9	LINEAR AMP GAIN	LG	GAIN between γ IN input and LINEAR γ IN input = 500mV	1.6	2.6	3.6	dB
10	DET OUT DC	DDC	DC output level of DET OUT	1.8	2.0	2.2	V
11	IRIS AMP GAIN	IG	GAIN between DATA input and IRIS DATA input = 300mV	8	10	12	dB
12	IRIS OUT DC	IDC	DC output level of IRIS	1.1	1.3	1.5	V
13	DRIVER GAIN	DG	GAIN between DRIVER IN and VIDEO DRIVER IN = 700mV	5.7	6.0	6.3	dB
14	SYNC level	SY	SYNC level/DG* of VIDEO output	270	293	316	mV
15	SET UP 1	SE1	SET UP level of preset mode 1 SET UP level/DG* of VIDEO output	-15	0	15	mV
16	SET UP 2	SE2	SET UP level of preset mode 2 SET UP level/DG* of VIDEO output	0	20	40	mV
17	Min. value of SET CONT	SE3	SET UP level/DG* of VIDEO output SET CONT = 2V	—	-3	15	mV
18	Max. value of SET CONT	SE4	SET UP level/DG* of VIDEO output SET CONT = 3.3V	80	130	—	mV
19	W-CLIP level	WC1	W-CLIP level/DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = GND	780	820	860	mV
20	Min. value of WC CONT	WC2	W-CLIP level/DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = 2.2V	—	300	600	mV
21	Max. value of WC CONT	WC3	W-CLIP level/DG* of VIDEO output DRIVER IN = 1500mV, WC CONT = 3.3V	1000	1300	—	mV
22	OP AMP output D range Low level	OPL	DC output level of OP OUT OP IN + = 2.5V, OP IN − = 4V	—	0.8	1.2	V
23	OP AMP output D range High level	OPH	DC output level of OP OUT OP IN + = 4V, OP IN − = 2.5V	4.5	4.8	—	V

*Characteristics value at DRIVER GAIN item

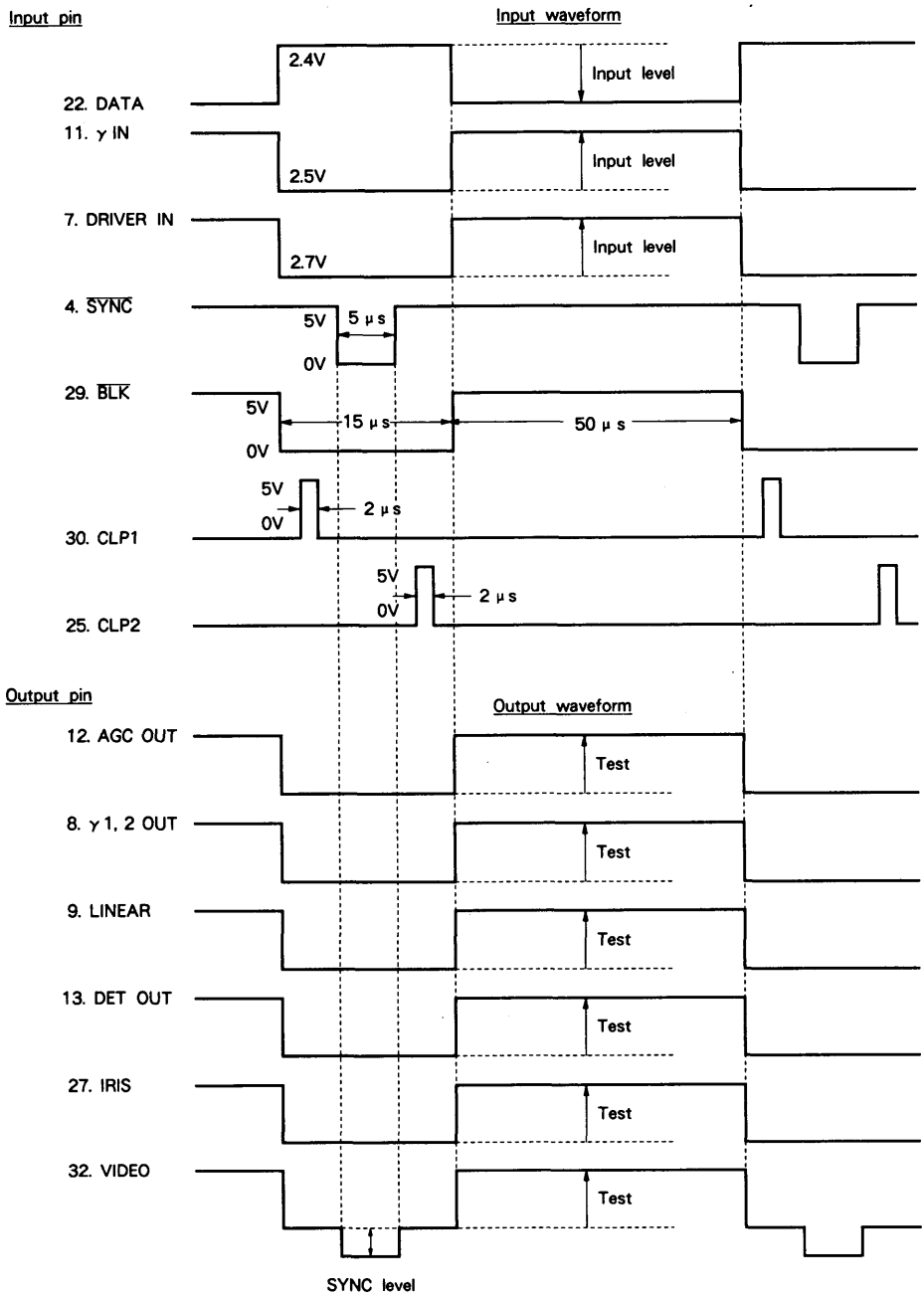
Electrical Characteristics Test Circuit



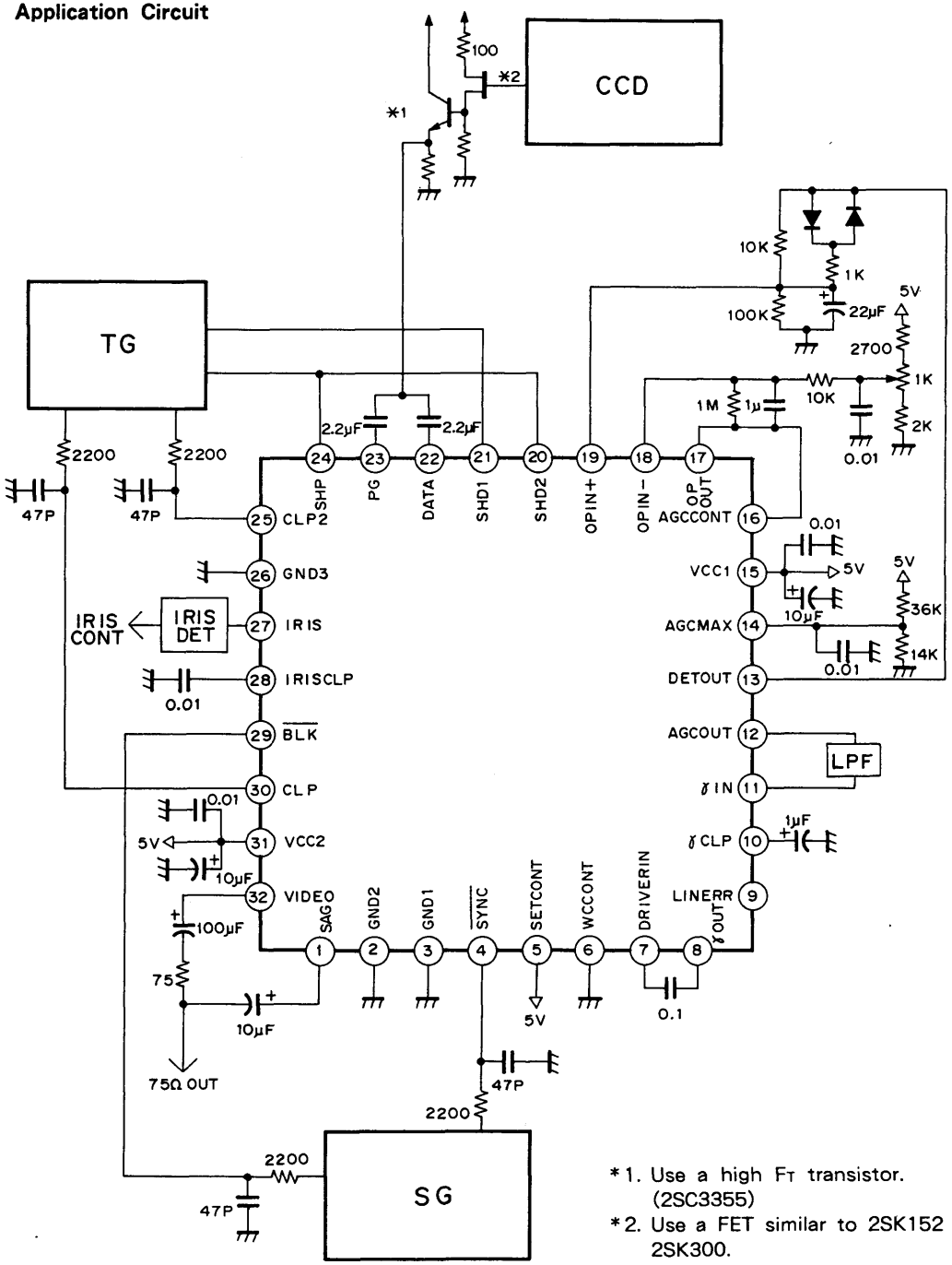
Note)

- μF is the capacitance unit of the capacitor.
- For Pins 5, 6, 14 and 16, apply voltage in brackets unless otherwise specified in the conditions column of the Electrical Characteristics.
- Ⓥ indicates a test pin. (Test AC, DC voltage)
- For Pins 7, 11 and 22, the input signal level is at 0mV, unless otherwise specified in the conditions column of the Electrical Characteristics.

Test Circuit I/O Waveform Diagram



Application Circuit

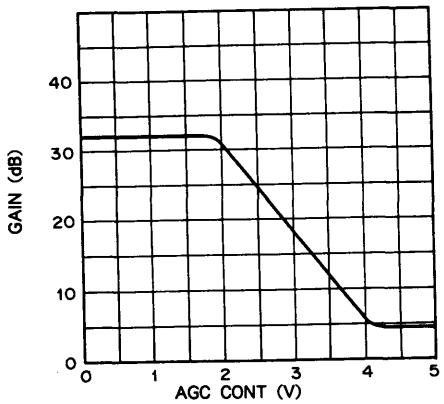


*1. Use a high FT transistor. (2SC3355)

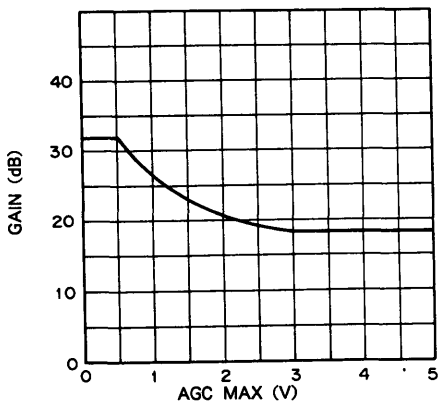
*2. Use a FET similar to 2SK152 or 2SK300.

Representative Characteristics (Vcc = 5V, Ta = 25°C)

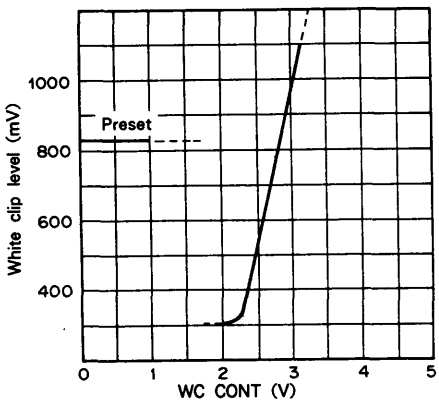
AGC control characteristics



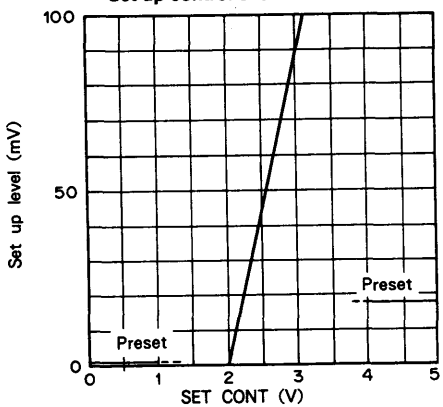
AGC MAX control characteristics



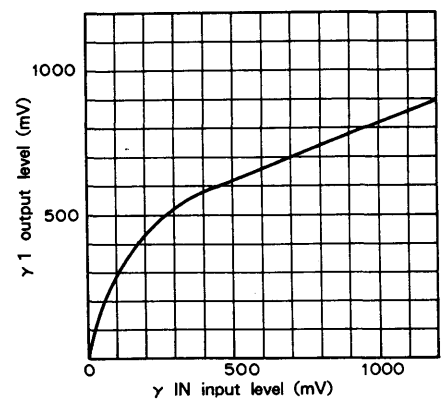
White clip control characteristics



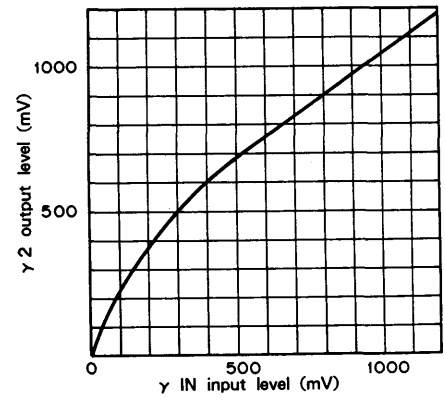
Set up control characteristics



γ 1 I/O characteristics

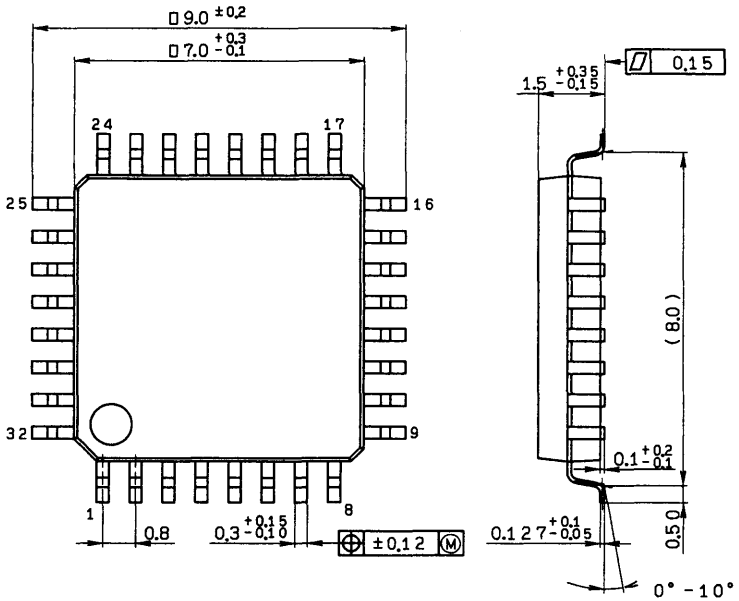


γ 2 I/O characteristics



Package Outline Unit : mm

32 pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———

SONY

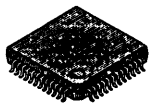
CX20053

Signal Processing for Color Camera

Description

CX20053 is a bipolar IC which has been developed as a processor of color-difference line alternating color camera and it is comprised of correlated double sampling, AGC, color separation S/H, color mixing correction, white balance, clamping, γ correction, blanking, white clipping, pedestal setting, etc. circuits. It processes various kinds of signals and forms G signal which has been γ corrected, and R and B lines alternating signals.

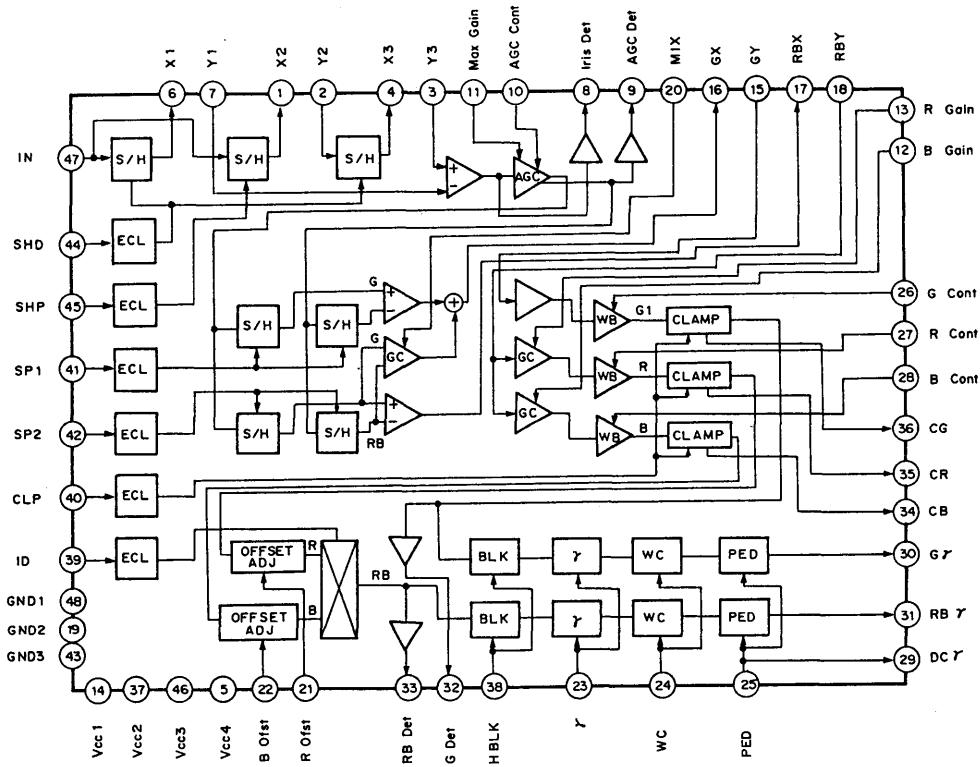
48 pin QFP (Plastic)



Features

- It can compose a consistent color camera signal processing system, together with the CX20054, CX20055 and CX20056.
- By adopting correlated double sample and hold, reduction of noises in low frequency bands and leakage of S/H pulses can be achieved.

Block Diagram



E89661 – ST

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

• Power supply voltage	Vcc to 4	10	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	833	mW

Operation Power Supply Voltage Range

Vcc1, Vcc2	8.5 ± 0.2	V
Vcc3, Vcc4	5.0 ± 0.15	V

Input Pin Maximum Voltage

Pin No.	Voltage(V)	Pin No.	Voltage(V)	Pin No.	Voltage(V)
2	≦Vcc1,2	20	≦Vcc1,2	38	≦Vcc1,2
3	≦Vcc1,2	21	≦Vcc1,2	39	≦Vcc3,4
7	≦Vcc1,2	22	≦Vcc1,2	40	≦Vcc3,4
10	≦Vcc1,2	23	≦Vcc3,4	41	≦Vcc3,4
11	≦Vcc3,4	24	≦Vcc3,4	42	≦Vcc3,4
12	≦Vcc3,4	25	≦Vcc3,4	44	≦Vcc3,4
13	≦Vcc3,4	26	≦Vcc3,4	45	≦Vcc3,4
15	≦Vcc1,2	27	≦Vcc3,4	47	≦Vcc1,2
18	≦Vcc1,2	28	≦Vcc3,4		

Output Pin Maximum Applied Voltage

Pin No.	Voltage(V)	Pin No.	Voltage(V)	Pin No.	Voltage(V)
1	≦Vcc1,2	16	≦Vcc1,2	32	≦Vcc1,2
4	≦Vcc1,2	17	≦Vcc1,2	33	≦Vcc1,2
6	≦Vcc1,2	29	≦Vcc3,4	34	≦Vcc1,2
8	≦Vcc1,2	30	≦Vcc3,4	35	≦Vcc1,2
9	≦Vcc1,2	31	≦Vcc3,4	36	≦Vcc1,2

Pulse Input Level

Pin No.	Input level
38	CMOS level
39	CMOS level
40	CMOS level
41	CMOS level
42	CMOS level
44	CMOS level
45	CMOS level

CMOS Level

	Min.	Max.	Unit
V_H	4.0	5.0	V
V_L	0	0.4	V

Allowable value of clamping pulse width
1.96 μsec ± 10%
Provided that it is APL 10 to 90% by using stair step.

Pin Description

No.	Symbol	I/O	Description
1	X2	O	Output of input signal which is sampled and hold with SHP pulse (together with externally attached capacitor).
2	Y2	I	Input in order to further sample and hold with SHD pulse (together with externally attached capacitor) to be phase matched the output of X2 to that of X1.
3	Y3	I	Another input of input signal which is sampled and hold to be fed to differential operation stage.
4	X3	O	Output of Y2
5	Vcc4		Power supply (5V) for control pins
6	X1	O	Output which is an input signal that is SHD sampled and hold (together with externally attached capacitor).
7	Y1	I	Another input of input signal which has been sampled and hold together with Y3 to be differential operation stage.
8	Iris Det	O	Output to be fed to CX20056, and it is an input signal which has been sampled and hold and whose gain is raised approximately 3 times.
9	AGC Det	O	Output of AGC which changes its gain in response to input signal and the output to be fed to CX20056.
10	AGC Cont	I	An input of control voltage from CX20056 which corresponds to the input signal, and it controls AGC gain.
11	Max Gain	I	An input which controls maximum gain of control.
12	B Gain	I	Among the input signals, it controls gain of B signal.
13	R Gain	I	Among the input signals, it controls gain of R signal.
14	Vcc1		Power supply voltage (8.5V) which is supplied to the first half of signals flow; namely, input signal, color separation sample and hold signal, etc.
15	GY	I	Signal input from the GX through coupling capacitor.
16	GX	O	G component output among input signals which is obtained by color separation sample and hold with SP1 pulse from input signal passing through AGC circuit.
17	RBX	O	RB component output among input signals obtained by color separation sample and hold with SP2 pulse from input signal passing through AGC circuit.
18	RBY	I	A signal input of RBX passing through coupling capacitor.
19	GND2		Grounding of Vcc2 and Vcc4.
20	MIX	I	Color mixing channel control pin of imagepicked up element. Color mixing to G of RB is controlled by it.
21	Rofst	I	Offset control pin of clamped R signal, and it performs matching into G channels (γ).
22	Bofst	I	Offset control pin of clamped B signal, and it performs matching into G channel (γ).
23	γ	I	It controls γ correction from clamped G and RB signals.
24	WC	I	It controls WC level from γ curves of Gγ and RBγ.
25	PED	I	It controls pedestals of γ corrected signals.
26	G Cont	I	It controls gain of G signal which has been color separated and clamped.

No.	Symbol	I/O	Description
27	R Cont	I	Control voltage (R channel) input for WB from WB(White Balance) IC.
28	B Cont	I	Control voltage (B channel) input for WB from WB IC.
29	DCγ	O	DC level output of pedestal.
30	Gγ	O	G component of γ corrected signal output.
31	RBγ	O	RB component of γ corrected signal output.
32	G Det	O	G component output for CX20056 in order to maintain WB.
33	RB Det	O	RB component for CX20056 in order to maintain WB.
34	CB	O	Output which holds black level of B signal whose gain becomes variable after it has been color separated and passed through WB amplifier.
35	CR	O	Output which holds black level of R signal whose gain becomes variable after it has been color separated and passed through WB amplifier.
36	CG	O	Output which holds black level of G signal whose gain becomes variable after it has been color separated and passed through WB amplifier.
37	Vcc2		Power supply voltage (8.5V) which allows the latter half of signal flow against Vcc1.
38	HBLK	I	Blanking pulse input.
39	ID	I	ID pulse input which switches over R signal and B signal.
40	CLP	I	Clamping pulse input.
41	SP1	I	Sample and holding pulse input in order to carry out color separation of G component.
42	SP2	I	Sample and holding pulse input in order to carry out color separation of RB component.
43	GND3		Grounding of Vcc3.
44	SHD	I	Another input of sample and hold pulse in order to sample and hold the input signal.
45	SHP	I	Another input of sample and hold pulse in order to sample and hold the input signal.
46	Vcc3		Power supply voltage (5.0V) of pulse system (ECL).
47	IN	I	Input of imager
48	GND1		Grounding of Vcc1.

Electrical Characteristics

(Ta=25°C, V_{CC1}=V_{CC2}=8.5V V_{CC3}=V_{CC4}=5V)

Item	Symbo	Measuring point	SW condition										Bias condition												Condition	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13					
Circuit current 1	I_{D1}	A1	a	a	a	a	a	a	a	a	a	a	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	Current of V_{CC1}	9.9	13.3	17.1	mA
Circuit current 2	I_{D2}	A2	a	a	a	a	a	a	a	a	a	a	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	Current of V_{CC2}	12.6	17.8	23.7	mA
Circuit current 3	I_{D3}	A3	a	a	a	a	a	a	a	a	a	a	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	Current of V_{CC3}	6.9	9.6	12.7	mA
Circuit current 4	I_{D4}	A4	a	a	a	a	a	a	a	a	a	a	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	Current of V_{CC4}	4.1	5.5	7.2	mA
C.D.S. frequency characteristics 1 to 3	X_{1F}~ X_{3F}	V1~V3	b	a	a	a	a	a	a	a	a	a	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S1(500 mVp-p)*1, P5=P51*2, Deterioration amount at 4 MHz against 500 kHz	−2.5	−1.7		dB
C.D.S. dynamic range 1 to 3	X_{1D}~ X_{3D}	V1~V3	b	a	a	a	a	a	a	a	a	a	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S2(1.5 Vp-p)*3, P5=P52 *4,	0.63	0.89	1.18	Vp-p
Iris amplifier gain	IR_{G1}	V4	a	a	a	a	a	a	a	a	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S3(150 mVp-p)*5	315	420	539	mVp-p
Iris amplifier dynamic range	IR_{D}	V4	a	a	a	a	a	a	a	a	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S3(2 Vp-p)	2.43	2.93	3.47	Vp-p
Iris DC level	IR_{DC}	V4	a	a	a	a	a	a	a	a	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p	3.51	4.10	4.73	V
AGC DC level	AGC_{DC}	V5	a	a	a	a	a	a	a	a	b	b	ST*6	ST*6	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V		3.60	4.18	4.79	V
AGC DC offset	AGC_{V1} AGC_{V2}	V5	a	a	a	a	a	a	a	a	b	b	2V 4V	2.34 V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p, Difference between AGC V_1 and AGC V_2	−220	0	275	mV
Max gain control range	MG_{C1} MG_{C2}	V5	a	a	a	a	a	a	a	a	b	b	4V	3V 2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S3(25 mVp-p), Ratio between MG C_1 and MG C_2	15.5	18.3	21.0	dB
AGC control range	AGC_{C1} AGC_{C2}	V5	a	a	a	a	a	a	a	a	b	b	3V 2V	3V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S3(25 mVp-p), Ratio between AGC C_1 and AGC C_2	23.0	26.5	30.0	dB
AGC dynamic range	AGC_{D}	V5	a	a	a	a	a	a	a	a	b	b	ST	ST	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S3(2 Vp-p)	1.44	1.80	2.20	Vp-p
Color separation SH balance characteristics 1	GX_{BL}	V6	a	a	a	a	a	a	a	a	a	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p, P4=P41*7	−2.2	0	5.5	mVp-p
Color separation SH balance characteristics 2	PBX_{BL}	V7	a	a	a	a	a	a	a	a	a	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V		−2.2	0	5.5	mVp-p
Color separation SH frequency characteristics 1	GX_{F}	V6	a	a	a	a	a	a	a	a	a	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S1(100 mVp-p), P4=P42*8 Deterioration amount at 2 MHz atainst 500 kHz	−4.5	−3.0		dB
Color separation SH frequency characteristics 2	RBX_{R}	V7	a	a	a	a	a	a	a	a	a	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S1(100 mVp-p), P4=P42 Deterioration amount at 2 MHz against 500 kHz	−4.5	−3.0		dB
Color separation SH dynamic range 1	GX_{D}	V6	a	a	a	a	a	a	a	a	a	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S2(15 Vp-p), P4=P52	0.63	0.90	1.21	Vp-p
Color separation SH dynamic range 2	RBX_{D}	V7	a	a	a	a	a	a	a	a	a	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S2(15 Vp-p), P4=P52	0.63	0.90	1.21	Vp-p
Differential amplifier frequency characteristics 1	GX_{F2}	V6	a	a	a	a	a	a	a	a	c	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S1(100 mVp-p), Deterioration amount at 10 MHz against 500 kHz	−3.5	−2.0		dB
Differential amplifier frequency characteristics 2	RBX_{F2}	V7	a	a	a	a	a	a	a	a	c	b	ST	ST	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S1(100 mVp-p), Deterioration amount at 10 MHz against 500 kHz	−3.5	−2.0		dB

(Ta=25°C, $V_{CC1}=V_{CC2}=8.5V$ $V_{CC3}=V_{CC4}=5V$)

Item	Symbol	Measuring point	SW condition 1	2	3	4	5	6	7	8	9	10	Bias condition E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	Condition	Min.	Typ.	Max.	Unit
Mixer characteristics	MIX_1 MIX_2	V6	a	a	a	a	a	a	a	a	c	b	ST	ST	2.5V	2.5V	3V 2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S3(100 mVp-p), Difference between MIX 1 and MIX 2	11.7	19.5	28.6	mVp-p
GWB control range	CG_{C1} CG_{C2}	V15	a	b	a	a	b	a	a	b	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	3V 2V	2.5V	2.5V	S=S3(300 mVp-p), Ratio between CG C_1 and CG C_2	11.0	13.0	15.0	dB
GWB dynamic range	CG_D	V15	a	b	a	a	b	a	a	b	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	ST*9	2.5V	2.5V	S=S3(3 Vp-p)	3.06	3.65	4.29	Vp-p
GWB DC offset	CG_{V1} CG_{V2}	V15	a	b	a	a	b	a	a	b	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	3V 2V	2.5V	2.5V	S=0 mVp-p, Difference between CG V_1 and CG V_2	−132	0	132	mV
GWB frequency characteristics	CG_F	V15	a	b	a	a	b	a	a	b	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	ST	2.5V	2.5V	S=S1(300 mVp-p), Deterioration amount at 10 MHz against 500 kHz	−4.5	−3.0		dB
R gain control range	CG_{C1} CR_{C2}	V14	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2.5V	3V 2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2V	2.5V	S=S3(100 mVp-p), Ratio between CR C_1 and CR C_2	18.0	22.0	26.0	dB
B gain control range	CB_{C1} CB_{V2}	V13	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	3V 2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2V	S=S3(100 mVp-p), Ratio between CB C_1 and CB C_2	18.0	22.0	26.0	dB
RWB control range	CR_{C3} CR_{C4}	V14	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2.5V	2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	3V 2V	2.5V	S=S3(300 mVp-p), Ratio between CR C_3 and CR C_4	11.0	13.3	15.5	dB
BWB control range	CB_{C3} CB_{C4}	V13	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	3V 2V	S=S3(300 mVp-p), Ratio between CB C_3 and CB C_4	11.0	13.3	15.5	dB
RWB dynamic range	CR_D	V14	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2.5V	2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	3V	2.5V	S=S3(3 Vp-p)	2.97	3.70	4.51	Vp-p
BWB dynamic range	CB_D	V13	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	3V	S=S3(3 Vp-p)	2.97	3.70	4.51	Vp-p
RWB offset	CR_{V1} CR_{V2}	V14	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2.5V	2V 3V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2V	3V	S=0 mVp-p, Difference between CR V_1 and CR V_2	−450	0	450	mV
BWB offset	CB_{V1} CB_{V2}	V13	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2V 3V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	3V 2V	S=0 mVp-p, Difference between CB V_1 and CB V_2	−451	0	451	mV
RWB frequency characteristics	CR_F	V14	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	ST*10	2.5V	S=S1(300 mVp-p), Deterioration amount at 10 MHz against 500 MHz	−4.0	−2		dB
BWB frequency characteristics	CB_F	V13	a	b	b	b	a	a	a	b	b	b	2.5V	2.5V	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	ST*11	S=S1(300 mVp-p), Deterioration amount at 10 MHz against 500 MHz	−4.0	−2		dB
Offset gain (R)	OG_{R1} OG_{R2}	V12	a	b	a	a	a	a	c	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	3V 2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p, Difference between OG R_1 and OG R_2	333	430	539	mV
Offset gain (B)	OG_{B1} OG_{B2}	V12	a	b	a	a	a	a	b	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	2.5V	3V 2V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p, Difference between OG B_1 and OG B_2	333	430	539	mV
G Det DC level	GD_{DC}	V11	a	b	a	a	a	a	a	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST*12	ST*12	ST*12	ST*12	ST*12	ST	ST	ST	S=0 mVp-p	4.12	4.33	4.95	V
PB Det DC level (R)	RD_{DC}	V12	a	b	a	a	a	a	c	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=0 mVp-p	4.12	4.33	4.95	V
PB Det DC level (B)	BD_{DC}	V12	a	b	a	a	a	a	b	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=0 mVp-p	4.12	4.33	4.95	V
γ matching G-R	γ_G γ_R	V9 V10	a	b	a	a	a	a	c	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=S3(300 mVp-p), Difference between γG and γR	−15.4	0	15.4	mVp-p
γ matching G-B	γ_G γ_B	V9 V10	a	b	a	a	a	a	b	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=S3(300 mVp-p), Difference between γG and γB	−15.4	0	15.4	mVp-p

(Ta=25°C, Vcc1=Vcc2=8.5V Vcc3=Vcc4=5V)

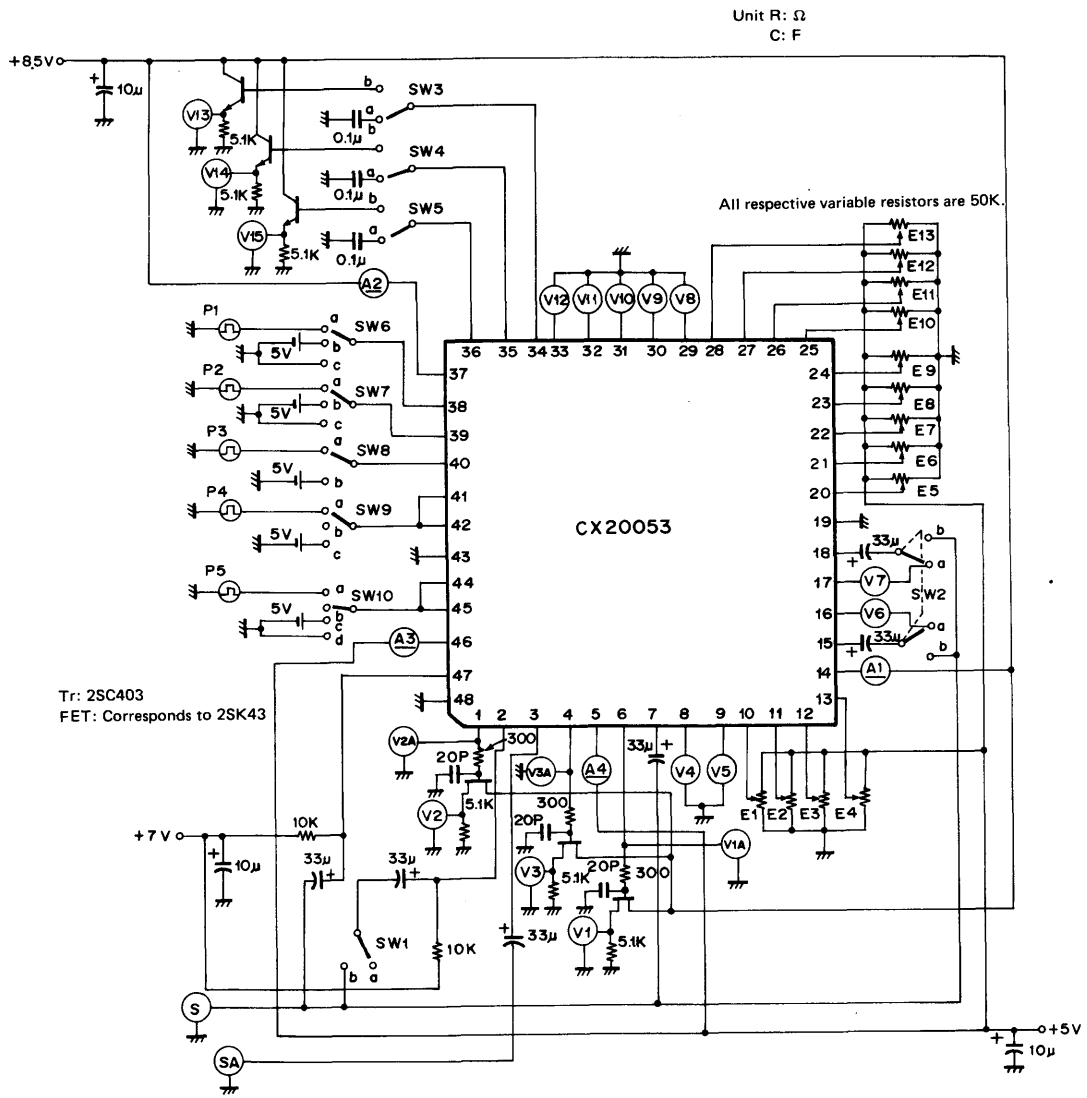
Item	Symbol	Measuring point	SW condition										Bias condition												Condition	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13					
Pedestal Gγ	$G\gamma_{DC}$	V9	a	b	a	a	a	c	a	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=0 mVp-p	1.62	2.35	3.19	V
Pedestal RBγ (R)	$R\gamma_{DC}$	V10	a	b	a	a	a	c	c	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=0 mVp-p	1.62	2.35	3.19	V
Pedestal RBγ (B)	$B\gamma_{DC}$	V10	a	b	a	a	a	c	b	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=0 mVp-p	1.62	2.35	3.19	V
DC pedestal	DCγ	V8	a	b	a	a	a	c	a	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	ST	ST	ST	ST	ST	ST	S=0 mVp-p	1.62	2.35	3.19	V
γ characteristics Gγ1	Gγ.1	V9	a	b	a	a	a	b	a	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	2V	3V	1.5V	ST	ST	ST	S=S3(300 mVp-p)	189	280	385	mVp-p
γ characteristics Gγ2	Gγ 2	V9	a	b	a	a	a	b	a	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	3V	3V	1.5V	ST	ST	ST	S=S3(300 mVp-p)	720	1100	1540	mVp-p
γ characteristics RBγ (R1)	Rγ 1	V10	a	b	a	a	a	b	c	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	2V	3V	1.5V	ST	ST	ST	S=S3(300 mVp-p)	189	280	385	mVp-p
γ characteristics RBγ (R2)	Rγ.2	V10	a	b	a	a	a	b	c	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	3V	3V	1.5V	ST	ST	ST	S=S3(300 mVp-p)	720	1100	1540	mVp-p
γ characteristics RBγ (B1)	Bγ.1	V10	a	b	a	a	a	b	b	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	2V	3V	1.5V	ST	ST	ST	S=S3(300 mVp-p)	189	280	385	mVp-p
γ characteristics RBγ (B2)	Bγ.2	V10	a	b	a	a	a	b	b	a	b	b	2.5V	2.5V	2.5V	2.5V	OV	ST	ST	3V	3V	1.5V	ST	ST	ST	S=S3(300 mVp-p)	720	1100	1540	mVp-p
CDS X1 to X3 H	$X1_H$ ~$X3_H$	$V1_A$ ~$V3_A$	b	a	a	a	a	a	a	a	a	c	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p	4.23	4.85	5.5	V
CDS X1 to X3 L	$X1_L$ ~3_L	$V1_A$ ~$V3_A$	b	a	a	a	a	a	a	a	a	d	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p	2.4	2.95	4.5	V
Iris amplifier gain	IR_{G1}	V4	a	a	a	a	a	a	a	a	b	b	2.64 V	2.53 V	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	SA=S3(150 mVp-p) (Other tests are all SA=0 mVp-p)	315	420	539	mVp-p
Color separation SH GX	GX_{V1} GX_{V2}	V6	a	a	a	a	a	a	a	a	b/a	b	2.64 V	2.53 V	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p, P4=P43*13 Difference between GX V_1 and GX V_2	−6	0	6	mV
Color separation SH GX	GX_{V3}	V6	a	a	a	a	a	a	a	a	a	b	2.64 V	2.53 V	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S2(500 mVp-p), P4=P43	5.6	6.35	7.2	V
Color separation SH RBX	RBX_{V1} RBX_{V2}	V7	a	a	a	a	a	a	a	a	b/a	b	2.64 V	2.53 V	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=0 mVp-p, P4=P43, Difference between RBX V_1 and RBX V_2	−6	0	6	mV
Color separation SH RBX	RBX_{V3}	V7	a	a	a	a	a	a	a	a	a	b	2.64 V	2.53 V	2.5V	2.5V	OV	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	S=S2(500 mVp-p), P4=P43	5.7	6.45	7.3	V
G Det AC level	GD_{AC}	V11	a	b	a	a	a	a	a	a	b	b	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.5V	2.66 V	2.5V	2.5V	S=S3(300 mVp-p)	180	235	297	mVp-p

* 1. S1 is sweep siganl of up to 10 MHz.
2. P51 is 10 MHz (pulse width 35 nsec) C-MOS level
3. S2 is 500 kHz, rectangular wave (see input and output waveform diagram)
4. P52 is 1 MHz (pulse width 35 nsec) C-MOS level (see input and output waveform diagram)
5. S3 is stairstep wave signal (see input and output waveform diagram)
6. E1=E2=ST means that when E1=4V with S=S3 (50 mVp-p), adjust E2 (max gain) so that V5 becomes 300 mVp-p and, in addition, adjust E1 so that V5 becomes 300 mVp-p at S=S3 (150 mVp-p). Thus the adjusted voltage values of E1 and E2 are respectively given as ST.
7. P41 is 250 kHz (pulse width 35 nsec) C-MOS level
8. P42 is 5 MHz (pulse width 35 nsec) C-MOS level
9. E11 =ST is the voltage value of E11 when the E11 is so adjusted that V11 becomes 250 mV.
10. E12=ST is the voltage value of E12 when the E12 is so adjusted that V12 becomes 250 mV.
11. E13=ST is the voltage value of E13 when the E13 is so adjusted that V12 becomes 250 mV.
12. E8=E9=E10=ST is, with S=S3 (300 mVp-p),
    i) Ajust E8 so that V9 becomes 500 mVp-p at E9=3V and E10=1.5V.
    ii) Adjust E9 so that V9 becomes 450 mVp-p.
    iii) Adjust E10 so that V9 becomes 500 mVp-p.
    The respective values of E8, E9 and E10 adjusted in the above mentioned manner becomes ST.

E6=E7=ST is the respective voltage values of E6 and E7 when they are so adjusted with S=S3 (300 mVp-p) and E8=E9=E10=ST so that V9 and V10 become equivalent.

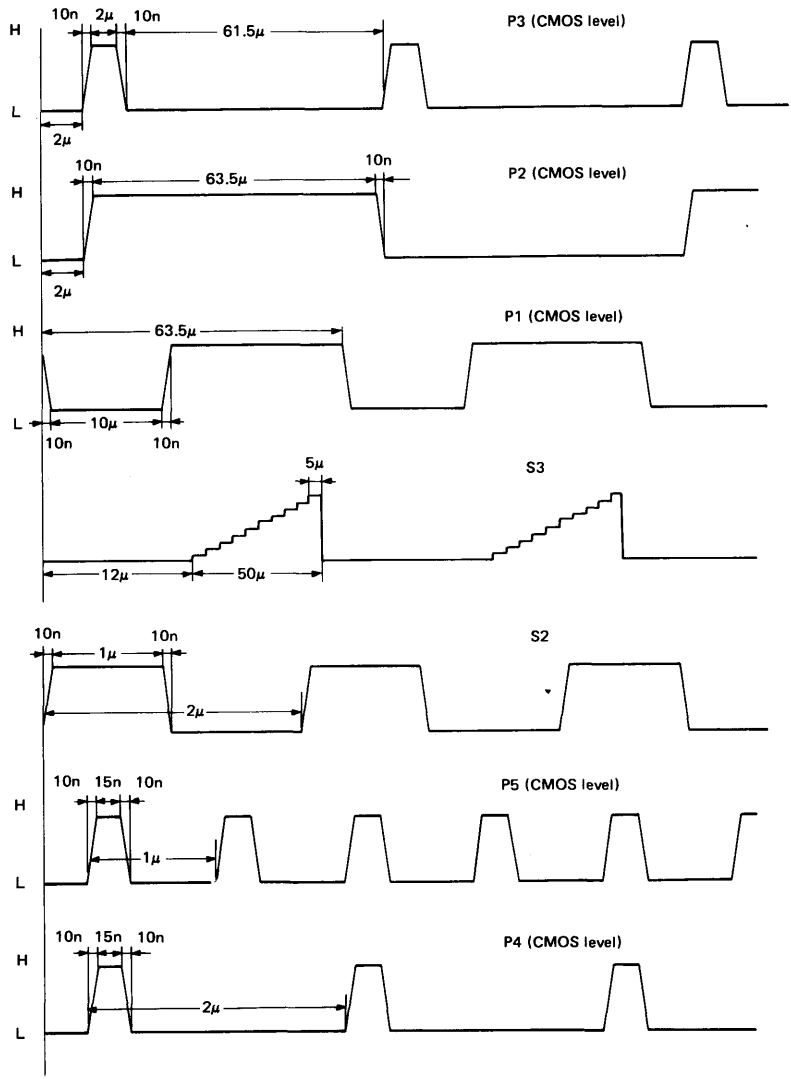
13. P43 is 500 kHz (pulse width 35 nsec) C-MOS level (See input and output waveform diagram)

Electrical Characteristics Test Circuit



Input and Output Waveform Diagram

Unit: sec.



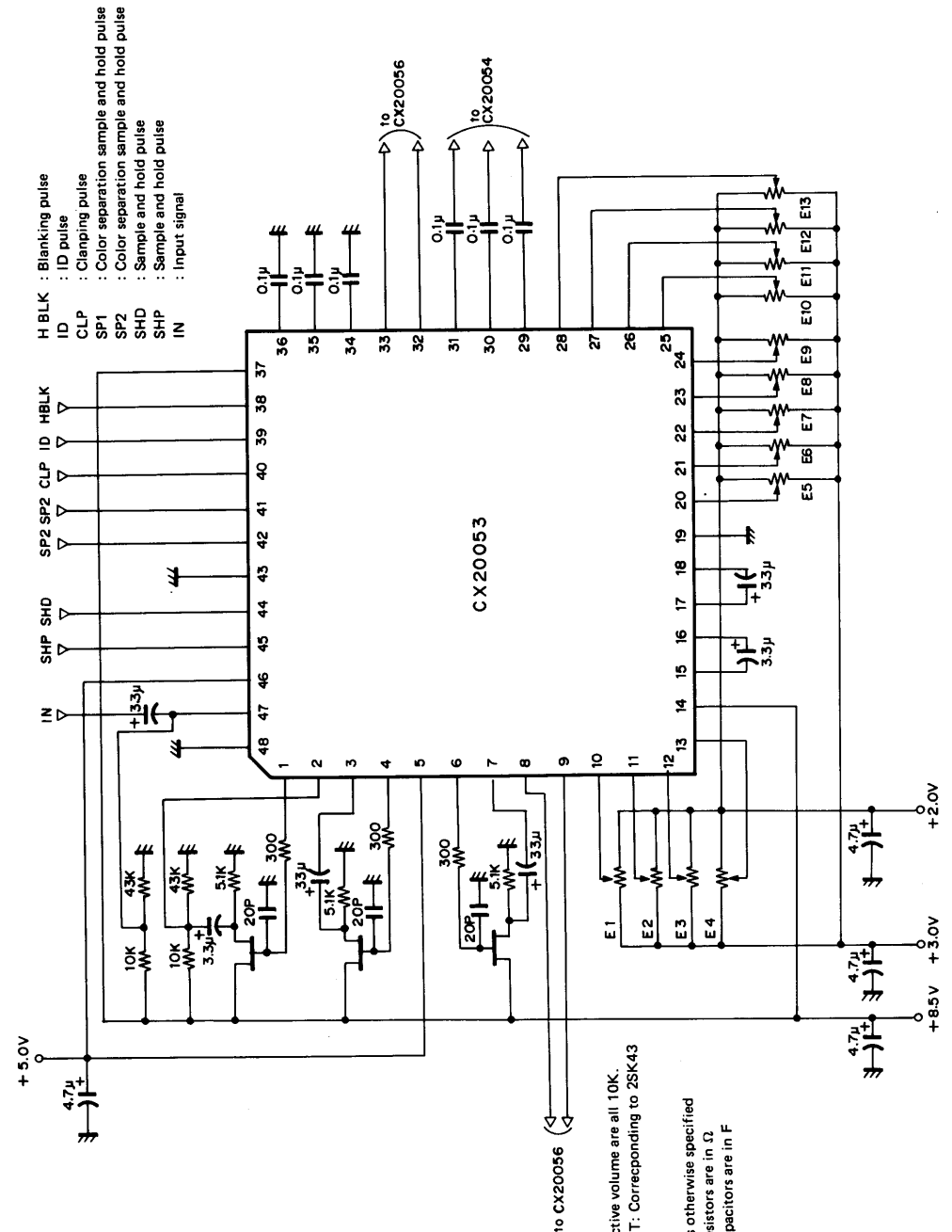
Standard Pin Voltage (DC) (When standard bias is applied)

Unit: V See the measuring circuit diagram During non-signal

Pin No.	Pin voltage	Pin No.	Pin voltage	Pin No.	Pin voltage
1	5.20	17	6.97	33	4.38
2	*1(7.1)	18	6.07	34	5.46
3	3.69	19	*1(0,GND)	35	5.46
4	5.19	20	*1(2.50)	36	5.48
5	*1(5.0, Vcc4)	21	*1(2.53)	37	*1(8.5, Vcc2)
6	5.20	22	*1(2.53)	38	*2(5.0, HBLK)
7	3.69	23	*1(2.39)	39	*2(5.0, ID)
8	4.19	24	*1(2.43)	40	*2(5.0, CLP)
9	4.20	25	*1(2.06)	41	*2(5.0, SP1)
10	*1(2.68)	26	*1(2.65)	42	*2(5.0, SP2)
11	*1(2.54)	27	*1(2.44)	43	*1(0, GND)
12	*1(2.50)	28	*1(2.46)	44	*2(5.0, SHD)
13	*1(2.50)	29	2.32	45	*2(5.0, SHP)
14	*1(8.5, Vcc1)	30	2.37	46	*1(5.0, Vcc3)
15	6.07	31	2.37	47	*1(7.1)
16	6.87	32	4.37	48	*1(0, GND)

*1. Numerals in the parentheses show externally applied values.
*2. It is a pulse input pin; however, the numerals represent the value externally applied as pulse ON.

Application Circuit



Standard Operating Characteristics (Ta=25°C) and Temperature Characteristics

Test conditions

SW condition										Bias condition												
1	2	3	4	5	6	7	8	9	10	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13
b	b	a	a	a	a	a	a	a	a													

[1] AGC amplifier output characteristics (Fig. 1)
When E1=4V with S=S3=50 mVp-p, adjust E2 so that V5 becomes 300 mVp-p. An output voltage of pin ⑨ when E11 is varied from 0 to 4V under the above-mentioned condition.

[2] G control characteristics (Fig. 2)
An output voltage of pin ㉜ set to S=S3=300 mVp-p, when E11 is varied from 0 to 4V.

[3] B or R control characteristics (Fig. 3)
An output voltage of pin ㉝ set to S=S3=300 mVp-p, when E12 and E13 are varied from 0 to 4V. Provided that E3 and E4 are fixed to 1V.

[4] B or R gain characteristics (Fig. 4)
An output voltage of pin ㉝ set to S=S3=300 mVp-p, when E3 and E4 are varied to 0 to 4V. Provided that E12=E13 is fixed to 1V.

[5] γ and knee characteristics (Fig. 5)
After the outputs of pins ㉝ and ㉜ become 250 mV set at S=S3, adjust by changing γ adjustment terminal voltage of pin ㉓ so that R/Bγ and Gγ outputs become 500 mV (without including pedestal amount). Then set the outputs of pins ㉝ and ㉜ so that they become 750 mV, and adjust WC pin voltage of pin ㉔ so that R/Bγ and Gγ outputs become 570 mV. Then, measure the γ and knee curves.

[6] Output variation of AGC amplifier due to the power supply voltage fluctuation (Fig. 6)
Output variation of AGC amplifier due to supply voltage fluctuation when set to S=S3=150 mV, and when the E1 is adjusted so that the output of pin ⑰ becomes 300 mV.
(Max gain = ST)

[7] Power supply voltage fluctuation characteristics of γ output (Fig. 7)
Power supply voltage dependability of the output voltage difference between R/Bγ and Gγ after adjustment similar to that stated in [5] has been performed. (R/Bγ and Gγ output = 500 mVp-p)

[8] Temperature characteristics of AGC amplifier (Fig. 8)
Temperature variation of GX pin output when set to S=S3= 150 mV, and E1 is so adjusted that the output of pin ⑯ becomes 303 mV (Ta=25°C) (Set that Max G = ST)

[9] γ temperature characteristics (Fig. 9)
Temperature variation of Gγ output after the adjustment similar to that stated in [5] has been performed.

[10] Pedestal temperature characteristics (Fig. 11)
Set the outputs of Gγ and R/Bγ to 500 mVp-p after the adjustment similar to that stated in [5] has been performed. Adjust G pedestal to 25 mV (Ta=25°C) with E10. Then adjust B offset and R offset with E7 and E6 so that R and B pedestal of pin ㉛ become identical with G pedestal and then observe the temperature variation of R, G and B pedestals.

[11] AGC output voltage obtained by parameterizing AGC control voltage and Max gain voltage (Fig. 12)
The output voltage of AGC DET pin ⑨ is measured by inputting S=S3=50 mV and using AGC control voltage and Max gain voltage as a parameter, and thus the gain is calculated.

[12] Pedestal amount of G and R/Bγ output sections vs Pedestal adjustment voltage (Fig. 13)
The pedestal amount when E10 is varied by adjusting R and B offsets by adjusting E5 and E6 after the adjustment similar to that stated in [5] has been performed.

[13] R/B offset variable amount vs Offset regulation voltage (Fig. 14)
After performing similar adjustment as stated in [5], adjust E10 so that the pedestal amount of Gγ becomes 70 mV. Then, the pedestal amount at R/Bγ section is measured with offset which becomes variable by adjusting E5 and E6, and thus the difference between the pedestal amount of Gγ and that of R/Bγ is obtained.

AGC characteristics

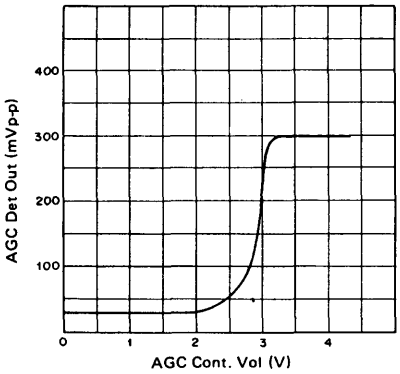


Fig. 1

G control characteristics

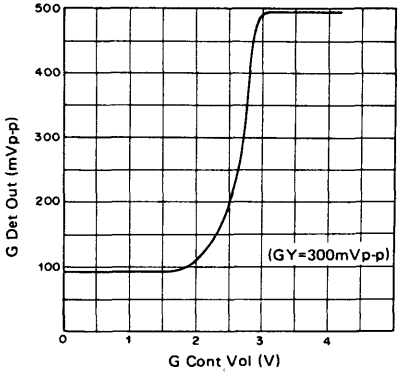


Fig. 2

B or R Cont characteristics

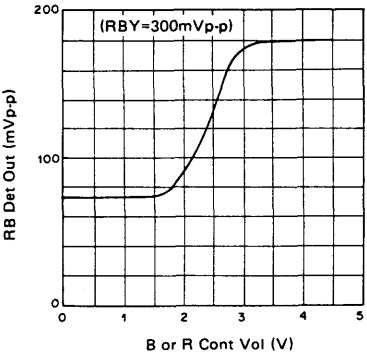


Fig. 3

B or R gain chracteristics

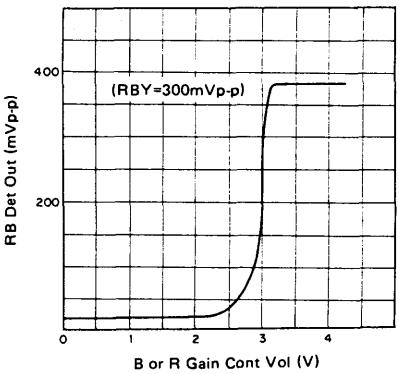


Fig. 4

γ characteristics

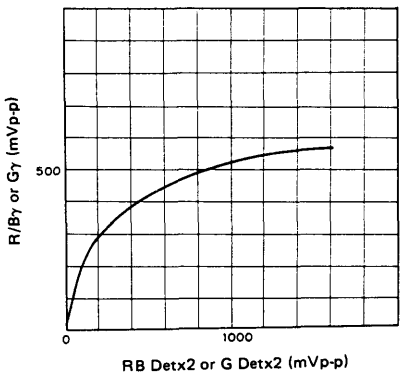


Fig. 5

AGC amplifier power supply voltage fluctuation characteristics

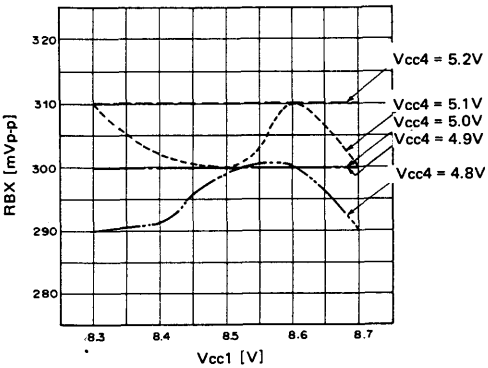


Fig. 6

γ output power supply voltage fluctuation characteristics

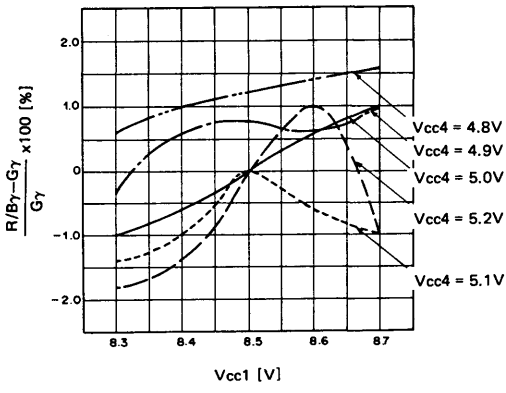


Fig. 7

AGC temperature characteristics

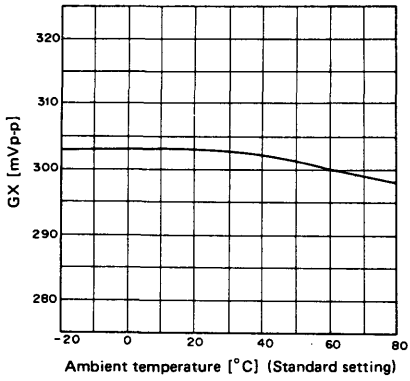


Fig. 8

γ temperature characteristics

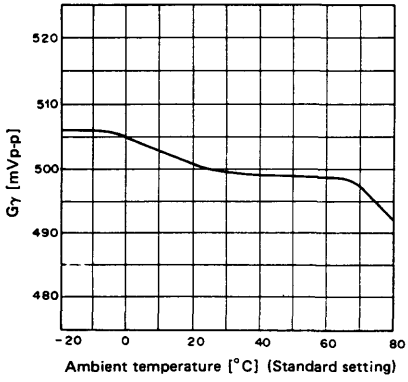


Fig. 9

Maximum allowable dissipation decreaseing curve

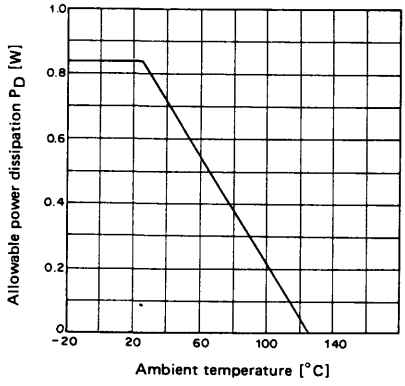
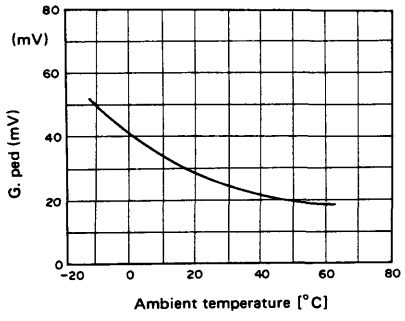
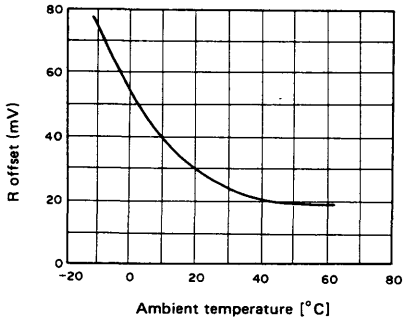


Fig. 10

Total pedestal (G pedestal) temperature characteristics



R offset (R pedestal) temperature characteristics



B offset (B pedestal) temperature characteristics

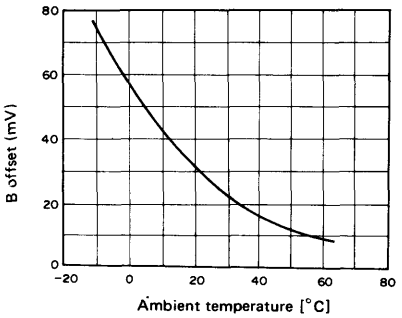


Fig. 11

AGC control voltage and Max gain voltage vs AGC amplifier amplification degree

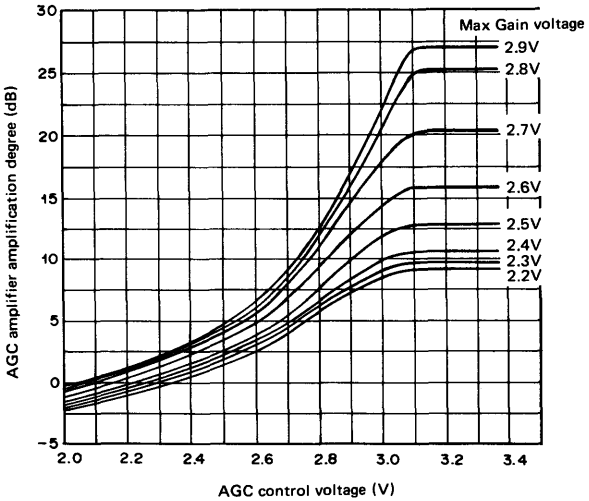


Fig. 12

Pedestal amount of G and R/Br output section vs Pedestal adjustable voltage

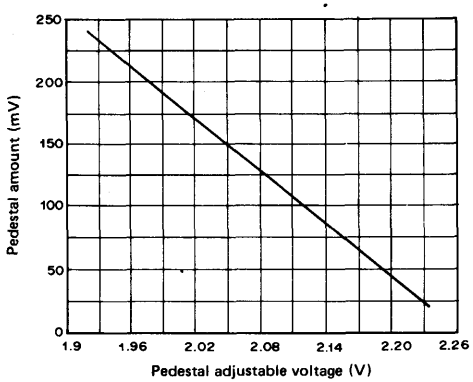


Fig. 13

R/B offset variable amount vs Offset adjustable voltage

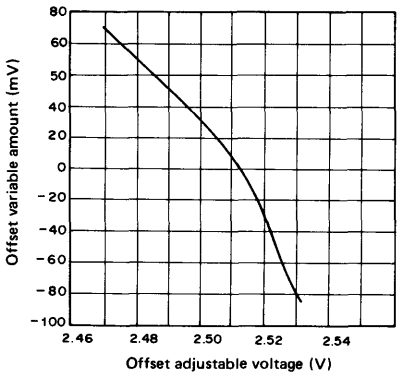
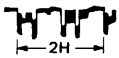
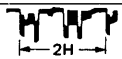
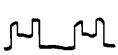
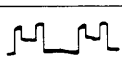
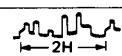
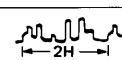
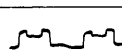
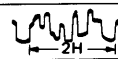
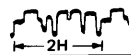
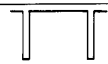
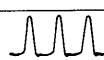
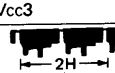


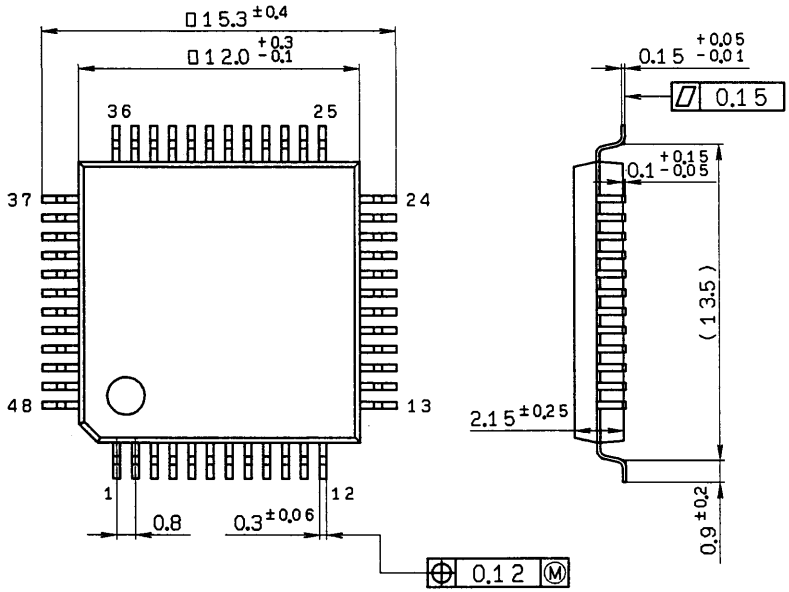
Fig. 14

Pin	DC [V]	AC [V]	Imp. [Ω]	Remark
1			<100	Accept with FET
2	6.9		>100k	
3	3.7		>7k	
4	5.0		<100	Accept with FET
5	5.0			Vcc4
6	4.6		<100	Accept with FET
7	3.7		>7k	
8	4.2	0.5 Vp-p	<200	
9	4.2	0.85 Vp-p	<200	
10	0.6		>100k	
11	2.5		>100k	
12	2.8		>100k	
13	2.6		>100k	
14	8.5			Vcc1
15	6.0	0.8 Vp-p	>5k	 H period
16	6.8	0.8 Vp-p	<200	 H period
17	6.8	0.52 Vp-p	<200	
18	6.0	0.52 Vp-p	>5k	
19	0			GND
20	1.8		>100k	
21	2.5		>100k	
22	2.5		>100k	
23	2.3		>100k	
24	2.3		>100k	
25	2.0		>100k	
26	2.7		>100k	
27	2.7		>100k	
28	2.3		>100k	
29	2.3		<100	
30	2.5	0.46 Vp-p	<100	 H period

Pin	DC [V]	AC [V]	Imp. [Ω]	Remark
31	2.5	0.5 Vp-p	<100	
32	4.3	0.3 Vp-p	<200	 H period
33	4.3	0.38 Vp-p	<200	
34	5.6	0.44 Vp-p	<100	
35	5.6	0.44 Vp-p	<100	
36	5.6	0.44 Vp-p	<100	
37	8.5			Vcc2
38	4.1	4.8 Vp-p	>3k	 H period
39	2.5	4.8 Vp-p	>7k	
40	0.7	4.8 Vp-p	>7k	 V period
41	0.7	5.4 Vp-p	>3k	 3.58 MHz
42	0.6	5.4 Vp-p	>3k	 3.58 MHz
43	0			GND
44	1.1	5.4 Vp-p	>3k	 7.16 MHz
45			>3k	
46	5.0			Vcc3
47	6.8	1.0 Vp-p	>50k	
48	0			GND

Package Outline Unit : mm

CX20053 48 pin QFP (Plastic) 0.7g



QFP-48P-L022

SONY

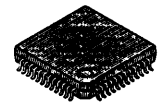
CX20055

Color Camera Encoder

Description

CX20055 is a bipolar IC designed for color camera encoders, compatible both with NTSC and PAL systems. It consists of such circuits as an aperture, blanking cleaning, pedestal set-up, white clip, sync, chroma modulation, phase shifter, fader, viewfinder switcher and 75 ohm cable driver.

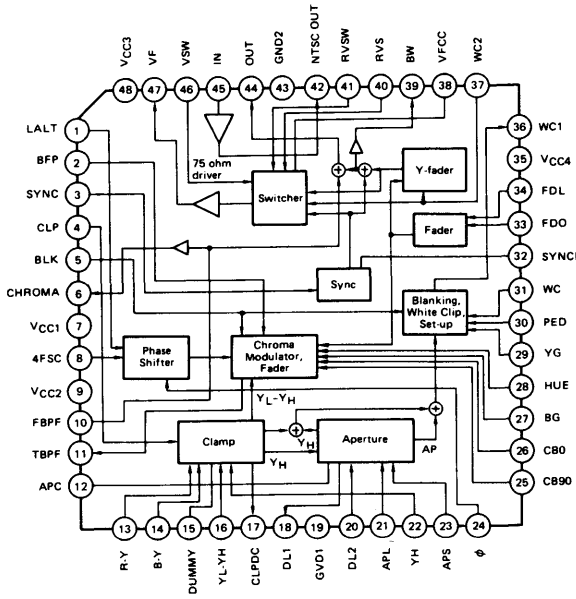
48pin QFP(Plastic)



Features

- Integrated color camera signal processing system when combined with CX20053, CX20054 (or CX200151), and CX20056.
- Digital phase shifter is incorporated to form the carrier's orthogonally-phased components to be modulated by the color difference signal.
- Compatible with NTSC and PAL systems.
- Luminance and Chroma (Chrominance) signals are output independently, as well as composite video and viewfinder output signals.
- The fader circuit is incorporated.
- A switch and circuit to select the viewfinder signal mode —B/W, COLOR, or RETURN VIDEO,— are self-contained.

Block Diagram



E89662-HP

Absolute Maximum Ratings (Ta = 25°C)

- Supply voltage V_{CC} 10 V
- Operating temperature Topr −10 to +60 °C
- Storage temperature Tstg −55 to +150 °C
- Allowable power dissipation P_D 833 mW

Recommended Operating Conditions

- Supply voltage $V_{CC1\sim3}$ 5.0 ±0.15 V
- Supply voltage V_{CC4} 8.5 ±0.2 V

Pulse Input Voltage CMOS level

	Min.	Max.	Unit
V_H	4.0	5.0	V
V_L	0	0.4	V

When Pin 8 has 1.25 ±0.25Vp-p.

Output Impedance

Pin 18 1kΩ ±200Ω

● Voltage of Input/Output Pins

Pin No.	Max. voltage (V)	Pin No.	Max. voltage (V)	Pin No.	Max. voltage (V)
1	≦ $V_{CC1\sim3}$	18	≦ $V_{CC1\sim3}$	35	
2	≦ $V_{CC1\sim3}$	19		36	≦ $V_{CC1\sim3}$
3	≦ $V_{CC1\sim3}$	20	≦ $V_{CC1\sim3}$	37	≦ $V_{CC1\sim3}$
4	≦ $V_{CC1\sim3}$	21	≦ $V_{CC1\sim3}$	38	≦ $V_{CC1\sim3}$
5	≦ $V_{CC1\sim3}$	22	≦ $V_{CC1\sim3}$	39	≦ $V_{CC1\sim3}$
6	≦ $V_{CC1\sim3}$	23	≦ $V_{CC1\sim3}$	40	≦ $V_{CC1\sim3}$
7		24	≦ $V_{CC1\sim3}$	41	Max. input current 500μA
8	≦ $V_{CC1\sim3}$	25	≦ $V_{CC1\sim3}$		
9		26	≦ $V_{CC1\sim3}$	42	≦ V_{CC4}
10	≦ $V_{CC1\sim3}$	27	≦ $V_{CC1\sim3}$	43	
11	≦ $V_{CC1\sim3}$	28	≦ $V_{CC1\sim3}$	44	≦ $V_{CC1\sim3}$
12	≦ $V_{CC1\sim3}$	29	≦ $V_{CC1\sim3}$	45	≦ V_{CC4}
13	≦ $V_{CC1\sim3}$	30	≦ $V_{CC1\sim3}$	46	≦ $V_{CC1\sim3}$
14	≦ $V_{CC1\sim3}$	31	≦ $V_{CC1\sim3}$	47	≦ $V_{CC1\sim3}$
15	≦ $V_{CC1\sim3}$	32	≦ $V_{CC1\sim3}$	48	
16	≦ $V_{CC1\sim3}$	33	≦ $V_{CC1\sim3}$		
17	≦ $V_{CC1\sim3}$	34	≦ $V_{CC1\sim3}$		

Allowable clamp pulse width
2.24μsec ±10%
When APL is 10 to 90% using a stair step signal.

Pin Description

No.	Symbol	I/O	Description
1	LALT	I	Phase inverting control for the subcarrier's 90° component. Ground pin terminal 1 for NTSC system.
2	BFP	I	Burst flag pulse input
3	SYNC	I	Sync pulse input
4	CLP	I	Clamp pulse input
5	BLK	I	Blanking pulse input
6	CHROMA	O	Modulated chroma signal output with burst
7	V_{CC1}		5V power supply for digital phase shifter
8	4FSC	I	Quadruple subcarrier inspect
9	V_{CC2}		5V power supply for luminance and chroma signal processing circuits
10	FBPF	I	Modulated chroma signal input through bandpass filter
11	TBPF	O	Modulated chroma signal output before bandpass filter
12	APC		Decoupling for aperture signal
13	R-Y	I	R-Y color difference input
14	B-Y	I	B-Y color difference input
15	DUMMY		Dummy clamp capacitor terminal
16	Y_L-Y_H	I	Y_L-Y_H luminance component input
17	CLPDC	O	Clamp voltage output
18	DL1	O	Y_H signal output to the delay line for aperture
19	GND1		Ground
20	DL2	I	Y_H signal input from the delay line for aperture
21	APL	I	Aperture signal amplitude control
22	Y_H	I	Y_H luminance component input
23	APS	I	Aperture signal slicer circuit control
24	ϕ	I	Phase adjustment of the modulated chroma signal's 90° phase component
25	CB90	I	Carrier balance adjustment of the 90° phase component
26	CB0	I	Carrier balance adjustment of the 0° phase component
27	BG	I	Burst amplitude adjustment
28	HUE	I	Burst phase adjustment
29	YG	I	Luminance level adjustment
30	PED	I	Set-up level adjustment
31	WC	I	White clip level adjustment
32	SYNCL	I	Sync level adjustment
33	FD0	I	Fader circuit gain adjustment
34	FDL	I	Fader signal input
35	V_{CC4}		8.5V power supply for 75 ohm driver circuit
36	WC1	O	White clip processing signal output
37	WC2	I	Luminance fader circuit input
38	VFCC		Decoupling of the viewfinder color mode signal
39	BW	O	B & W signal output with sync signal
40	RVS	I	Return video signal input
41	RVSW	I	Return video mode switcher
42	NTSCOUT	O	75 ohm composite signal input
43	GND2		Ground
44	OUT	O	500mVp-p composite signal output
45	IN	I	75 ohm driver input
46	VSW	I	B/W-color mode switch of the viewfinder output signal
47	VF	O	Viewfinder signal output
48	V_{CC3}		5V power supply for viewfinder block

Electrical Characteristics (Ta=25°C)

Item	Symbol	Measuring point	SW conditions 1	2	3	5	8	10	12	13	14	21	22	23	34	37	40	41	45	46	VR conditions VR25	VR26	VR27	VR28	VR29	VR30	VR31	Conditions	Min.	Typ.	Max.	Unit
5V circuit supply current	I1	I1	a	a	a	a	b	c	a	b	b	a	b	a	a	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	(Note 1) ST	(Note 1) ST	3.0V	3 signals are input: SIG Y-1 400mVp-p, SIG BY-1 200mVp-p, SIG RY-1 200mVp-p	27.0	39.0	51.7	mA
8.5V circuit supply current	I2	I2	a	a	a	a	b	c	a	b	b	a	b	a	a	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	6.3	12.5	19.3	mA
Pin (17) potential	P17	M17	a	a	a	b	a	a	a	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	DC potential measuring	3.2	3.65	4.2	V
Pin (24) potential	P24	M24	a	a	a	b	a	a	a	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	2.3	2.7	3.1	V
Max. aperture level	APLH	M12	a	b	b	b	a	a	b	a	a	b	b	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Input potential SIG Y-2 2MHz, 300mVp-p	405	700	1100	mV
Min. aperture level	APLL	M12	a	b	b	b	a	a	b	a	a	a	b	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	0	0.5	11	mV
Aperture range	APR	M12	a	b	b	b	a	a	b	a	a	b	b	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Measurement of the output V_1 when 100mVp-p sine wave of SIG Y-2 = 2MHz is input, and the output V_2 when 100mVp-p sine wave of SIG Y-2 = 0.5MHz is input. Rating 20 x log (V_1/V_2)	15.0	18.0	21.0	dB
Aperture dynamic range	APD	M12	a	b	b	b	a	a	b	a	a	b	b	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Measurement of the V_1 when 300mVp-p sine wave of SIG Y-2 = 2MHz is input and the V_2 when 600mVp-p sine wave of SIG Y-2 = 2MHz is input. Rating V_2 (2V_1)	0.68	0.88	1.10	–
Y BLK level	BLKL	M36	a	b	b	a	a	a	a	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Measure the set-up level after set-up amount is set to maximum with VR30.	239	310	396	mV
Min. set-up	PDH	M36	a	b	b	a	a	a	a	a	a	a	a	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	3.0V	3.0V	Measure the set-up amount. Its polarity waveform is indicated by the right arrow direction as positive. BLK period Pin 36 output	-5.5	0	5.5	mV
Y gain offset	YGO	M36	a	b	b	a	a	a	a	a	a	a	a	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	3.0V 2.0V	VR	3.0V	Adjust VR30 so the set-up output becomes 200mV when VR29 is 3.0V. Then, set VR29 to 2.0V and measure the set-up amount. Rating V_1 -200mV	0	0	66	mV
Aperture slice offset	APSO	M36	a	b	b	a	a	a	a	a	a	a	a	a	a/b	a	b	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Adjust VR30 so the set-up output becomes 200mV when S23 is a, then measure the set-up amount after S23 is set to b. Rating V_1 -200mV	0	0	88	mV
Max. Y gain	YGH	M36	a	b	b	a	a	a	a	a	a	a	a	b	a	a	b	a	a	a	2.5V	2.5V	2.3V	2.5V	3.0V	VR	3.0V	Adjust VR30 so the output set-up becomes 50mV. Measure the output (excluding the set-up) when SIG Y-1 = 360mVp-p is input.	414	500	605	mV
Min. Y gain	YGL	M36	a	b	b	a	a	a	a	a	a	a	a	a	b	a	a	b	a	a	2.5V	2.5V	2.3V	2.5V	2.0V	VR	3.0V	Ditto, with the input signal level of SIG Y-1 = 100mVp-p.	23	45	88	mV
Y_H dynamic range	YHD	M36	a	b	b	a	a	a	a	a	a	a	a	a	b	a	a	b	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Adjust VR30 so the output set-up becomes 50mV. Calculate as in Note 2 using the M36 Y output component when SIG Y-1 = 500mVp-p is input.	0	2.6	4.4	%
White clip	WC	M36	a	b	b	a	a	a	a	a	a	a	a	a	b	a	a	b	a	a	2.5V	2.5V	2.3V	2.5V	3.0V	2.5V	(Note 1) ST	Measure the signal amplitude from output black level when SIG Y-1 = 500mVp-p.	405	490	605	mV
Aperture slice OFF	APSOFF	M36	a	b	b	a	a	a	c	a	a	a	a	a	c	a	b	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Adjust VR30 so the output set-up becomes 200mV. Input 2MHz SIG (APL = 50mVp-p) and measure the output.	234	300	374	mV
Aperture slice ON	APSON	M36	a	b	b	a	a	a	c	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Ditto	0	0	5.5	mV
Sync level NTSC output	SNT	M42	a	b	a	b	a	a	a	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Measure sync level	513	595	682	mV
Sync level VF	SVF	M47	a	b	a	b	a	a	a	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	239	280	325	mV
Sync level BW	SBW	M39	a	b	a	b	a	a	a	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	248	290	336	mV
Sync level Return video	SRV	M47	a	b	a	b	a	a	a	a	a	a	a	a	b	b	b	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Sync level when SIG RV ~ 300mVp-p sync signal is input.	239	282	325	mV
Y level NTSC output	YNT	M42	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Y signal output when SIG WC ~ 450mVp-p is input.	1.2	1.4	1.60	V
Y level BW	YBW	M39	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	554	660	754	mV
Y level VF (BW)	YVFB	M47	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	572	680	776	mV
Y level VF (color)	YVFC	M47	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	b	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	527	660	759	mV
Y level VF (RV)	YVFR	M47	a	b	a	c	a	a	a	a	a	a	a	a	a	a	b	b	b	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Y signal output when B/W (APL 50%) SIG RV = 1Vp-p (Y input = 700mV) is input.	585	662	742	mV
Y dynamic range NTSC output	YDNT	M42	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Calculate (Note 2) using the input when the SIG WC ~ 500mVp-p Y signal is input.	0	0.5	2	%
Y dynamic range BW	YDBW	M39	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	0	1.25	4	%
Y dynamic range VF (BW)	YDVFB	M47	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	0	2	12	%
Y dynamic range VF (color)	YDVFC	M47	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	b	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	0	2	13	%
Chroma dynamic range NTSC output	CDNT	M42	a	b	b	b	a	b	a	a	a	a	a	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Measure the output V_1 when 200mVp-p of SIG BPF ~ 4MHz sine wave and the output V_2 when 400mVp-p are input.	0	1.0	2.2	%
Chroma dynamic range CHROMA	CDCHR	M6	a	b	b	b	a	b	a	a	a	a	a	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Ditto	0	0.2	4	%
Chroma level CHROMA	CLCHR	M6 M42	a	b	b	b	a	b	a	a	a	a	a	a	a	b	a	a	a	b	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	Measure the output amplitudes of M7 and M42 when 200mVp-p sine wave with SIG BPF ~ 4MHz is input. Rating 2V_1/(V_1 -1 x 100	0	5	12	%
Chroma level VF (color)	CLVFC	M42 M47	a	b	b	b	a	b	a	a	a	a	a	a	a	b	a	a	a	b	2.5V	2.5V	2.3V	2.5V	ST	ST	3.0V	– ditto –, with V_1 = M47 output amplitude	0	-5	18	%

Item	Symbol	Measuring point	SW conditions 1	2	3	5	8	10	12	13	14	21	22	23	34	37	40	41	45	46	VR conditions VR25	VR26	VR27	VR28	VR29	VR30	VR31	Conditions	Min.	Typ.	Max.	Unit
Frequency	F	M42	a	b	b	a	a	a	a	a	a	a	b	a	a	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Input SIG Y-2 = 100mVp-p at 0.5MHz and 4MHz. Adjust VR30 so the output is not distorted when 0.5MHz is input, then measure its output V_1 and the V_2 when 4MHz are input. Rating 20 x log (V_1/V_2)	-6.5	-3.5	-1.5	dB
Switcher test 1	VSWBC	M47	a	b	a	c	a	b	a	a	a	a	a	a	a	b	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Measure the output amplitude at 0.5MHz when 300mVp-p with SIG BPF = 0.5MHz is input.	0	7	17	mV
Switcher test 2	VSWCB	M47	a	b	a	c	a	a	a	a	a	a	a	a	a	c	a	a	a	b	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Measure Y output when SIG WC = 450mVp-p is input, with Pin 38 open.	0	1	17	mV
Switcher test 3	RVSWB	M47	a	b	a	c	a	a	a	a	a	a	a	a	a	c	b	b	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Input SIG RVAPL = 1Vp-p and SIG WCAPL = 450mVp-p and measure the cross-talk at the sync tip of output signal.	0	0	17	mV
Switcher test 4	RVSWC	M47	a	b	a	c	a	b	a	a	a	a	a	a	a	c	b	b	a	b	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Measure as above with the input signal and SIG BPF = 200mVp-p input.	0	0	17	mV
Y fader	YFD	V34 M42	a	b	b	c	a	a	a	a	a	a	a	a	b	c	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Adjust V34 so M42 Y output becomes 100mVp-p when SIG WC = 450mVp-p is input and measure the V34 voltage.	1.1	1.35	1.7	V
Burst OFF	BFPH	M42	a	b	b	c	b	c	a	a	a	a	a	a	b	a	a	a	a	a	2.5V	2.5V	2.3V	2.5V	ST	VR	3.0V	Measure the 3.58MHz output amplitude. Absolute value	0	0	11	mV
Carrier Bal. NTSC	CBNT	Vector-scope M42	b a	a	b	a	b	c	a	a	a	a	a	a	a	b	a	a	a	a	(Note 3) Cal	(Note 3) Cal	(Note 3) Cal	(Note 3) Cal	ST	VR	3.0V	Align the split bursts on the vectorscope using VR28 with S_1 set at b, and set to 75% burst using VR27. Adjust the carrier balance with V25 and V26. With S_1 set at a, measure the leakage of the carrier (Note 4).	37	41	–	dB
Carrier Bal. PAL	CBPAL	Vector-scope M42	c	a	b	a	b	c	a	a	a	a	a	a	b	a	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure the carrier leakage (Note 4)	29	35	–	dB
Carrier's orthogonal degree 1	0DEC	Vector-scope	b	a	b	a	b	c	a	b	b	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure the phase difference between the B-Y axis and the burst when SIG BY-2 and SIG RY-2 = 100mVp-p are input.	-11	0	11	deg.
Carrier's orthogonal degree 2	90DEC	Vector-scope	b	a	b	a	b	c	a	b	b	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure the phase difference between the burst and 90° (R-Y) axis with the above signal input.	-11	0	11	deg.
Carrier's orthogonal degree 3	-90DEC	Vector-scope	b	a	b	a	b	c	a	b	b	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure the phase difference between the burst and 270° (R-Y) axis with the above signal input.	-11	0	11	deg.
Chroma BLK offset	CBLIK	M11	a	a	b	a	b	c	a	a	a	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure BLK pulse amplitude with M11.	0	0	72	mV
Max. Burst gain	BGH	M42	a	a	b	a	b	c	a	a	a	a	a	a	b	a	a	a	a	a	Cal	Cal	3.0V	Cal	ST	VR	3.0V	Measure burst amplitude	1.1	1.5	2.2	V
Min. Burst gain	BGL	M42	a	a	b	a	b	c	a	a	a	a	a	a	b	a	a	a	a	a	Cal	Cal	2.0V	Cal	ST	VR	3.0V	Ditto	81	150	360	mV
Hue control	HUEH	M42	a	a	b	a	b	c	a	a	a	a	a	a	b	a	a	a	a	a	Cal	Cal	VR	Cal 3.0V	ST	VR	3.0V	Measure the burst phase variation when VR28 is varied from Cal to 3.0V. (Level is adjusted with VR27).	41	60	83	deg.
B-Y level	BY	M42	a	a	b	a	b	c	a	a	b	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure 3.58MHz output amplitude when SIG BY-2 = 100mVp-p	0.65	0.91	1.10	V
R-Y level	RY	M42	a	a	b	a	b	c	a	b	a	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure 3.58MHz output amplitude when SIG RY-2 = 100mVp-p.	0.9	1.3	1.5	V
B-Y dynamic range	BYD	M42	a	a	b	a	b	c	a	a	b	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Measure the outputs V_1 and V_2 when SIG BY-2 = 100mVp-p and 200mVp-p are input.	0	2	7	%
R-Y dynamic range	RYD	M42	a	a	b	a	b	c	a	b	a	a	a	a	a	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	VR	3.0V	Ditto, but with the input signal SIG RY-2	0	5	12.7	%
C fader	CFD	M42	a	b	b	a	b	c	a	b	a	a	a	a	b	b	a	a	a	a	Cal	Cal	Cal	Cal	ST	ST	3.0V	Adjust V34 so M42 3.58MHz chroma output becomes 100mVp-p when SIG RY-2 = 100mVp-p is input, then measure V34 voltage.	1.1	1.35	1.7	V
DG output amplifier	DG	M42	a	b	b	b	a	c	a	a	a	a	a	a	a	b	a	a	b	a	Cal	Cal	Cal	Cal	ST	ST	3.0V	Input DG and DP measuring signals with SIG IN = 500mVp-p (DC 4.25V and APL 50%) and measure DG.	–	1.5	3	%
Output amplifier dynamic range	OAD	M42	a	b	b	b	a	c	a	a	a	a	a	a	a	b	a	a	b	a	Cal	Cal	Cal	Cal	ST	ST	3.0V	Measure the output amplitude value when SIG IN = 3.6VDC + 6Vp-p (100kHz) sine wave is input.	4.6	5.8	7.2	V

(Note 1) The ST in VR conditions indicates a VR condition showing voltages VR29 = 2.410V, VR30 = 2.725V and VR31 = 2.771V with the IC removed from the VR mid-point.

(Note 2) Calculation (Note 2) is as follows:

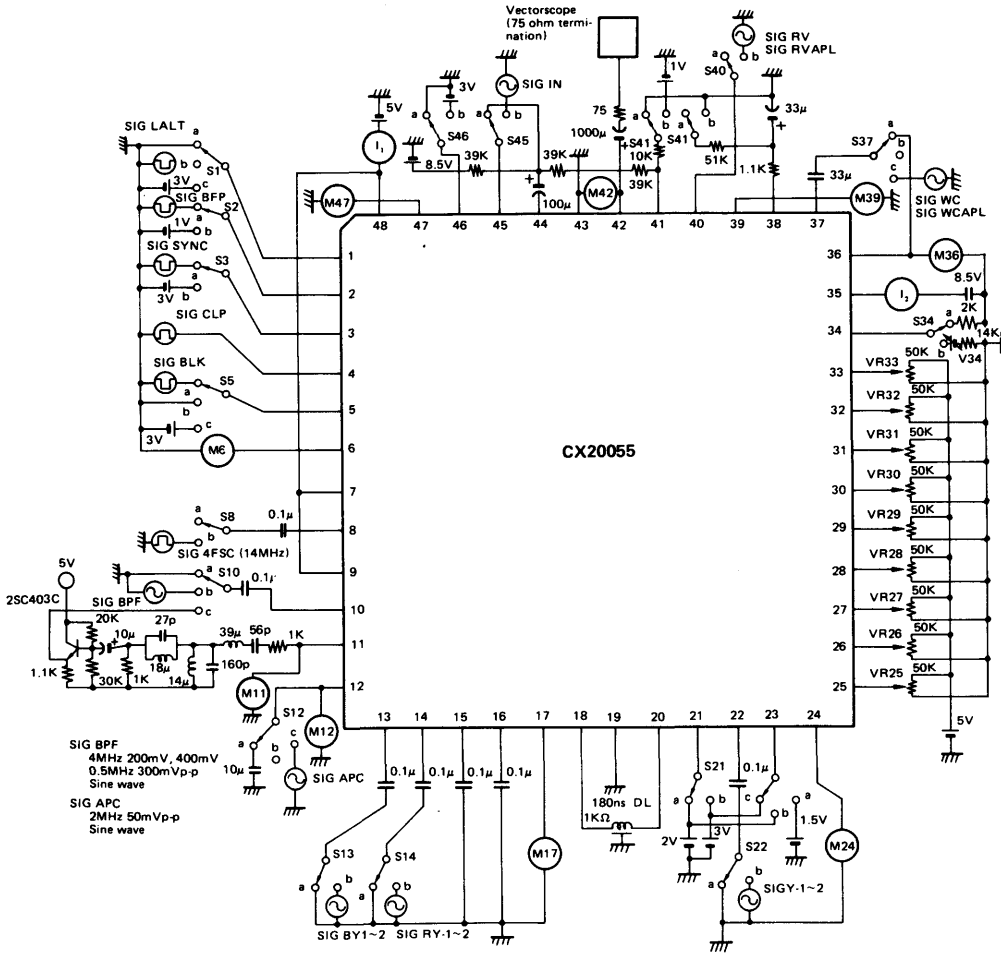
$$\left| \frac{V_O(t)}{V_O} - \frac{V_i(t)}{V_i} \right| \text{ is M, where } V_i(t) \text{ is the input signal, } V_O(t), V_i(t) \text{ component out of the output signal, } V_i, \text{ the maximum } V_i(t) \text{ and } V_O, \text{ the maximum } V_O(t).$$

Calculate 100X M (%) when the maximum

(Note 3) The Cal in VR conditions indicates each of VR25–28 values when it is adjusted according to the conditions of the item (Carrier Bal. NTSC).

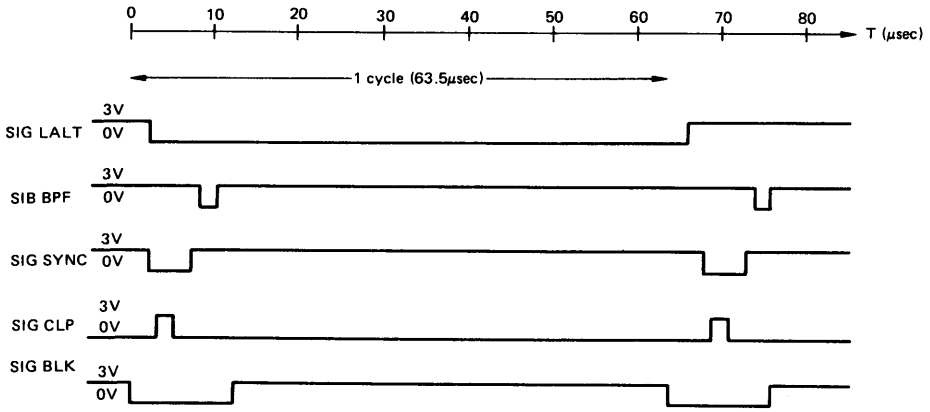
(Note 4) Measure 3.58MHz amplitude V_1 of the video period and burst (75%) amplitude V_2, then calculate 20 x log (V_1/V_2).

Electrical Characteristic Test Circuit

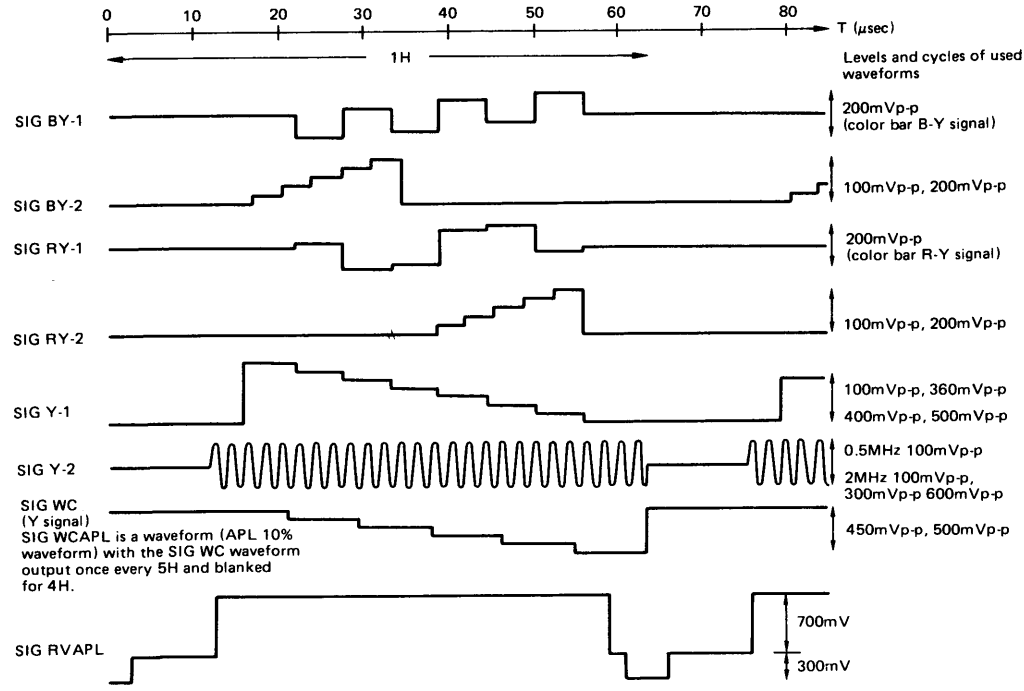


VR32 and VR33 indicate a VR condition when VR32 = 2. 189V and VR33 = 2. 412V with the IC removed and open.

Synchronized Signal Waveform

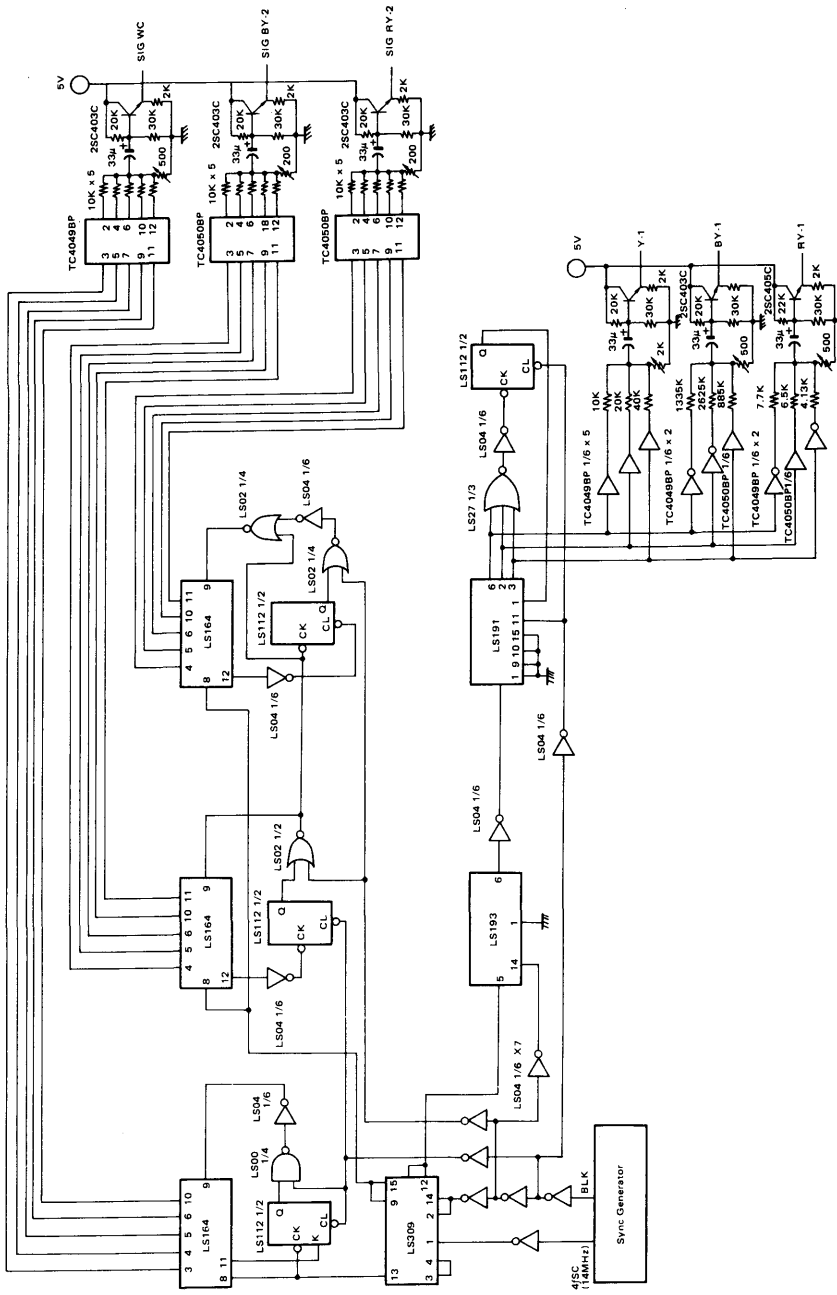


Input Signal Waveform



(Note) SIG RVAPL waveform only is synchronized with SIG WC waveform peak in a RVAPL Sync period (waveform: APL 90%).

Signal Waveform Generation Circuit Diagram



Reference Pin Voltage DC Characteristics (Ta=25°C Vcc1~3=5V, Vcc4=8.5V)
Refer to Electrical Characteristic Test Circuit

Pin No.	Pin voltage (V)	Pin No.	Pin voltage (V)
6	3.17	22	3.57
8	3.16	24	2.75
10	2.23	32	2.49
11	3.24	36	2.60
12	2.54	37	2.12
13	3.57	38	2.29
14	3.57	39	2.88
15	3.57	40	3.97
16	3.57	42	5.90
17	3.62	44	3.04
20	2.92	47	2.65

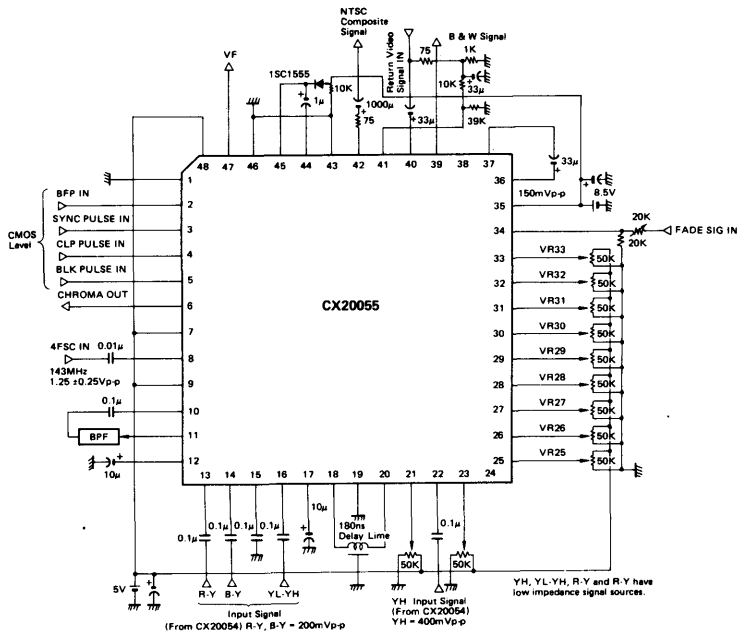
Test Conditions

S1	S2	S3	S5	S8	S10	S12	S13	S14	S21	S23	S34	S37	S40	S41	S45	S46
a	b	b	b	a	a	a	a	a	a	a	a	b	a	a	a	a

VR25	VR26	VR27	VR28	VR29	VR30	VR31	VR33	V34
2.5V	2.5V	2.5V	2.5V	2.5V	3V	3V	2.5V	3V

Pin 32 is open.

Application Circuit (NTSC Mode)



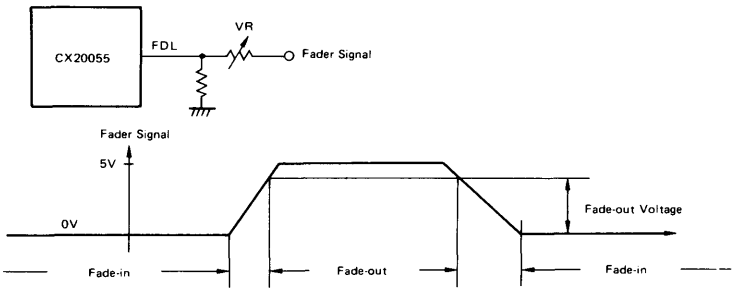
References for Circuit Design

(1) NTSC and PAL systems

- NTSC system
  Ground LALT (Pin 1) terminal.
- PAL system
  Input a phase inverting signal every 1H to LALT (Pin 1) terminal.

$$CPAL = U\sin\omega t + V\cos\omega t \text{ ------- } LALT = \text{"L"}$$
$$U\sin\omega t - V\cos\omega t \text{ ------- } LALT = \text{"H"}$$

(2) Fader Signal (CMOS Level)

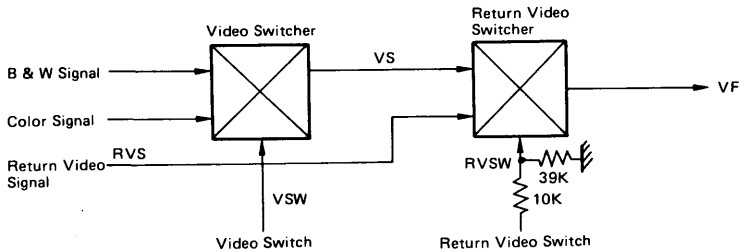


With the fader signal, the composite video (Pin 42), B & W (Pin 39), CHROMA (Pin 6) and viewfinder (Pin 47, when viewfinder output signal has a color mode) output signals are faded in or out.
(Refer to Y, CHROMA FADE-IN/OUT CHARACTERISTICS on page 14 as well as the above diagram).
With the above diagram, the fader-out voltage is determined by VR.

Fader signal	Mode
"L" level	Fade-in
"H" level	Fade-out

(3) Viewfinder switch (i)

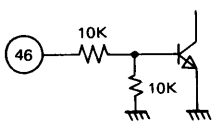
The viewfinder switching systems are available; video switch (VSW) and return video switch (RVSW).



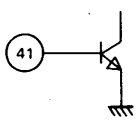
VSW	RVSW	VF
"L"	"L"	B & W mode
"H"	"L"	Color mode
"L" or "H"	"H"	Return video mode

The switcher input is as shown in the diagram below.

Video switcher input



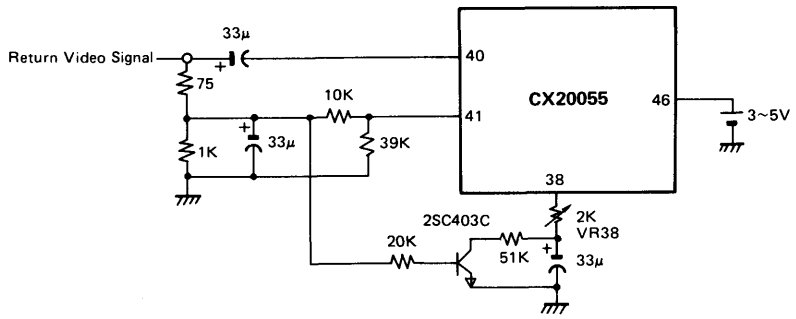
Return video switcher input



Video switcher has "H" level = 3 ~ 5V, return video switcher has ("H" level) with 10K and 39K external resistors.

(4) Viewfinder switch (ii)

When using a color mode, modify the circuit as in the diagram below. In this case, adjust the output level using VR38 (see below).



(5) Caution in burst adjustment (Refer to EXAMPLE OF APPLICATION CIRCUIT)

Burst is a composite signal of the carrier's 0° component $\sin\omega$ sct and 90° component $\cos\omega$ sct as in the following equation.

$$\text{Burst} = A\,[\sin\omega\,\text{sct} + B\cos\omega\,\text{sct}]$$

where A is a gain determined by VR27 and B by VR28.

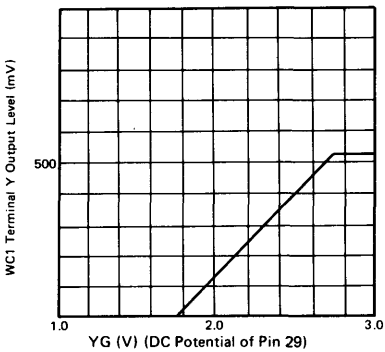
Hence, the burst amplitude varies when the hue is varied with VR28. Therefore, adjust the burst amplitude with VR27 (BG) only after VR28 (HUE) is adjusted.

(6) Adjustment of luminance and chroma signals (Refer to EXAMPLE OF APPLICATION CIRCUIT)

- Adjust VR29 so Pin 36 output becomes 450mVp-p.
- Adjust the luminance level of Pin 42 output with VR33.
- Adjust the chroma level of Pin 42 output with the input level variation of Pin 13 and Pin 14.

Control Characteristics

YG Control Characteristics



YG (V) (DC Potential of Pin 29)

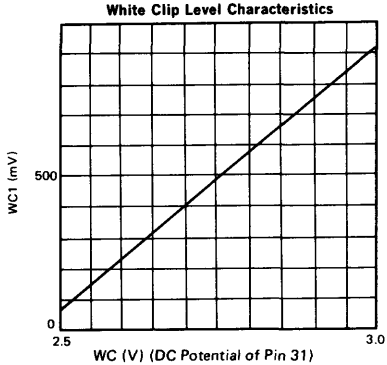
YH = 400mV Stayer Step

Measuring item (YGMAX) condition

Measure Y signal level of Pin 36 excluding set-up with SIGY-1 = 400mV and VR29 made variable.

Fig. 1

White Clip Level Characteristics

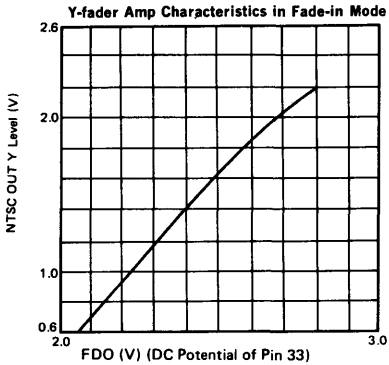


WC (V) (DC Potential of Pin 31)

Measure the clipped Y signal level of Pin 36 when VR31 is varied with measuring item in (WC) condition.

Fig. 3

Y-fader Amp Characteristics in Fade-in Mode



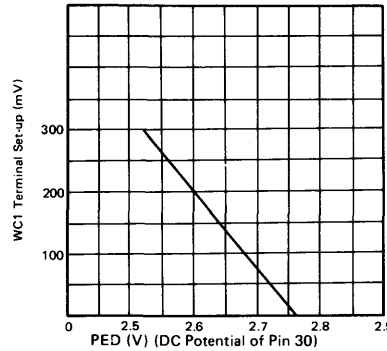
FDO (V) (DC Potential of Pin 33)

WC2 = −450mV stayer step input

Measure the Y output level of Pin 42 when VR33 is varied with measuring item in (YFD) condition.

Fig. 5

Set-up Characteristics

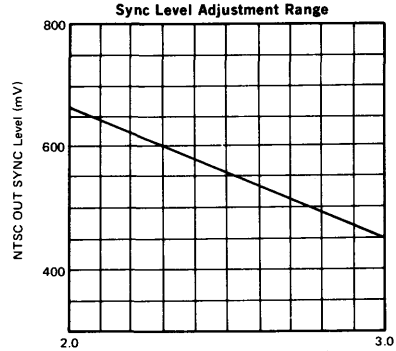


PED (V) (DC Potential of Pin 30)

Measure the clipped Y signal level of Pin 36 when VR30 is varied, with measuring item in (BKL) condition.

Fig. 2

Sync Level Adjustment Range

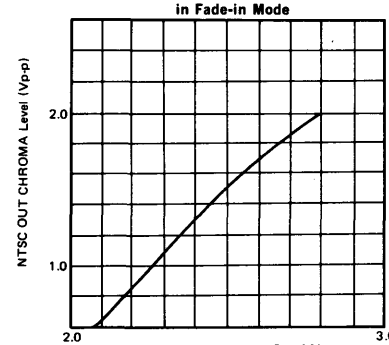


SYNC L (V) (DC Potential of Pin 32)

Measure the SYNC output level of Pin 42 when VR32 is varied with measuring item in SYNCNT condition.

Fig. 4

Chroma Fader Amp Characteristics in Fade-in Mode



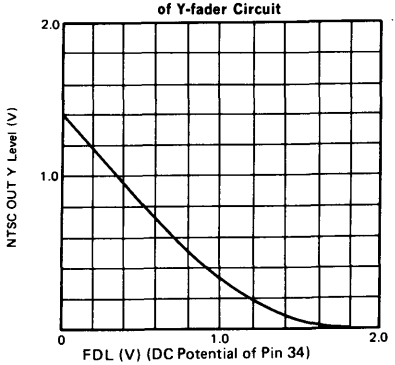
FDO (V) (DC Potential of Pin 33)

(B-Y) or (R-Y) = 100mV input

Measure the chroma output level of Pin 42 when VR33 is varied with measuring item in (CFD) condition.

Fig. 6

Fade-in/Face-out Characteristics of Y-fader Circuit

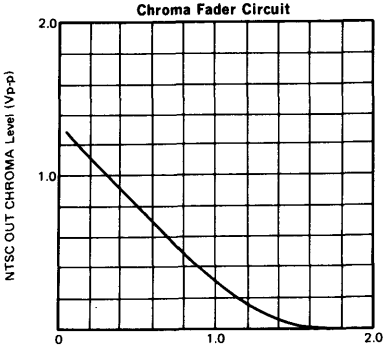


FDL (V) (DC Potential of Pin 34)
WC2 = -450mV stayer step input
FDO = 2.45V

Measure Y output level of Pin 42 when V34 is varied with measuring item in ⟨ YFD ⟩ condition.

Fig. 7

Fade-in/Fade-out Characteristics of Chroma Fader Circuit

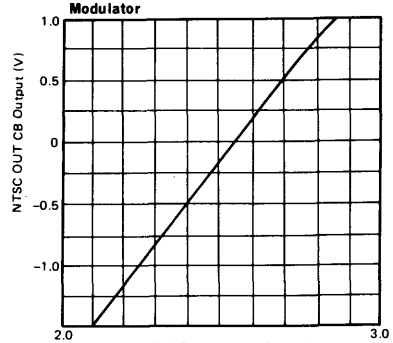


FDL (V) (DC Potential of Pin 34)
(B-Y) or (R-Y) = 100mV input

Measure the chroma output level of Pin 42 when V34 is varied with measuring item in ⟨ CFD ⟩ condition.

Fig. 8

Carrier Balance Characteristics of B-Y chroma Modulator

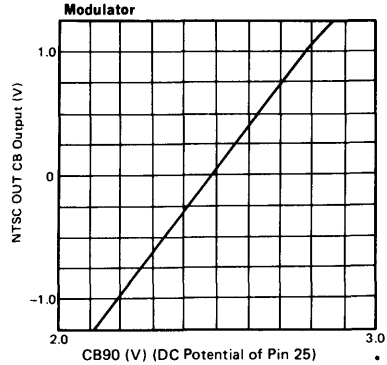


CBO (V) (DC Potential of Pin 26)
CB90 = Cal

Measure chroma level Pin 42 when VR26 is varied with measuring item in ⟨ CB ⟩ condition.

Fig. 9

Carrier Balance Characteristics of R-Y Chroma Modulator

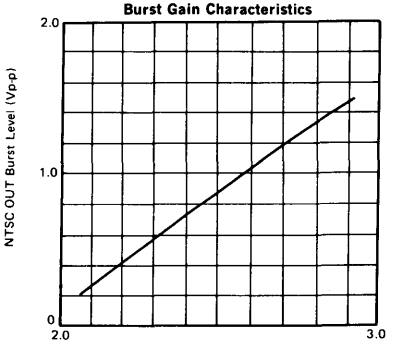


CB90 (V) (DC Potential of Pin 25)
CBO = Cal

Measure chroma level of Pin 42 when VR25 is varied with measuring item in ⟨ CB ⟩ condition.

Fig. 10

Burst Gain Characteristics

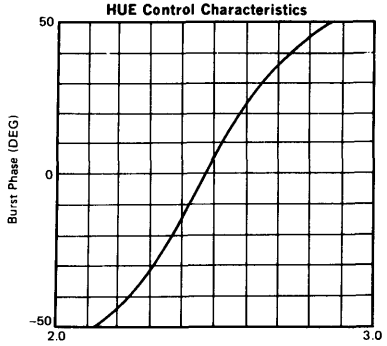


BG (V) (DC Potential of Pin 27)
HUE = Cal

Measure the burst level of Pin 42 output when VR27 is varied with measuring item in ⟨ BGH ⟩ condition.

Fig. 11

HUE Control Characteristics



HUE (V) (DC Potential of Pin 28)

Measure the output of Pin 42 using a vectorscope with measuring item in ⟨ HUEH ⟩ condition.

Fig. 12

VCC1 ~ 3 5V Power Supply Characteristics
Measuring point: Pin 42 output
VCC4 = 8.5V constant

Y Output Power Supply Variation Characteristics

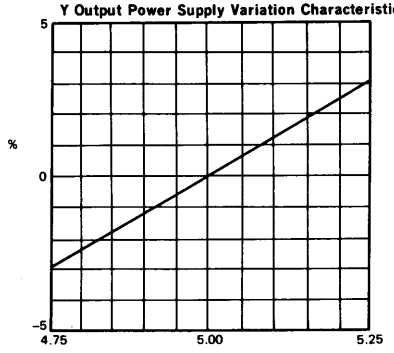


Fig. 13

SYNC Output Voltage Variation Characteristics

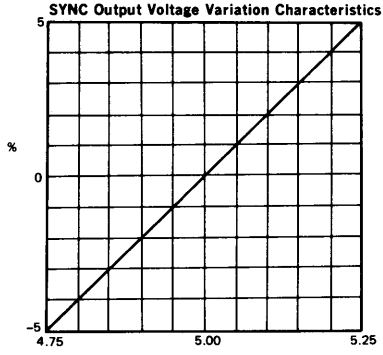


Fig. 14

Burst Output Power Supply Voltage Variation Characteristics

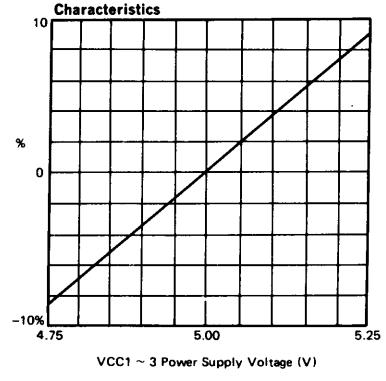


Fig. 15

CHROMA Output Power Supply Voltage Variation Characteristics

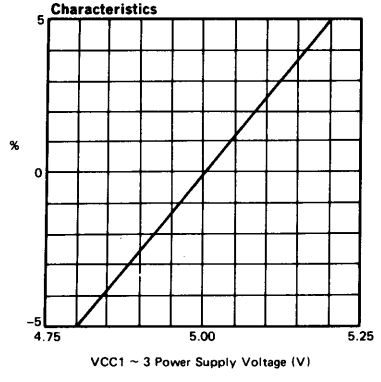


Fig. 16

VCC4 8.5V Power Sunply Voltage Characteristics (Measuring Output of Pin 42)

(Refer to item "Output Amp D Range" of ELECTRICAL CHARACTERISTICS)

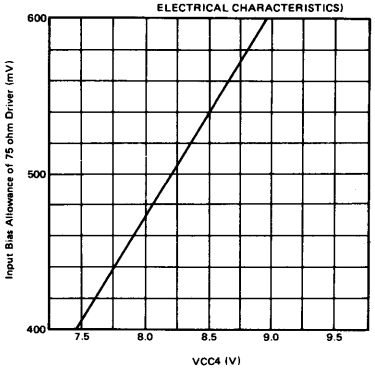
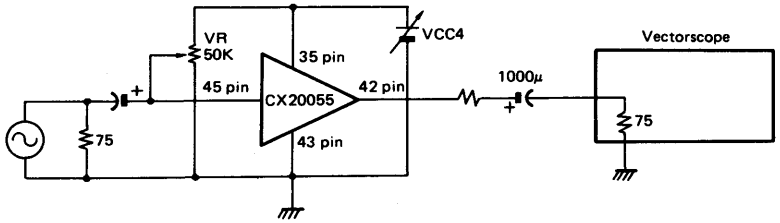


Fig. 17

Test Method of VCC4 8.5V Power Supply Voltage Variations



CX20055 is connected as shown above, with connecting terminals other than Pins 35, 42, 43 and 45 being open or in ⟨DG⟩ condition of electrical characteristics.

As signal sources, DG and DP measuring signals (APL: 50%) are used.

(1) Adjust the signal source output so the DC voltage of Pin 45, being set at 4.05V, becomes 1Vp-p signal sigh the 75 ohm termination of Pin 42 output (VCC4 = 8.5V).

(2) Set VCC4 at a measuring power supply voltage changing from 8.5V.

(3) Measure the DC voltage of Pin 45 when sync level decreases by 5% compared with that of (2) (VDC1). At this time, adjust VR so the DC voltage of Pin 45 decreases.

(4) Adjust VR so the DC voltage of Pin 45 increases and measure its voltage when DG is 2% (VDC2).

Fig. 17 is a diagram with the range VDC1 to VDC2 (VDC2-VDC1) defined as an input bias allowance.

Temperature Characteristics (Pin 42 Output)

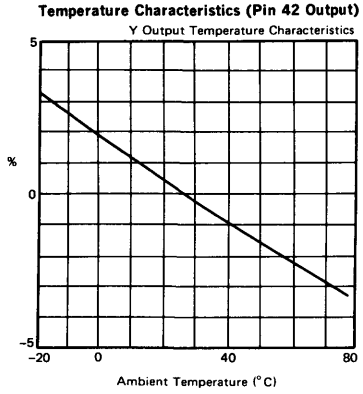


Fig. 18

Y/SYNC Temperature Characteristics

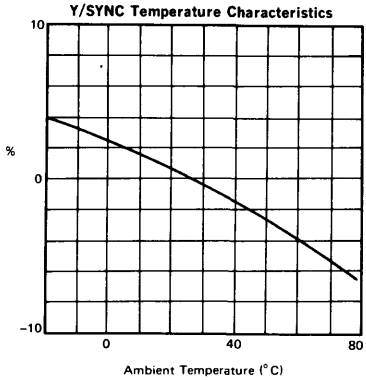


Fig. 19

Burst Output Temperature Characteristics

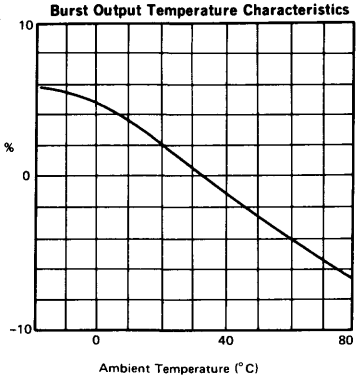


Fig. 20

CHROMA (Red)/Burst Temperature Characteristics

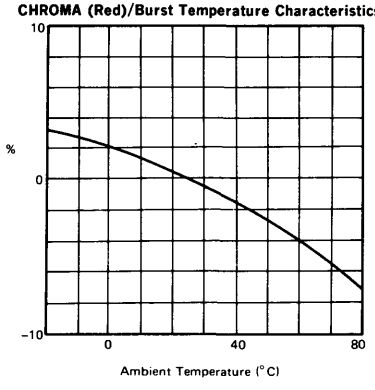


Fig. 21

Maximum Allowable Power Dissipation Decrement Curve

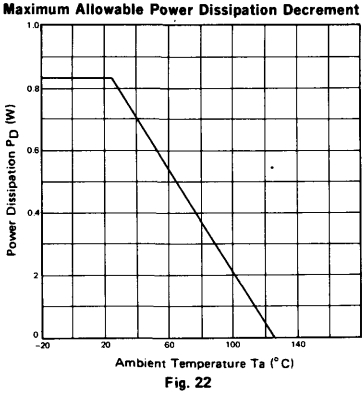


Fig. 22

White Clip Characteristics

(ST: WC1 White clip circuit input at standard output level of 400mV)

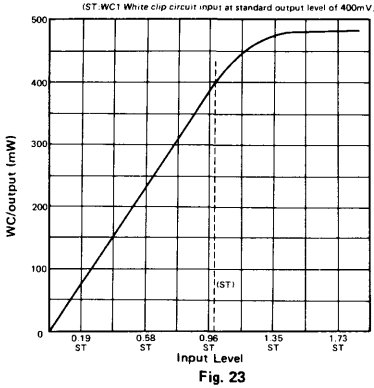
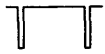
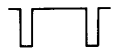
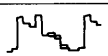
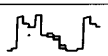


Fig. 23

Terminal Reference Value

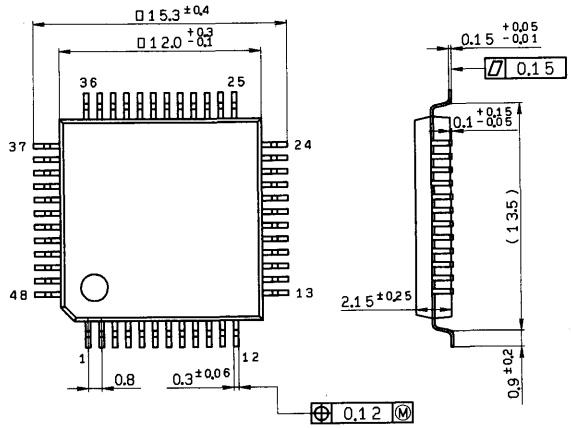
(When using a device ICX016K)

Pin	DC [V]	AC [V]	Imp [Ω]	Remark
1	0		> 7k	
2	3.9	4.0Vp-p	> 7k	 H cycle
3	3.8	4.0Vp-p	> 7k	 H cycle
4	0.1	4.0Vp-p	> 7k	 H cycle
5	3.0	3.7Vp-p	> 10k	 H cycle
6			< 200	
7	5.0			$V_{CC}3$
8	2.5	5.4Vp-p	> 7k	 14.32MHz
9	5.0			$V_{CC}2$
10	2.2	0.4Vp-p	> 7k	
11	3.2	1.05Vp-p	< 200	
12	2.5		> 2k	
13	3.6	0.27Vp-p	> 100k	
14	3.6	0.34Vp-p	> 100k	
15	3.6		> 100k	
16	3.6		> 100k	
17	3.6		< 50	
18	3.1	0.5Vp-p	≃ 1k	 H cycle
19	0			GND
20	3.1	0.5Vp-p	> 50k	 H cycle
21	2.4		> 100k	
22	3.8	0.5Vp-p	> 100k	 H cycle
23	2.1		> 100k	
24	2.5		> 9k	

Pin	DC [V]	AC [V]	Imp [Ω]	Remark
25	2.5		> 100k	
26	2.5		> 100k	
27	2.3		> 100k	
28	2.4		> 100k	
29	2.3		> 100k	
30	2.7		> 100k	
31	2.8		> 100k	
32	2.3		> 7k	
33	2.4		> 100k	
34	0.1		> 100k	
35	8.5			$V_{CC}1$
36	2.1	0.7Vp-p	< 100	 H cycle
37	2.1	0.7Vp-p	> 7k	 H cycle
38	2.3		> 7k	
39			< 200	
40	1.5		> 6k	
41	0			DC not apply more than 0.5V direct.
42	5.7	1.3Vp-p	< 5	 H cycle
43	0			GND
44	3.0		< 200	
45	4.1	0.7Vp-p	> 100k	 H cycle
46	2.6	1.5Vp-p	> 7k	 H cycle
47	2.6	1.5Vp-p	< 5	 H cycle
48	5.0			$V_{CC}4$

Package Outline Unit : mm

48pin QFP(Plastic) 0.7g



QFP-48P-L022

SONY

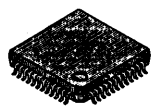
CX20056

Automatic Iris and Automatic White Balance

Description

CX20056 is a bipolar IC which has been developed for Automatic White Balance control, AGC control and automatic iris driving for color camera, and it has functions of signal amplifying, clamping, R/B line sequential signal separation, pedestal setting, window extraction, A.W.B. peak detection and comparison, AGC amplifier controlling, iris driving, low light alarm indication (LED drive), etc.

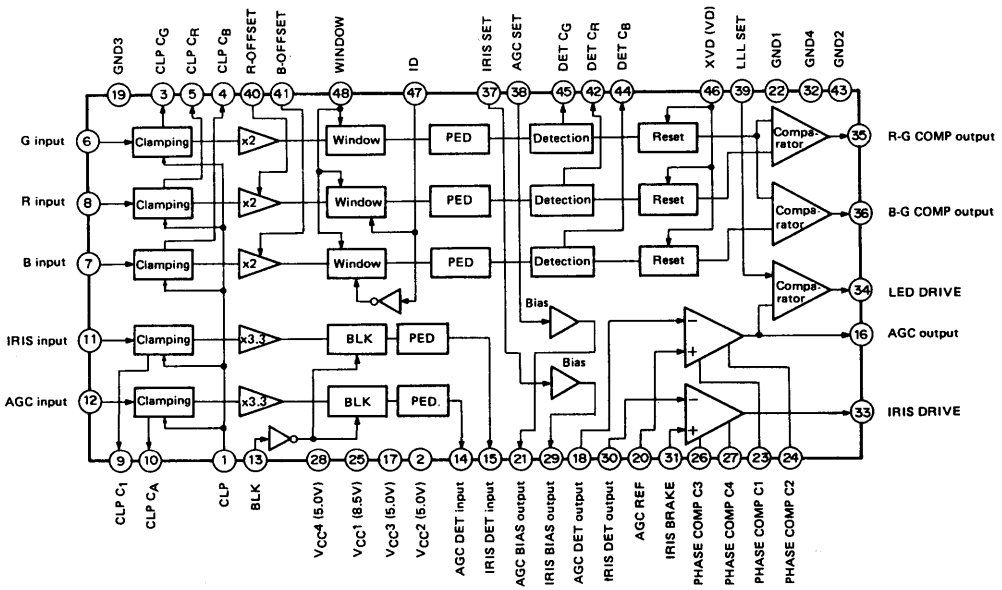
48 pin QFP (Plastic)



Features

- It can be composed as a consistent color camera signal processing system, together with CX20053, CX20054, CX20055, etc.
- Automatic white balance is standardized to the color difference line sequential signal; however, it is respective input pins of R, G and B, and it can available for various kinds of image pick-up systems.
- A comparator with active load is incorporated within it, and therefore high precision white balance can be obtained.
- Time constant and detection system of the AGC and automatic iris can be set arbitrarily with the external circuit.
- Operational amplifier which can drive the iris coil directly is incorporated.
- LED drive output pin for low light alarm indication.

Block Diagram



E89663 – ST

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	$V_{CC}1$ to 4	10	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	833	mW

Input Pin Maximum Voltage

No.	Voltage(V)	No.	Voltage(V)	No.	Voltage(V)
1	≦$V_{CC}2$ to 4	18	≦$V_{CC}1$	40	≦$V_{CC}2$ to 4
6	≦$V_{CC}2$ to 4	20	≦$V_{CC}1$	41	≦$V_{CC}2$ to 4
7	≦$V_{CC}2$ to 4	30	≦$V_{CC}1$	46	≦$V_{CC}2$ to 4
8	≦$V_{CC}2$ to 4	31	≦$V_{CC}1$	47	≦$V_{CC}2$ to 4
11	≦$V_{CC}2$ to 4	37	≦$V_{CC}2$ to 4	48	≦$V_{CC}2$ to 4
12	≦$V_{CC}2$ to 4	38	≦$V_{CC}2$ to 4		
13	≦$V_{CC}2$ to 4	39	≦$V_{CC}2$ to 4		

Recommended Operating Conditions

• Supply voltage	$V_{CC}1$	8.5 ± 0.2	V
	$V_{CC}2$ to 4	5.0 ± 0.15	V

Maximum Output Current

No.	Current(mA)
16	10
33	100*
34	20

* Care should be exercised so that P_D does not exceed the maximum rating.

Recommended Input Pulse level

No.	Input level
1	CMOS level
13	CMOS level
46	CMOS level
47	CMOS level
48	CMOS level

CMOS level

	Min.	Max.	Unit
V_H	4.0	5.0	V
V_L	0	0.4	V

Pin Description

No.	Symbol	I/O	Description
1	CLP	I	Pulse input which clamps the input signals (white balance, AGC and IRIS)
2	$V_{CC}2$		A partial power source (5V) of the white balance section.
3	CLP C_G	O	Output which has been clamped by G signal.
4	CLP C_B	O	Output which has been clamped by B signal.
5	CLP C_R	O	Output which has been clamped by R signal.
6	G input	I	Input of G signal from CX20053.
7	B input	I	Input of R/B signal from CX20053 which corresponds to B signal.
8	R input	I	Input of R/B signal from CX20053 which corresponds to B signal.
9	CLP C_I	O	Output which has been clamped by IRIS signal.
10	CLP C_A	O	Output which has been clamped by AGC signal.
11	IRIS input	I	Input of IRIS signal from CX20053.
12	AGC input	I	Input of AGC signal from CX20053.
13	BLK	I	Blanking pulse input
14	AGC DET input	O	Output of the signal to which pedestal is attached after it has been input to pin ⑫ and clamped. An externally attached detecting circuit is connected to this pin.
15	IRIS DET input	O	Output of the signal to which pedestal is attached after it has been input to pin ⑪ . An externally attached detecting circuit is connected to this pin.
16	AGC output	O	Output of the AGC operational amplifier, and it controls the AGC gain of CX20053.
17	$V_{CC}3$		Power source (5V) of the AGC and IRIS sections.
18	AGC DET output	I	Negative input of the AGC operation amplifier.
19	GND3		Ground of the AGC and IRIS sections.
20	AGC REF	I	Positive input of the AGC operation amplifier.
21	AGC BIAS output	O	Reference voltage output to be fed to pin ⑳ . It is possible to be controlled by pin ㊳ .
22	GND1		Ground of the operational amplifier and low light comparator.
23	PHASE COMP C1	I	AGC operation amplifier for phase correction.
24	PHASE COMP C2	I	AGC operation amplifier for phase correction.
25	$V_{CC}1$		Power source (8.5V) of the operational amplifier and comparator sections.
26	PHASE COMP C3	I	IRIS operational amplifier for phase correction.
27	PHASE COMP C4	I	IRIS operation amplifier for phase correction.
28	$V_{CC}4$		Power source (5V) of a portion of the white balance system and the bias circuit section.
29	IRIS BIAS output	O	Reference voltage output to be input to pin ㉛ . It is possible to be controlled by pin ㊲ .
30	IRIS DET output	I	Negative input of the IRIS operational amplifier.
31	IRIS BRAKE	I	Positive input of the IRIS operational amplifier.
32	GND4		Ground of a portion of the white balance system and the bias circuit.
33	IRIS DRIVE	O	Output of the IRIS operational amplifier.
34	LED DRIVE	O	Output to drive the externally attached LED by comparing the output of the AGC operational amplifier with the voltage of pin ㊴ .

No.	Symbol	I/O	Description
35	R-G COMP output	O	Output comparing the level of R signal with that of G signal. Input into white balance IC (CX-7938).
36	B-G COMP output	O	Output comparing the level of B signal with that of G signal. Input into white balance IC (CX-7938).
37	IRIS SET	I	Input which adjusts the output voltage of pin ㉙ .
38	AGC SET	I	Input which adjusts the output voltage of pin ㉑ .
39	LLL SET	I	Input which determines the voltage to light the LED.
40	R OFFSET	I	Input in order to match R signal with G signal.
41	B OFFSET	I	Input in order to match B signal with G signal.
42	DET C_R	O	Output of peak detect voltage of R signal.
43	GND2		Ground a portion of the white balance section.
44	DET C_B	O	Output of peak detect voltage of B signal.
45	DET C_G	O	Output of peak detect voltage of G signal.
46	XVD	I	Input of pulse to reset peak detection circuit.
47	ID	I	Input of pulse to separate the R/B line sequential signal.
48	WINDOW	I	Input of pulse which extracts 1/9 portion (1/3 in H-direction and 1/3 in V-direction) of signal from the entire image.

Electrical Characteristics

Ta=25°C, Vcc1=8.5V, Vcc2=Vcc3=Vcc4=5.0V

Item	Symbol	Test point	SW conditions													Bias conditions									Condition	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	E1	E2	E3	E4	E5	E6	E7	E8	E9					
Circuit current 1	Icc1	A1	a	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p. Pin ㉞ is opened, and pin ⑯ and pin ㉝ are measured without load.	11.7	19.0	27.5	mA
Circuit current 2	Icc2	A2	a	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p. Pin ㉞ is opened, and pin ⑯ and pin ㉝ are measured without load.	2.16	3.35	4.73	mA
White balance clamping pedestal	CLPG	V3	b	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.25	2.60	2.97	V
White balance clamping pedestal	CLPB	V4	b	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.25	2.60	2.97	V
White balance clamping pedestal	CLPR	V5	b	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.25	2.60	2.97	V
Window potential	WPG	V45	b	a	a	a	a	a	a	b	b	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		1.44	1.68	1.93	V
Window potential	WPB	V44	b	a	a	a	a	a	a	b	b	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		1.44	1.68	1.93	V
Window potential	WPR	V42	b	a	a	a	a	a	a	b	b	c	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		1.44	1.68	1.93	V
Color separation	IDPB	V44	b	a	a	a	a	a	a	b	b	c	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		1.44	1.68	1.93	V
Color separation	IDPR	V42	b	a	a	a	a	a	a	a	b	b	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		1.44	1.68	1.93	V
Comparator sensitivity 1	R-GL	V35	a	a	a	a	a	a	a	c	b	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.71V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p.	36	90	154	mV
Comparator sensitivity 1	R-GH	V35	a	a	a	a	a	a	a	c	b	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.69V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p.	3.6	4.5	5.5	V
Comparator sensitivity 2	B-GL	V36	a	a	a	a	a	a	a	c	b	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.69V	2.71V	2.70V	Amplitude of SG1 is 250mVp-p.	36	90	154	mV
Comparator sensitivity 2	B-GH	V36	a	a	a	a	a	a	a	c	b	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.69V	2.69V	2.70V	Amplitude of SG1 is 250mVp-p.	3.6	4.5	5.5	V
R offset	RL	V35	a	a	a	a	a	a	a	a	b	c	c	a	a	4.2V	4.2V	2.5V	2.5V	2.0V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p.	3.6	4.5	5.5	V
R offset	RH	V35	a	a	a	a	a	a	a	a	a	b	c	c	a	4.2V	4.2V	2.5V	2.5V	3.0V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p.	36	90	154	mV
B offset	BL	V36	a	a	a	a	a	a	a	a	b	b	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.0V	2.70V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p.	3.6	4.5	5.5	V
B offset	BH	V36	a	a	a	a	a	a	a	a	b	b	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	3.0V	2.70V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p.	36	90	154	mV
White balance gain	GG	V45	a	a	a	a	a	a	a	b	b	b	c	a	a	4.2V	4.2V	2.5	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 250mVp-p.	378	455	539	mVp-p
White balance gain *ratio*	GB/GG	V44/V45	a	a	a	a	a	a	a	b	b	b	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Ratio of PP values between pin ㊹ and pin ⑮ .	0.88	1.00	1.12	
White balance gain ratio	GR/GG	V42/V45	a	a	a	a	a	a	a	b	b	c	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Ratio of PP value between pin ㊷ and pin ⑮ .	0.88	1.00	1.12	
White balance dynamic range	DYNG	V45	a	a	a	a	a	a	a	a	b	b	b	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 800mVp-p. Measure PP value of pin ㊺ .	0.86	1.05	1.27	Vp-p
White balance dynamic range	DYNB	V44	a	a	a	a	a	a	a	a	b	b	b	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 800mVp-p. Measure PP value of pin ㊹ .	0.86	1.05	1.27	Vp-p
White balance dynamic range	DYNR	V42	a	a	a	a	a	a	a	a	b	b	c	c	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 800mVp-p. Measure PP value of pin ㊷ .	0.86	1.05	1.27	Vp-p

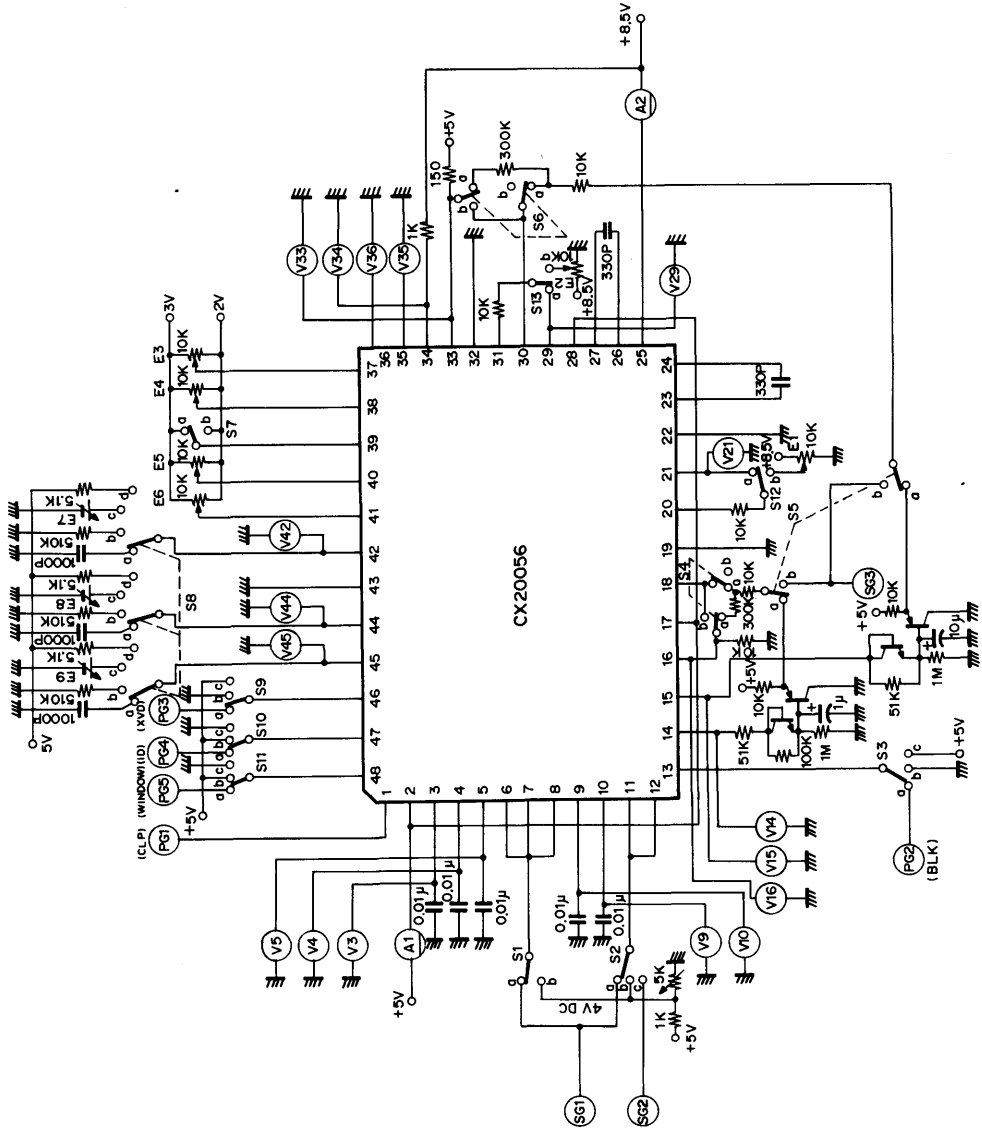
Ta=25°C, $V_{CC}1$=8.5V, $V_{CC}2$=$V_{CC}3$=$V_{CC}4$=5.0V

Item	Symbol	Test point	SW conditions													Bias conditions									Condition	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	E1	E2	E3	E4	E5	E6	E7	E8	E9					
V reset	XVDG	V45	a	a	a	a	a	a	a	d	c	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		3.7	4.3	5.0	V
V reset	XVDB	V44	a	a	a	a	a	a	a	d	c	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		3.7	4.3	5.0	V
V reset	XVDR	V42	a	a	a	a	a	a	a	d	c	b	b	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		3.7	4.3	5.0	V
AGC clamping potential	CLPA	V10	a	b	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.25	2.60	2.97	V
IRIS clamping potential	CLPI	V9	a	b	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.25	2.60	2.97	V
AGC blanking potential	BLKA	V14	a	b	b	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		1.98	2.25	2.53	V
IRIS blanking potential	BLKI	V15	a	b	b	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		1.98	2.25	2.53	V
AGC pedestal potential	PEDA	V14	a	b	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.36	2.72	3.10	V
IRIS pedestal potential	PEDI	V15	a	b	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.36	2.72	3.10	V
AGC signal amplitude	GA	V14	a	a	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 300mVp-p.	765	940	1155	mVp-p
IRIS signal amplitude	GI	V15	a	a	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 300mVp-p.	765	940	1155	mVp-p
Entire amplitudes of AGC signal	AGA	V14	a	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 300mVp-p.	1.17	1.43	1.71	Vp-p
Entire amplitudes of IRIS signal	AGI	V15	a	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 300mVp-p.	1.17	1.43	1.71	Vp-p
AGC dynamic range	DYNA	V14	a	a	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 300mVp-p. Measure PP value of pin ⑭.	1.22	1.45	1.71	Vp-p
IRIS dynamic range	DYNI	V15	a	a	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Amplitude of SG1 is 700mVp-p. Measure PP value of pin ⑮.	1.22	1.45	1.71	Vp-p
AGC frequency characteristics	FA	V14	a	c	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Based on the output amplitude when frequency of SG2 is 1MHz, measure input frequency in which the output amplitude becomes −3dB when the frequency is varied.	6.3	9.3		MHz
IRIS frequency characteristics	FI	V15	a	c	c	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		6.3	9.3		MHz

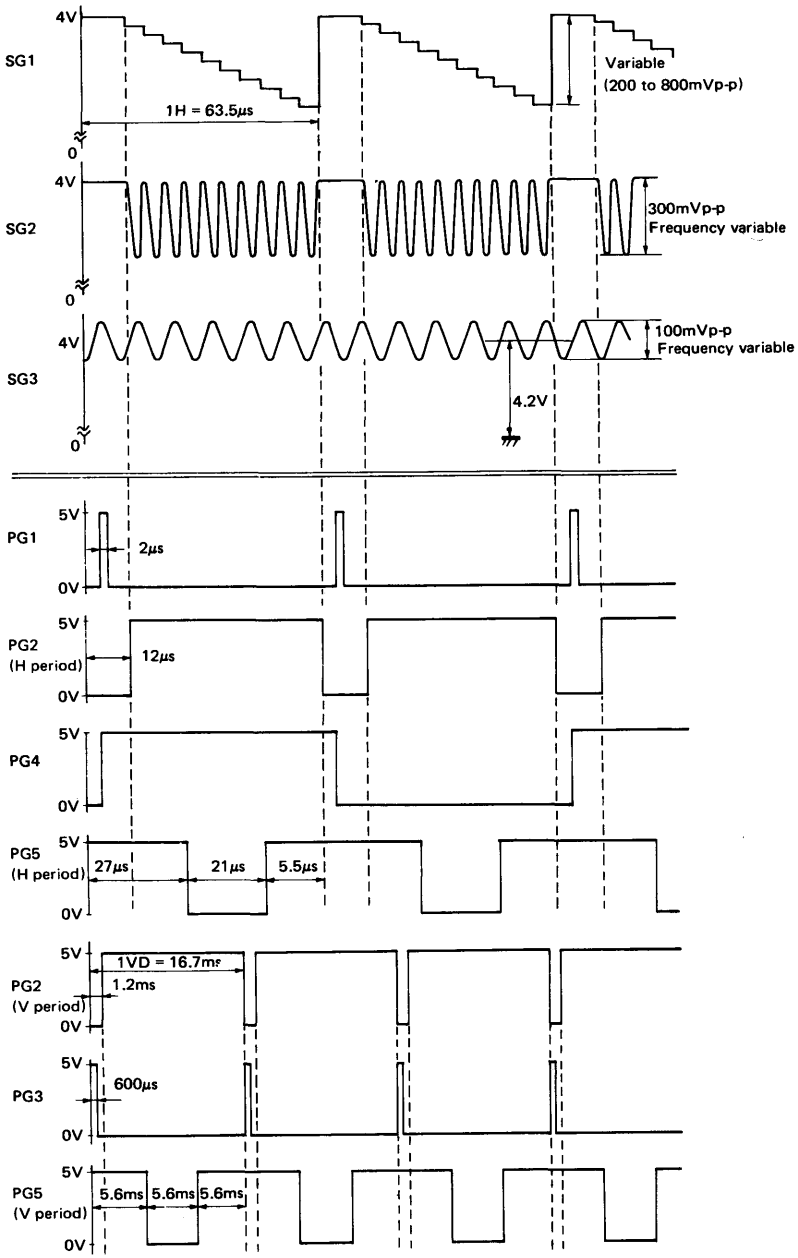
Ta=25°C, $V_{CC}1$=8.5V, $V_{CC}2$=$V_{CC}3$=$V_{CC}4$=5.0V

Item	Symbol	Test point	SW conditions													Bias conditions									Condition	Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	E1	E2	E3	E4	E5	E6	E7	E8	E9					
AGC operational amplifier amplifying	AMPA	V16	a	a	a	a	b	a	a	a	a	a	a	b	b	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Measure the PP value when amplitude of SG3 is 100mVp-p and output frequency is 1kHz.	2.57	3.00	3.47	Vp-p
IRIS operational amplifier amplifying characteristics	AMPI	V33	a	a	a	a	b	a	a	a	a	a	a	b	b	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Measure the PP value when amplitude of SG3 is 100mVp-p and output frequency is 1kHz.	2.57	3.00	3.47	Vp-p
AGC operational amplifier offset	OFFA	V16	a	a	a	a	b	a	a	a	a	a	a	b	b	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Set the amplitude of SG3 to 0mVp-p. Subtract 4.2V from the measured value.	−352	70	605	mV
IRIS operational amplifier offset	OFFI	V33	a	a	a	a	b	a	a	a	a	a	a	b	b	4.2V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V	Set the amplitude of SG3 to 0mVp-p. Subtract 4.2V from the measured value.	−242	130	858	mV
AGC operational amplifier follower characteristics	FOL3A	V16	a	a	a	b	b	a	a	a	a	a	a	b	b	3.0V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.67	3.00	3.36	V
AGC operational amplifier follower characteristics	FOL7A	V16	a	a	a	b	b	a	a	a	a	a	a	b	b	7.0V	4.2V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		6.26	7.00	7.76	V
IRIS operational amplifier follower characteristics	FOL3I	V33	a	a	a	a	b	b	a	a	a	a	a	b	b	4.2V	3.0V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		2.66	3.00	3.36	V
IRIS operational amplifier follower characteristics	FOL7I	V33	a	a	a	a	b	b	a	a	a	a	a	b	b	4.2V	7.0V	2.5V	2.5V	2.5V	2.5V	2.70V	2.70V	2.70V		6.26	7.00	7.76	V
Bias circuit 1	BIAS1	V21	a	a	a	a	a	a	a	a	a	a	a	b	b	4.2V	4.2V	2.5V	2.0V	2.5V	2.5V	2.70V	2.70V	2.70V		0.9	1.25	1.65	V
Bias circuit 2	BIASA2	V21	a	a	a	a	a	a	a	a	a	a	a	b	b	4.2V	4.2V	2.5V	3.0V	2.5V	2.5V	2.70V	2.70V	2.70V		3.6	4.25	4.95	V
Bias circuit 2	BIASI1	V29	a	a	a	a	a	a	a	a	a	a	a	b	b	4.2V	4.2V	2.0V	3.0V	2.5V	2.5V	2.70V	2.70V	2.70V		0.9	1.25	1.65	V
Bias circuit 2	BIASI2	V29	a	a	a	a	a	a	a	a	a	a	a	b	b	4.2V	4.2V	3.0V	3.0V	2.5V	2.5V	2.70V	2.70V	2.70V		3.6	4.25	4.95	V
Low light indication	LLL	V34	a	a	a	a	a	a	a	a	a	a	a	a	a	4.2V	4.2V	3.0V	Adj.	2.5V	2.5V	2.70V	2.70V	2.70V	Set the amplitude of SG1 to 300mVp-p, and adjust E4 so that the output of pin ⑯ becomes 2.5V. Then perform measuring by switching S7.	7.56	8.45	9.35	V
Low light indication	LLH	V34	a	a	a	a	a	a	b	a	a	a	a	a	a	4.2V	4.2V	3.0V	Adj.	2.5V	2.5V	2.70V	2.70V	2.70V		0.32	0.43	0.55	V

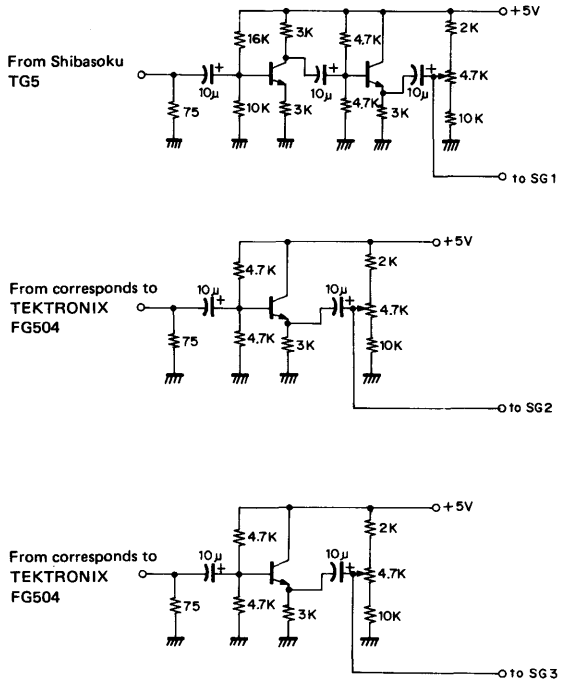
Electrical Characteristics Test Circuit

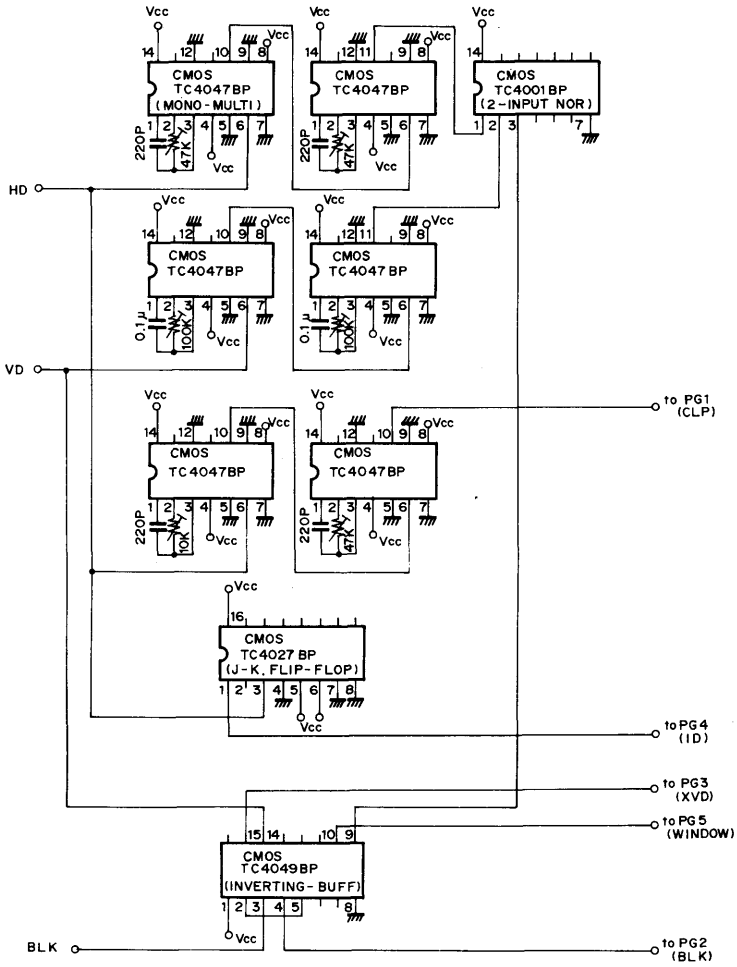


Input Waveform and Input Pulse



Electrical Characteristics Test Circuit (Part 2)





SONY®

CX20056

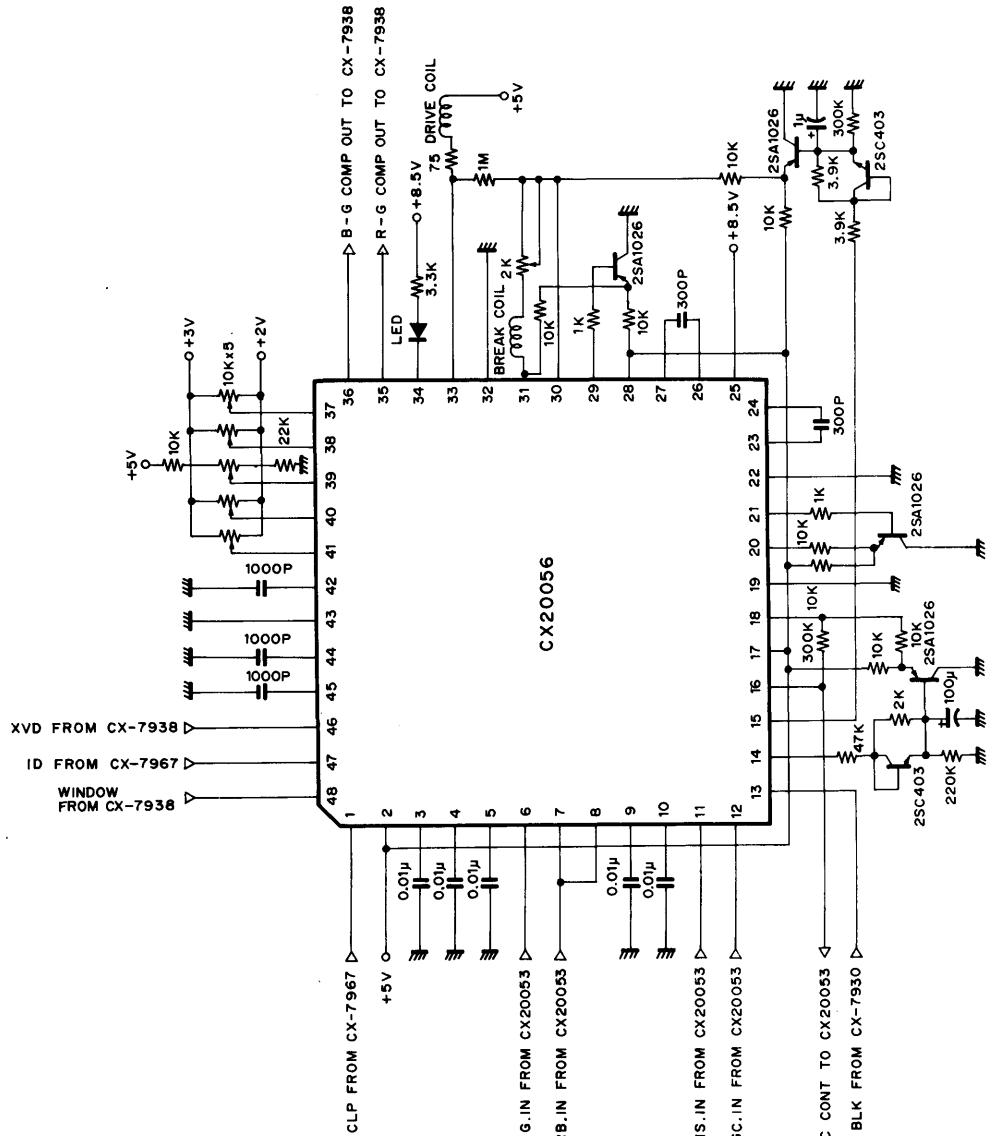
Reference Pin Voltage (DC)

See Test Circuit
During non-signal
Ta=25°C, $V_{CC}1$=8.5V, $V_{CC}2$ to 4=5.0V

No.	Voltage(V)	No.	Voltage(V)	No.	Voltage(V)
1	(5.0 CLP)*2	17	(5.0 Vcc3)*1	33	3.00
2	(5.0 Vcc2)*1	18	2.83	34	8.49
3	2.65	19	(D GND)*1	35	4.99
4	2.65	20	2.79	36	4.99
5	2.65	21	2.80	37	2.64*4
6	(4.00)*3	22	(O GND)*1	38	2.51*5
7	(4.00)*3	23	3.26	39	(3.00)*1
8	(4.00)*3	24	1.63	40	(2.50)*1
9	2.65	25	(8.5 Vcc1)*1	41	(2.50)*1
10	2.65	26	3.45	42	1.92
11	(4.00)*3	27	3.86	43	(O GND)*1
12	(4.00)*3	28	(5.0 Vcc4)*1	44	1.92
13	(5.0 BLK)*2	29	3.22	45	1.92
14	2.74	30	3.26	46	(O XVD)*2
15	2.74	31	3.21	47	(5.0 ID)*2
16	2.00	32	(O GND)*1	48	(5.0 WINDOW)*2

*1) The pin voltage in parentheses is applied externally.
*2) The pin voltage in parentheses is an input pin; however, DC is applied to it.
*3) The pin voltage in parentheses is in non-signal state to which DC is applied.
*4) The voltage when the output voltage of pin 33 is so adjusted that it becomes 3(V).
*5) The voltage when the output voltage of pin 16 is so adjusted that it becomes 2(V).

Application Circuit



Standard Operation Characteristics (Ta=25°C), and Temperature Characteristics

	SW conditions													Bias conditions								
	1	2	3	4	5	6	7	8	9	10	11	12	13	E1	E2	E3	E4	E5	E6	E7	E8	E9
AGC voltage amplifying operational amplifier output characteristics	b	b	a	a	a	a	a	a	a	a	a	a	a	4.2	4.2	2.5	—	2.5	2.5	2.7	2.7	2.7
	Measure the voltage of the AGC output voltage pin ⑯ when the E4 (AGC SET) voltage is varied from 2 to 3V. (Fig. 1)																					
Operational amplifier output Characteristics for IRIS driving	b	b	a	a	a	a	a	a	a	a	a	a	a	4.2	4.2	—	2.5	2.5	2.5	2.7	2.7	2.7
	Measure the voltage of IRIS output pin ㉝ when the E3 (IRIS SET) voltage is varied from 2 to 3V. (Fig. 2)																					
R.B offset voltage vs. G DET-R/B DET	a	b	a	a	a	a	a	a	a	a	a	a	a	4.2	4.2	2.5	2.5	—	—	2.7	2.7	2.7
	Input SG1=250mV to pins ⑥, ⑧ and ⑦, and measure the difference between the output of pins ㊺ and ㊹ and that of pin ㊷ against the voltage of E5 and E6. (Fig. 3)																					
G, R and B inputs vs. Detection output characteristics	a	b	a	a	a	a	a	a	a	a	a	a	a	4.2	4.2	2.5	2.5	2.5	2.5	2.7	2.7	2.7
	Measure the detecting output of pins ㊺, ㊷ and ㊹ when the input of pins ⑥, ⑧ and ⑦ is varied from 0mV to 500mV. (Fig. 4)																					
AGC IRIS setting voltage vs. Setting output voltage	a	a	a	a	a	a	a	a	a	a	a	b	b	4.2	4.2	—	—	2.5	2.5	2.7	2.7	2.7
	Measure the output voltage of pins ㉑ and ㉙ when the E3 and E4 voltages are varied from 0 to 5V. (Fig. 5)																					
(G DET-R/B DET) voltage vs. Power supply fluctuation	a	b	a	a	a	a	a	a	a	a	a	a	a	4.2	4.2	2.5	2.5	—	—	2.7	2.7	2.7
	The change due to the power supply fluctuation when 250mV is input to pins ⑥, ⑧ and ⑦, and the E5 and E6 are adjusted so that they become (G DET-R/B DET) = 0mV. (Fig. 6)																					
AGC (IRIS) DET peak voltage	b	a	a	a	a	a	a	a	a	a	a	a	a	4.2	4.2	2.5	2.5	2.5	2.5	2.7	2.7	2.7
	Measure the output peak voltage of pins ⑭ and ⑮ by setting SG1=300mVp-p. (Fig. 7)																					
(R/B DET-G DET) temperature characteristics	a	b	a	a	a	a	a	a	a	a	a	a	a	4.2	4.2	2.5	2.5	—	—	2.7	2.7	2.7
	Temperature characteristics after ajustment has been performed by setting to SG1=250mV, so that the potential difference between R/B DET and G DET becomes 0 at Ta=25°C. (Fig. 8)																					

AGC OUT vs. AGC SET

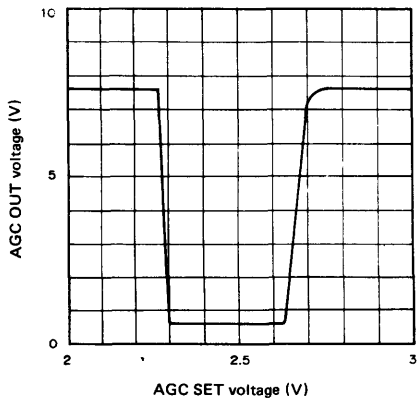


Fig. 1

IRIS OUT vs. IRIS SET

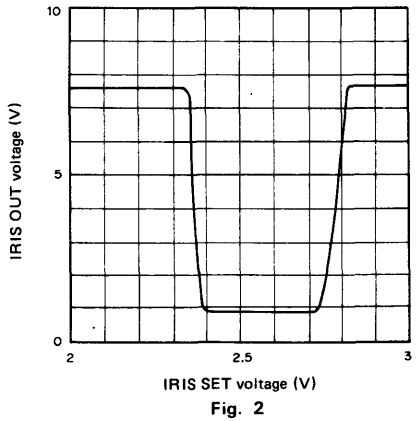


Fig. 2

G DET - $\frac{R}{B}$ DET vs. $\frac{R}{B}$ OFF SET

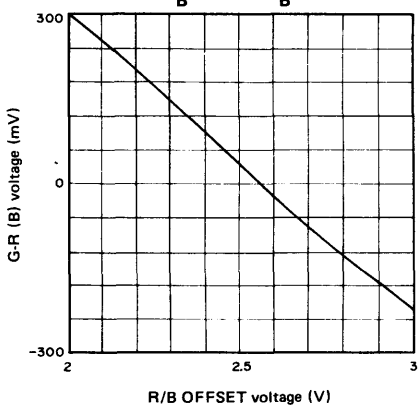


Fig. 3

DET peak voltage vs. G/R/B IN

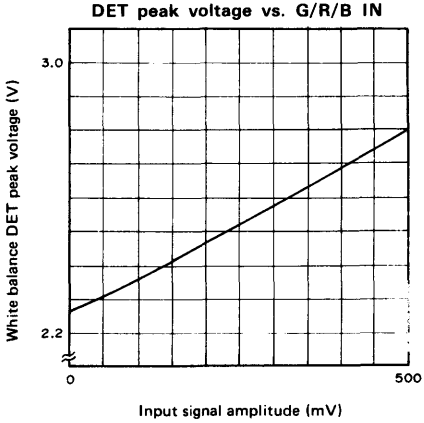


Fig. 4

$\frac{AGC}{IRIS}$ BIAS OUT vs. $\frac{AGC}{IRIS}$ SET

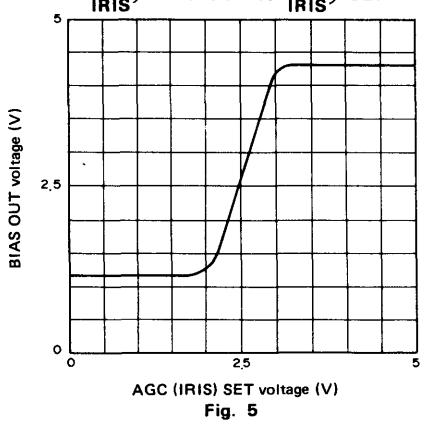


Fig. 5

(DET C_G) - (DET $C_{R(B)}$) vs. Supply voltage

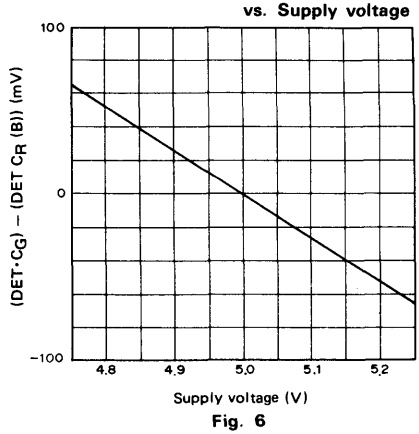


Fig. 6

AGC (IRIS) DET IN peak voltage vs. Supply voltage

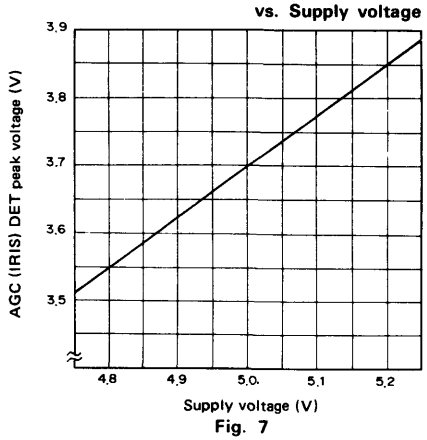


Fig. 7

DET (R/B)-DET G vs. Ambient temperature

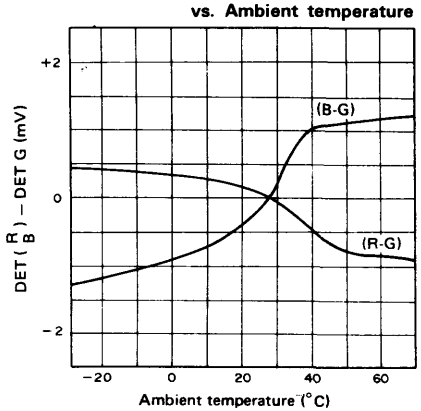


Fig. 8

Iris Drive characteristics 1

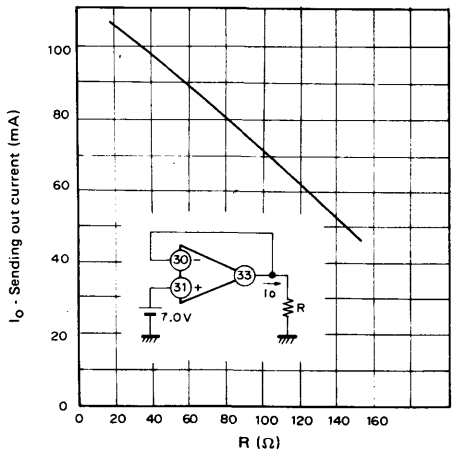


Fig. 9

Iris Drive characteristics 2

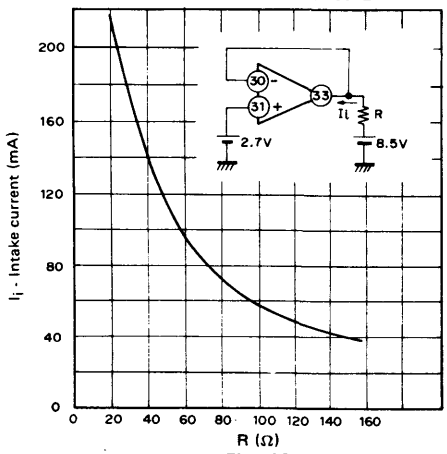


Fig. 10

Derating curve

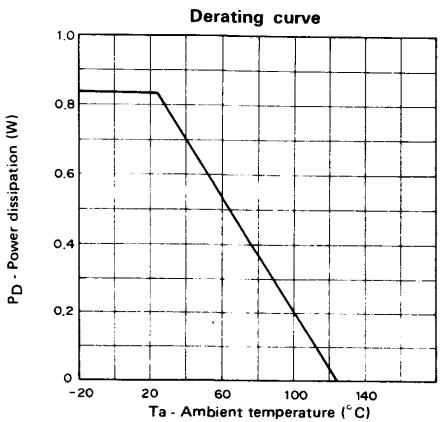
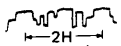
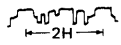
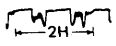
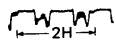
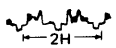
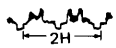
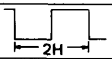


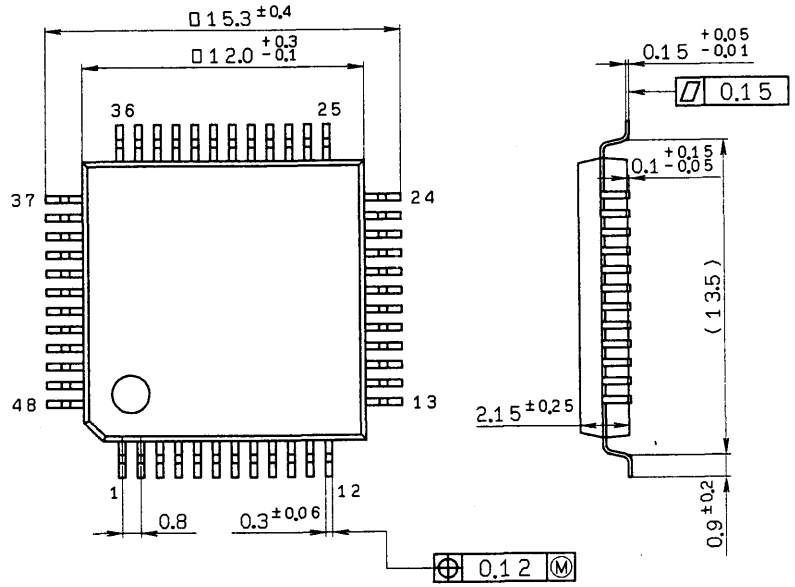
Fig. 11

No.	DC [V]	AC [V]	Impedance [Ω]	Remarks
1	0.1	4.0 Vp-p	>100k	 H period
2	5.0			Vcc2
3	2.9		<50	
4	3.0		<50	
5	2.9		<50	
6	4.2	0.32 Vp-p	>100k	 H period
7	4.2	0.38 Vp-p	>100k	 2H
8	4.2	0.38 Vp-p	>100k	 2H
9	2.6		<50	
10	2.7		<50	
11	4.0	0.16 Vp-p	>100k	 2H
12	4.0	0.36 Vp-p	>100k	 2H
13	3.0	3.7 Vp-p	>10k	 H period
14	2.8	1.8 Vp-p	<200	 2H
15	2.7	1.0 Vp-p	<200	 2H
16	7.4		<10	
17	5.0			Vcc3
18	3.4		>100k	
19	0			GND
20	1.7		>100k	
21	1.2		<200	
22	0			GND
23	3.0		>100k	Indicates AC impedance
24	8.1		>100k	Indicates AC impedance
25	8.5			Vcc1
26	3.6		>100k	Indicates AC impedance
27	4.3		>100k	Indicates AC impedance
28	5.0			Vcc4
29	2.5		<200	
30	3.1		>100k	
31	3.0		>100k	
32	0			GND

No.	DC [V]	AC [V]	Impedance [Ω]	Remarks
33	4.8		<10	
34	0.1			Open collector
35	0.1		>7k	
36	0.1		>7k	
37	2.4		>100k	
38	2.5		>100k	
39	5.2		>100k	
40	2.5		>100k	
41	2.5		>100k	
42	1.7		>1k	
43	0			
44	1.7		>1k	
45	1.7		>3k	
46	0.1	4.8 Vp-p	>30k	 H period
47	2.0	4.8 Vp-p	>100k	
48	4.7		>6k	

Package Outline Unit : mm

CX20056 48 pin QFP (Plastic) 0.7g



QFP-48P-L022

SONY®

CX20151

Matrix for Color Camera

Description

CX20151 is a bipolar IC which has been developed to obtain Y_H and Y_L-Y_H luminance signal outputs and R-Y and B-Y chroma signal outputs by inputting G signal and R/B signals, and connecting to 1H DL, for the G vertical striped R/B line sequential type color camera. Composed of circuits such as clamp, sampling hold for waveform shaping, DC bias adjustment of 1H DL input, 1H DL gain adjustment, multiplexer, color-difference (R-Y and B-Y) signal forming, color-difference (R-Y and B-Y) signal mixing, luminance low band width (-Y_L) signal forming, luminance high band width (Y_H) signal forming, luminance (Y_L-Y_H) signal forming, V aperture control, switchover sample hold, color-difference signal blanking, ECL conversion, etc.

48 pin QFP (Plastic)

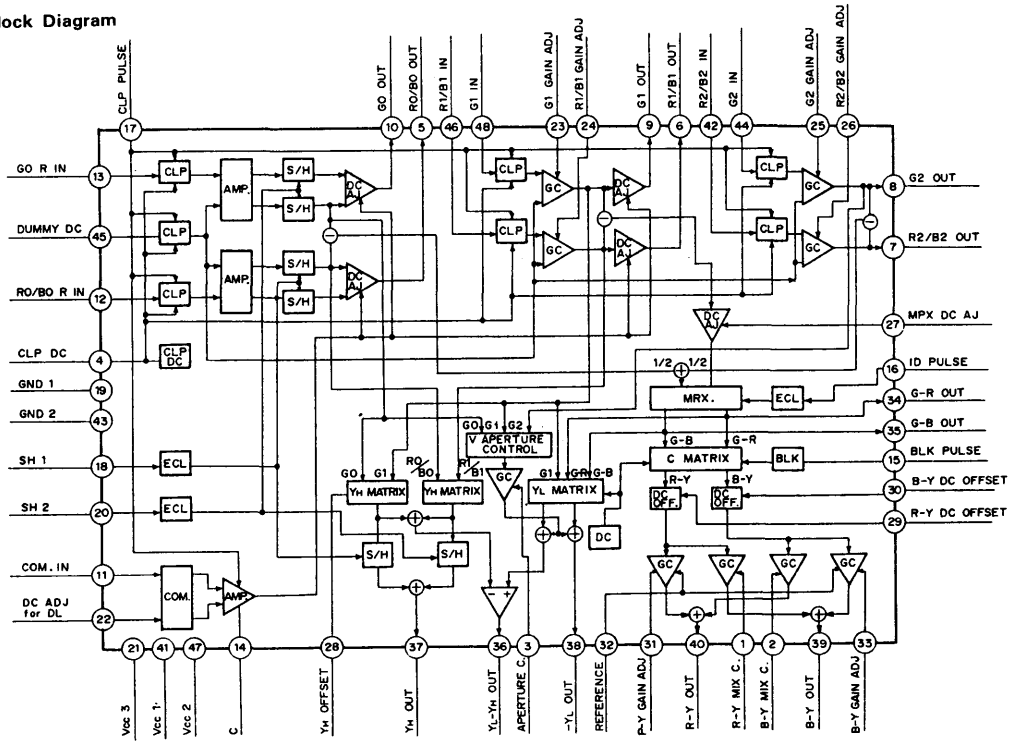
Features

Together with CX20053, CX20055 and CX20056, it is possible to compose a consistent color camera signal processing system.

Structure

Bipolar silicon monolithic IC

Block Diagram



E89664 – ST

Absolute Maximum Ratings (Ta=25°C)

- Power supply voltage $V_{CC}1$ to 3 — 17 V
- Operating temperature Topr — −20 to +75 °C
- Storage temperature Tstg — −55 to +150 °C
- Allowable power dissipation P_D — 850 mW

Recommended Pulse Input Level

Pin No.	Input level
15	CMOS level
16	CMOS level
17	CMOS level
18	CMOS level
20	CMOS level

CMOS Level

	Min.	Max.	Unit
V_H	4.0	5.0	V
V_L	0	0.4	V

Input Pin Maximum Voltage

Pin No.	Voltage(V)	Pin No.	Voltage(V)	Pin No.	Voltage(V)
1	≦Vcc1	24	≦Vcc2,3	32	≦Vcc1
2	≦Vcc1	25	≦Vcc2,3	33	≦Vcc1
3	≦Vcc2,3	26	≦Vcc2,3	42	≦Vcc2,3
11	≦Vcc1	27	≦Vcc2,3	44	≦Vcc2,3
12	≦Vcc2,3	28	≦Vcc1	45	≦Vcc2,3
13	≦Vcc2,3	29	≦Vcc2,3	46	≦Vcc2,3
22	≦Vcc1	30	≦Vcc2,3	48	≦Vcc2,3
23	≦Vcc2,3	31	≦Vcc1		

Recommended Operating Conditions (Ta=25°C)

- Vcc1 8.5 ± 0.4 V
- Vcc2 5.0 ± 0.2 V
- Vcc3 5.0 ± 0.2 V

Pin Configuration

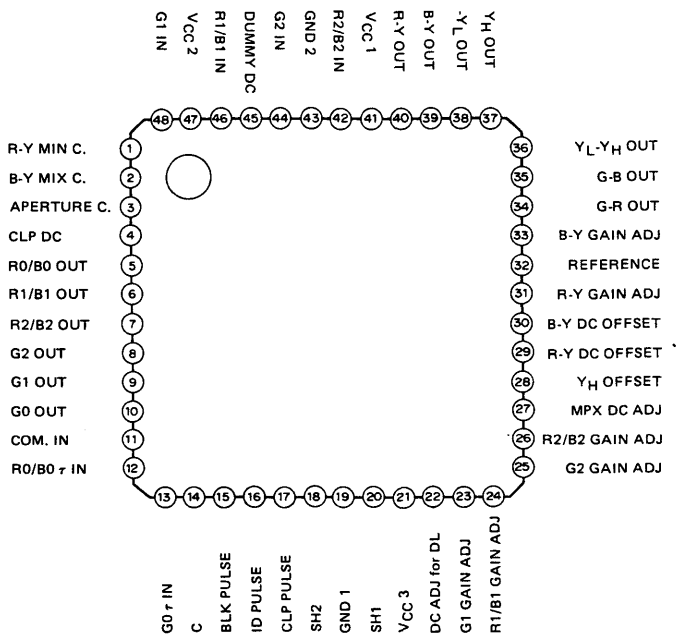


Fig. 1

Pin Description

No.	Symbol	I/O	Description
1	R-Y MIX C.	I	Pin to mix R-Y signal to B-Y signal output of pin ㊴ by applying DC potential (2.0 to 3.0V). Positive/Negative adjustment; 2.5V center. In case of open state, biased approximately 1.8V internally and mixing cannot be performed.
2	B-Y MIX C.	I	Pin to mix B-Y signal to R-Y signal output of pin ㊵ by applying DC potential (2.0 to 3.0V). Positive/Negative adjustment; 2.5V center. In case of open state, biased approximately 1.8V internally and mixing cannot be performed.
3	APERTURE C.	I	Adjust V direction aperture level which is applied to $-Y_L$ signal output of pin ㊳ by applying DC potential (2.0 to 3.0V). Aperture is turned off at 2.0V.
4	CLP DC	O	Output DC of internal clamping circuit. Connect to ground through a capacitor.
5	R0/B0 OUT	O	Signal input from pin ⑫ is sampled by sample and hold pulse of pin ⑱, and is output after DC adjusted by pin ㉒.
6	R1/B1 OUT	O	Signal input from pin ㊻ is gain controlled by pin ㉔, and is output after DC adjusted by pin ㉒.
7	R2/B2 OUT	O	Signal input from pin ㊷ is gain controlled by pin ㉖ and then is output.
8	G2 OUT	O	Signal input from pin ㊹ is gain controlled by pin ㉕ and then is output.
9	G1 OUT	O	Signal input from pin ㊽ is gain controlled by pin ㉓ and is output after DC adjusted by pin ㉒.
10	G0 OUT	O	Signal input from pin ⑬ is sampled by sample and hold pulse of pin ⑳, and is output after DC adjusted by pin ㉒.
11	COM IN	I	Signal input pin to compare with DC which has been input to pin ㉒. ex. When G0 (pin ⑩) is connected, G0 output DC potential will become equal to input DC of pin ㉒.
12	R0/B0 γ IN	I	Input R/B line sequential signal of 0.35 Vp-p through a clamping capacitor.
13	G0 γ IN	I	Input G signal of 0.35 Vp-p through a clamping capacitor.
14	C		Capacitor pin for holding comparator output to compare pin ⑪ input with DC potential of pin ㉒ input. Normally, a capacitor is inserted between it and the power supply.
15	BLK pulse	I	Input BLK pulse when application of color-difference blanking is desired. When unnecessary, connect to 5V.
16	ID pulse	I	Input pulse: L; R signal H; B signal.
17	CLP pulse	I	CLP pulse input to clamp the input signals of pins ⑫, ⑬, ㊷, ㊹, ㊺, ㊻ and ㊽. The comparison between pin ⑪ input and pin ㉒ input is also performed with this pulse.
18	SH1	I	Input sample and hold pulse for sampling of input signal of pin ⑫ and also for switchover sample and hold.
19	GND1		Ground

No.	Symbol	I/O	Description
20	SH2	I	Input sample and hold pulse for input signal of pin ⑬ for sampling use and also for switchover of sample and hold use.
21	$V_{CC}3$		5.0V power supply for ECL conversion and also for pulse section input.
22	DC ADJ for DL	I	Adjust the DC of output signals of pins ⑤, ⑥, ⑨ and ⑩ by applying DC potential (3.0 to 6.0V). (Output by clamping the potential applied to this pin.)
23	G1 GAIN ADJ	I	Adjust the gain of pin ⑨ output signal by applying DC potential (2.0 to 3.0V).
24	R1/B1 GAIN ADJ	I	Adjust the gain of pin ⑥ output signal by applying DC potential (2.0 to 3.0V).
25	G2 GAIN ADJ	I	Adjust the gain of pin ⑧ output signal by applying DC potential (2.0 to 3.0V).
26	R2/B2 GAIN ADJ	I	Adjust the gain of pin ⑦ output signal by applying DC potential (2.0 to 3.0V).
27	MPX DC ADJ	I	Eliminate the DC offset at the multiplexer circuit section by applying DC potential (2.0 to 3.0V).
28	Y_H OFFSET	I	Eliminate the DC offset of Y_H switchover sample and hold circuit section by applying DC potential (4.0 to 5.0V). Normally, it is permissible in the open state (biased internally).
29	R-Y DC OFFSET	I	Eliminate the DC offset of R-Y signal at BLK term by applying DC potential (2.0 to 3.0V). In case of NO BLK, it is permissible in the open state (biased internally).
30	B-Y DC	I	Eliminate the DC offset of B-Y signal at BLK term by applying DC potential (2.0 to 3.0V). In case of NO BLK, it is permissible in the open state (biased internally).
31	R-Y GAIN ADJ	I	Adjust the gain of R-Y signal output of pin ㊵ by applying DC potential (2.0 to 3.0V).
32	REFERENCE	I	When fade-in and fade-out are desired of the chroma (R-Y and B-Y) signal, input fader signal. If fade-in and fade-out do not function, it is permissible in the open state (biased internally). Note) When performing fading, R-Y and B-Y signals mixed with pin ① and pin ②, then do not perform fade-in and fade-out operations.
33	B-Y GAIN ADJ	I	Adjust the gain of B-Y signal output of pin ㊴ by applying DC potential (2.0 to 3.0V).
34	G-R OUT	O	Output G-R color-difference signal synchronized by the multiplexer circuit.
35	G-B OUT	O	Output G-B color-difference signal synchronized by the multiplexer circuit.
36	Y_L-Y_H OUT	O	Output Y_L-Y_H signal.
37	Y_H OUT	O	Output Y_H signal which has been switchovered and sampled and held. [Y_H=0.25(G0+G1+R0/B0+R1/B1)]
38	$-Y_L$ OUT	O	Output YL signal by negative polarity. [Y_L=−0.3(G−R)−0.1(G−B)+G1+Δ(−G0−G2+G1)] Δ: Adjust with pin ③.

No.	Symbol	I/O	Description
39	B-Y OUT	O	Adjust gain with pin ㉝ and output B-Y signal in which the mixed volume of R-Y has been adjusted by pin ①. [B−Y=0.3(G−R)−0.9(G−B)±Δ[0.1(G−B)−0.7(G−R)] Δ: Adjust with pin ①.
40	R-Y OUT	O	Adjust gain with pin ㉛ and output R-Y signal in which the mixed volume of B-Y has been adjusted by pin ②. [R−Y=0.1(G−B)−0.7(G-R)±[0.3(G−R)−0.9(G−B)] Δ: Adjust with pin ②.
41	Vcc1		8.5V power supply
42	R2/B2 IN	I	Input R/B linesequentialsignal delayed 2H through a clamping capacitor.
43	GND2		Ground
44	G2 IN	I	Input G signal delayed 2H through a clamping capacitor.
45	Dummy DC	I	DC input corresponding to pins ⑫, ⑬, ㊷, ㊹, ㊻ and ㊽, connect to power supply or GND through a capacitor.
46	R1/B1 IN	I	Input R/B linesequentialsignal delayed 1H through a clamping capacitor.
47	Vcc2		5.0V power supply signal processing system.
48	G1 IN	I	Input G signal delayed 1H through a clamping capacitor.

Electrical Characteristics

(Ta=25°C, V_{CC}=8.5V, $V_{CC}2$=$V_{CC}3$=5.0V, See Fig. 2.)

Symbol	Item	Measuring point	SW condition																Bias condition (V)														
			SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12	SW 13	SW 14	SW 15	SW 16	E 1	E 2	E 3	E 4	E 5	E 6	E 7	E 8	E 9	E 10	E 11	E 12	E 13	E 14	E 15
DC1	DC check	V1	a	a	a	a	a	a	a	a	a	a	OFF	OFF	OFF	OFF	OFF	OFF	5.0	2.5	2.5	2.5	2.5	2.5				2.5		2.5			2.5
DC2	DC check	V2																															
DC3	DC check	V4																															
DC4	DC check	V28																															
DC5	DC check	V29																															
DC6	DC check	V30																															
DC7	DC check	V32	↓	↓	↓	↓	↓	↓		↓	↓	↓																					
I1	Circuit current (5.0V)	A1	b	b	b	b	b	b		b	c	c																					
I2	Circuit current (8.5V)	A2																															
G1	G0 gain	V10																															
G2	R0/B0 gain	V5	↓	↓	↓	↓													↓														
DC8	G0 output DC range	V10	a	a	a	a													3.5														
DC9		↓																	6.0														
DC10	R0/B0 output DC range	V5																	3.5														
DC11		↓																	6.0														
DC12	G1 output DC range	V9																	3.5														
DC13		↓																	6.0														
DC14	R1/B1 output DC range	V6																	3.0														
DC15		↓																	6.0														
DC16	Dispersion among 4 channels	↓	↓	↓	↓	↓													5.0	↓	↓	↓	↓										
G3	G1 gain control range	V9	b	b	b	b														2.0	2.0	2.0	2.0										
G4		↓																		3.0	3.0	3.0	3.0										
G5	R1/B1 gain control range	V6																		2.0	2.0	2.0	2.0										
G6		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	3.0	3.0	3.0	3.0	↓			↓		↓			↓
G7	G2 gain control range	V8	b	b	b	b	b	b	a	b	c	c	OFF	OFF	OFF	OFF	OFF	OFF	5.0	2.0	2.0	2.0	2.0	2.5				2.5		2.5			2.5
G8		↓																		3.0	3.0	3.0	3.0										
G9	R2/B2 gain control range	V7																		2.0	2.0	2.0	2.0										
G10		↓								↓										3.0	3.0	3.0	3.0										
G11	G-R amplifier gain	V34								a										(1)	(2)	(3)	(4)										
		↓					↓	↓												ST2	ST3	ST4	ST5										
R1	Color-difference	V35	↓				a	a												↓	↓	↓	↓										
R2	composition ratio		a	a	↓	↓	b	b		↓																							
DC17	MPX variable range				a	a	a	a		b										2.5	2.5	2.5	2.5	2.0									
DC18		↓			↓	↓														↓	↓			3.0									
G12	R-Y amplifier gain	V40			b	b				a										ST2	ST3			2.5			2.0						
G13			↓	↓	↓	↓	↓	↓												↓	↓	↓	↓				3.0						
R3	R-Y composition ratio	↓	b	b	a	a	b	b	↓					↓						2.5	2.5	ST4	ST5	↓			↓		↓			↓	
DC19	R-Y DC offset	V40	a	a	a	a	a	a	b					ON								2.5	2.5	2.5		2.0		(5) ST10		2.5			2.5
DC20			↓	↓			↓	↓	↓							↓		↓				↓	↓			3.0		↓					

Symbol	Item	Measuring point	SW condition																Bias condition (V)															
			SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12	SW 13	SW 14	SW 15	SW 16	E 1	E 2	E 3	E 4	E 5	E 6	E 7	E 8	E 9	E 10	E 11	E 12	E 13	E 14	E 15
G14	B-Y MIX gain		b	b				b	b	a				OFF		ON		ON				ST4	ST5					1.8	3.5			2.2	
G15																																2.8	
G16	B-Y amplifier gain	V39														OFF		OFF									2.5		2.0				
G17																														3.0			
R4	B-Y composition ratio		a	a	b	b	a	a												ST2	ST3	2.5	2.5							3.0			
DC21	B-Y DC offset				a	a			b						ON					2.5	2.5						2.0			(6) ST12			
DC22																											3.0						
G18	R-Y MIX gain	V39	a	a	b	b	a	a	a	a	c	c	OFF	OFF	OFF	ON	ON	OFF	5.0	ST2	ST3	2.5	2.5	2.5				2.5	3.5	1.8	2.2		2.5
G19																															2.8		
G20	$-Y_L$ amplifier gain	V38	b	b	b	b	b	b	a	a	c	c				OFF	OFF			ST2	ST3	ST4	ST5							2.5			
R5	$-Y_L$ composition ratio		a		a	a	a																										
R6			a		b		a																										
G21	V aperture control				b	a															2.5	2.5	2.5										2.0
																																	3.0
G22	V_H amplifier gain	V37	b																														2.5
	Y_H composition ratio				a																ST3												
R7			a	b																													
R8				a	b																												
R9					a	b																											
DC23	Y_H DC offset					a																											
DC24	Y_H DC variable range												ON												4.0								
DC25																									5.0								
G23	Y_L-Y_H gain	V36	b	b	b	b	b	b					OFF									ST4	ST5										
DR1	G0 D.R	V10	c	c	c	c	c	c																									
DR2	R0/B0 D.R	V5																															
DR3	G1 D.R	V9																		3.0	3.0	3.0	3.0	3.0									
DR4	R1/B1 D.R	V6																															
DR5	G2 D.R	V8																															
DR6	R2/B2 D.R	V7																															
DR7	R-Y D.R	V40	a	a			a													ST2	ST3	2.5	2.5					4.0					
DR8	B-Y D.R	V39	c	c	a	a	c	c												2.5	2.5	ST4	ST5					2.5		4.0			
DR9	$-Y_L$ D.R	V38	c	c	c	c	c	c	a	a	c	c	OFF	OFF	OFF	OFF	OFF	OFF	5.0	ST2	ST3	ST4	ST5	3.0				2.5		2.5			2.5
DR10	Y_H D.R	V37		a		a																											
DR11	Y_L-Y_H D.R	V36		c		c																											
DR12	0 line DR ratio	V10.5																						2.5									
DR13	1 line DR ratio	V9.6																															
DR14	2 line DR ratio	V8.7																															

Electrical Characteristics (Ta=25°C, Vcc1=8.5V, Vcc2=Vcc3=5.0V, See Fig. 2)

Symbol	Item	Measuring point	Condition	Min.	Typ.	Max.	Unit
DC1	DC check	V1	DC potential of pin 1	1.5	1.8	2.1	V
DC2	DC check	V2	DC potential of pin 2	1.5	1.8	2.1	V
DC3	DC check	V4	DC potential of pin 4	2.4	2.7	3.0	V
DC4	DC check	V28	DC potential of pin 28	3.9	4.3	4.7	V
DC5	DC check	V29	DC potential of pin 29	2.2	2.5	2.8	V
DC6	DC check	V30	DC potential of pin 30	2.2	2.5	2.8	V
DC7	DC check	V32	DC potential of pin 32	2.2	2.5	2.8	V
I1	Circuit current (5.0V)	A1	Circuit current of 5.0V group	18.1	25.0	32.6	mA
I2	Circuit current (8.5V)	A2	Circuit current of 8.5V group	11.4	15.0	18.9	mA
G1	G0 gain	V10	Pin 10 OUT/S1	1.0	1.2	1.4	
G2	R0/B0 gain	V5	Pin 5 OUT/S2	1.0	1.2	1.4	
DC8	G0 output DC range	V10	DC potential of pin 10 OUT when E1 is set to 3.5V and 6.0V	3.33	3.5	3.68	V
DC9		↓		5.68	6.01	6.34	V
DC10	R0/B0 output DC range	V5	DC potential of pin 5 OUT when E1 is set to 3.5V and 6.0V	3.26	3.53	3.82	V
DC11		↓		5.60	6.02	6.46	V
DC12	G1 output DC range	V9	DC potential of pin 9 OUT when E1 is set to 3.5V and 6.0V	3.28	3.56	3.85	V
DC13		↓		5.61	6.03	6.49	V
DC14	R1/B1 output DC range	V6	DC potential of pin 6 OUT when E1 is set to 3.5V and 6.0V	3.28	3.56	3.85	V
DC15		↓		5.59	6.01	6.45	V
DC16	Dispersion among 4 channels	↓	DC10-DC8, DC12-DC8, DC14-DC8	−85	50	210	mV
G3	G1 gain control range	V9	Pin 9 PUT/S1		0	0.16	mV
G4		↓		1.48	1.68	1.89	
G5	R1/B1 gain control range	V6	Pin 6 OUT/S3		0	0.16	
G6		↓		1.48	1.68	1.89	
G7	G2 gain control range	V8	Pin 8 OUT/S1		0	0.16	
G8		↓		1.48	1.68	1.89	
G9	R2/B2 gain control range	V7	Pin 7 OUT/S2		0	0.16	
G10		↓		1.48	1.68	1.89	
G11	G-R amplifier gain	V34	Pin 34 OUT/S1	0.95	1.20	1.47	
R1	Color-difference composition ratio	V35	Pin 34 OUT/ Pin 35 OUT of G11	1.78	1.98	2.21	
R2		↓		1.78	1.98	2.21	
DC17	MPX variable range	↓	A (See p.16)	−76	−160	−252	mV
DC18		↓		+86	+170	+263	mV
G12	R-Y amplifier gain	V40	Pin 40 OUT/S1	0.31	0.48	0.66	
G13		↓		1.14	1.43	1.71	

Symbol	Item	Measuring point	Condition	Min.	Typ.	Max.	Unit
R3	R-Y composition ratio	↓	Pin 40 out/ Pin 40 OUT of G13	5.8	6.7	7.6	
DC19	R-Y DC offset	V40	B (See p.16)	48	100	158	mV
DC20		↓		−173	−115	−63	mV
G14	B-Y MIX gain	↓	Pin 40 OUT/S1 Note) Output during E14=22V is negative polarity.	0.19	0.28	0.40	
G15		↓		0.28	0.37	0.48	
G16	B-Y amplifier gain	V39	Pin 39 OUT/S1	0.4	0.5	0.6	
G17		↓		1.3	1.6	1.9	
R4	B-Y composition ratio	↓	Pin 39 OUT/ Pin 39 OUT of G17	2.61	3.0	3.41	
DC21	B-Y DC offset	↓	C (See p.16)	43	95	152	mV
DC22		↓		−163	−105	−52	mV
G18	R-Y MIX gain	V39	Pin 39 OUT/S1 Note) Output during E13=2.8V is negative polarity	0.18	0.26	0.35	
G19		↓		0.27	0.34	0.42	
G20	$-Y_L$ amplifier gain	V38	Pin 38 OUT/S1	1.0	1.3	1.6	
R5	$-Y_L$ composition	↓	Pin 38 OUT/	8.6	10.5	12.6	
R6	ratio	↓	Pin 38 OUT of G20	2.9	3.3	3.8	
G21	V aperture control gain	↓	Measure pin 38 OUT during E15= 2.0V and 3.0V, and caluculate (output during 3.0V − output during 2.0V)/2				
		↓		170	255	340	mV
G22	Y_H amplifier gain	V37	Pin 37 OUT/S1	1.9	2.45	3.0	
	Y_H composition ratio	↓	Set pin 37 OUT to a Set pin 37 OUT to b and obtain b/a				
R7		↓		0.5	1.0	1.5	
R8		↓	Set pin 37 OUT to c and obtain c/a	0.5	1.0	1.5	
R9		↓	Set pin 37 OUT to d and obtain d/a	0.5	1.0	1.5	
DC23	Y_H DC offset	↓	D (See p.16)		0	105	mV
DC24	Y_H DC variable range	↓	E (See p.16)	323	620	945	mV
DC25		↓		494	810	1155	mV
G23	Y_L-Y_H gain	V36	Pin 36 OUT/S1	0.34	0.45	0.57	
DR1	G0 D.R	V10	Pin 10 OUT/S4	1.05	1.18	1.32	
DR2	R0/B0 D.R	V5	Pin 5 OUT/S5	1.05	1.18	1.32	
DR3	G1 D.R	V9	Pin 9 OUT/S4	1.40	1.57	1.75	
DR4	R1/B1 D.R	V6	Pin 6 OUT/S6	1.40	1.57	1.75	

Symbol	Item	Measuring point	Condition	Min.	Typ.	Max.	Unit
DR5	G2 D.R	V8	Pin 8 OUT/S4	1.40	1.57	1.75	
DR6	R2/B2 D.R	V7	Pin 7 OUT/S5	1.40	1.57	1.75	
DR7	R-Y D.R	V40	Pin 40 OUT/S4	1.3	1.7	2.1	
DR8	B-Y D.R	V39	Pin 39 OUT/S4	1.57	1.85	2.15	
DR9	$-Y_L$ D.R	V38	Pin 38 OUT/S4	1.10	1.26	1.43	
DR10	Y_H D.R	V37	Pin 37 OUT/S4	1.9	2.28	2.69	
DR11	Y_L-Y_H D.R	V36	Pin 36 OUT/S4	0.38	0.465	0.56	
DR12	0 line DR ratio	V10.5	DR2/DR1	0.8	1.0	1.2	
DR13	1 line DR ratio	V9.6	DR4/DR3	0.8	1.0	1.2	
DR14	2 line DR ratio	V8.7	DR6/DR5	0.8	1.0	1.2	

Measuring Condition of Temperature Characteristics

Measuring item	Measuring pin	SW condition	Bias condition (V)														
			E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15
G0 OUT temperature characteristics	10	Similar to Electrical Characteristics I1 [Circuit current(5.0V)]	5.0	ST2	ST3	ST4	ST5	ST6*				ST10		ST12			2.0
R0/B0 OUT	5	Similar to Electrical Characteristics I1 [Circuit current(5.0V)]															
G1 OUT	9	Similar to Electrical Characteristics I1 [Circuit current(5.0V)]															
R1/B1 OUT	6	Similar to Electrical Characteristics I1 [Circuit current(5.0V)]															
G2 OUT	8	Similar to Electrical Characteristics I1 [Circuit current(5.0V)]															
R2/B2 OUT	7	Similar to Electrical Characteristics I1 [Circuit current(5.0V)]	↓														
Auto bias for DL	11	Similar to Electric Characteristics DC8 [G0 output DC range]	3.0														
G-R OUT	34	Similar to Electric Characteristics I1 [Circuit current (5.0V)]	5.0														
G-B OUT	35	Similar to Electric Characteristics I1 [Circuit current (5.0V)]															
R-Y OUT	40	Similar to Electric Characteristics I1 [Circuit current (5.0V)]															
B-Y OUT	39	Similar to Electric Characteristics I1 [Circuit current (5.0V)]										↓		↓			
R-Y MIX	39	Similar to Electric Characteristics G18 [R-Y MIX gain]										1.8	3.5	1.8	3.0	3.0	
B-Y MIX	40	Similar to Electric Characteristics G14 [B-Y MIX gain]										↓	↓	↓	↓	↓	
Y_H OUT	37	Similar to Electric Characteristics G14 [B-Y MIX gain]										ST10		ST12			
Y_L-Y_H OUT	36	Similar to Electric Characteristics G14 [B-Y MIX gain]															
$-Y_L$ OUT	38	Similar to Electric Characteristics G14 [B-Y MIX gain]															↓
V aperture control volume	38	Similar to Electric Characteristics G21 [V aperure control gain]	↓	↓	↓	↓	↓	↓				↓		↓			3.0

* **Note)** ST6 ... Potential of E6 in which the output becomes a straight line under the SW condition of DC17 (MPX variable range), and by making the biases other E6 have the same G0 OUT temperature characteristics as above and by varying the E6 while observing pin 34.

Electrical Characteristics Test Circuit

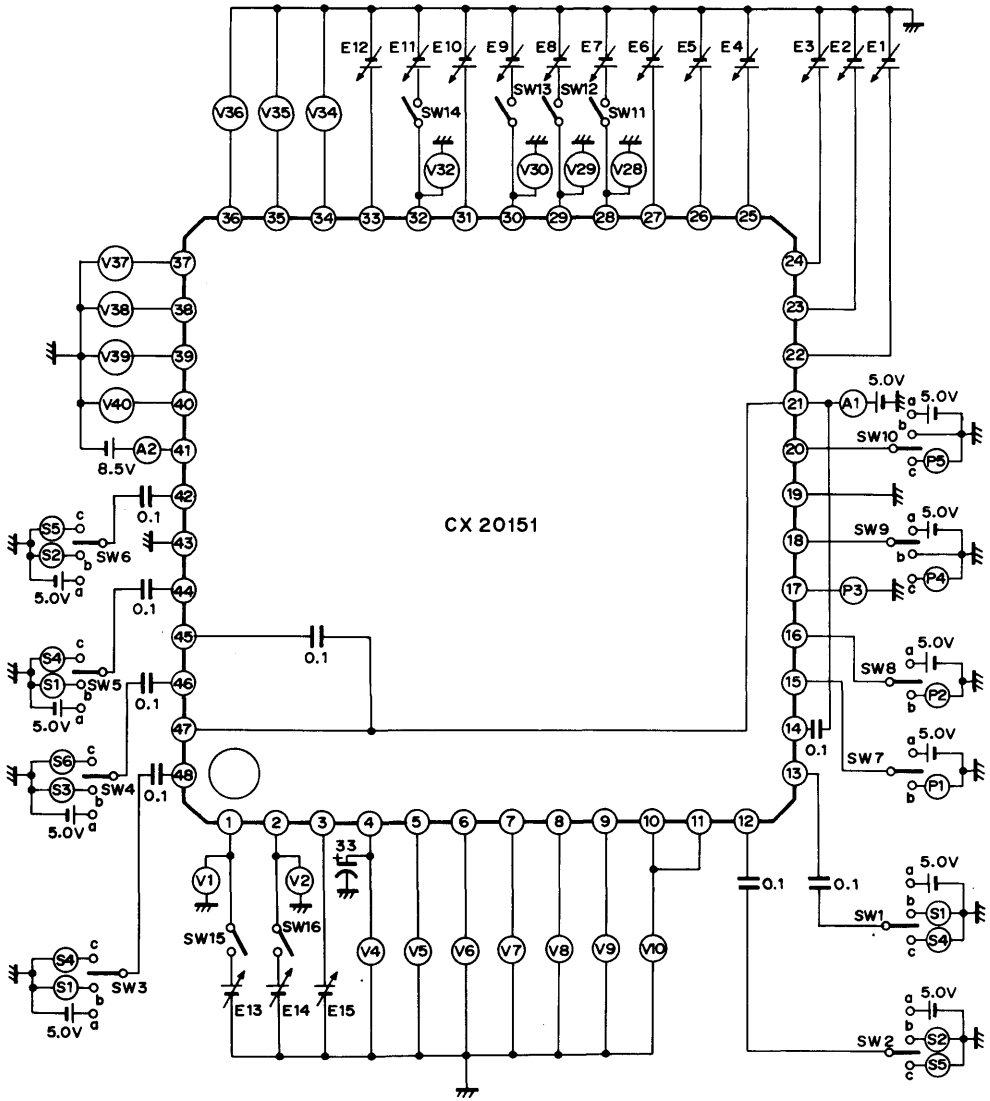
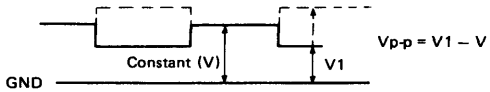


Fig. 2

Bias Condition Definition

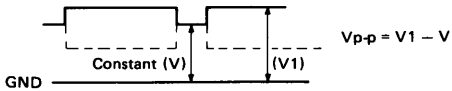
(1) ST2: E2 potential in which the output p-p of pin 9 becomes equivalent to output p-p of pin 10.
(2) ST3: E3 potential in which the output p-p of pin 6 becomes equivalent to output p-p of pin 5.
(3) ST4: E4 potential in which the output p-p of pin 8 becomes equivalent to output p-p of pin 10.
(4) ST5: E5 potential in which the output p-p of pin 7 becomes equivalent to output p-p of pin 5.
(5) ST10: E10 potential in which the output p-p of pin 40 becomes 400 mV.
(6) ST12: E12 potential in which the output p-p of pin 39 becomes 400 mV.

Condition A



Waveform similar to P2 is output to pin 35 as shown in above figure. DC is constant when P2 is H. Measuring of V1 has been performed when E6 is set to 2.0V and 3.0V, and the Vp-p has been calculated.

Condition B and C



Waveform similar to P1 is output to pins 40 and 39 as shown in above figure. Measuring of V1 has been performed when E8 and E9 are set to 2.0V and 3.0V, and the Vp-p has been calculated.

Condition D and E

Signal of 4.77 MHz is output to pin 37 as shown in the above figure. D measures this Vp-p. E varies the DC of pin 28 with E7, and measuring is carried out on Vp-p of pin 37 output.
(When the DC of pin 28 is varied, the Vp-p of pin 37 output fluctuates. In this case, confirm that there is a point of Vp-p=0 mV between E7=4.0V and 5.0V.)

Timing of Electrical Characteristics in the Signal System

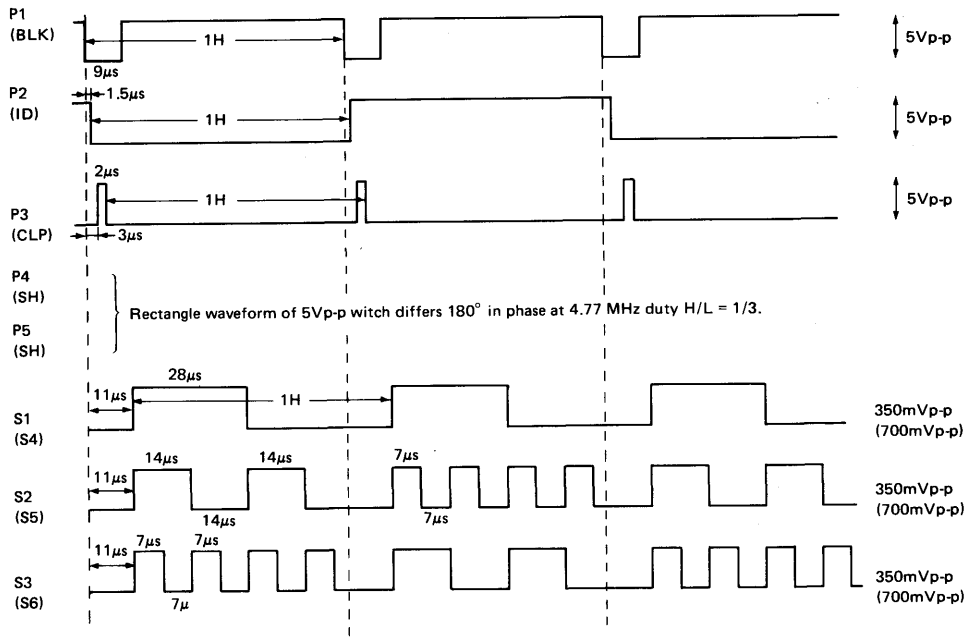
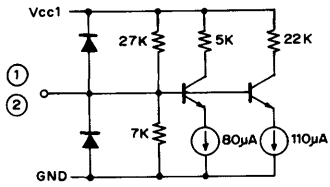
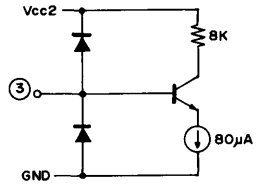
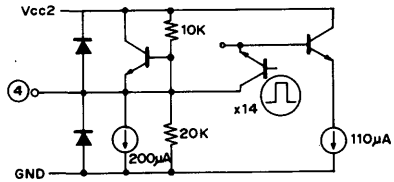
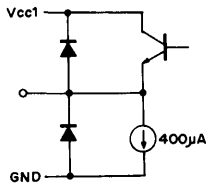
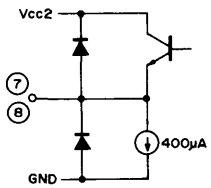
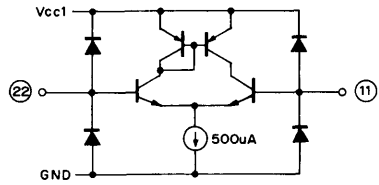
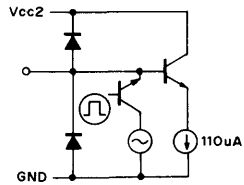
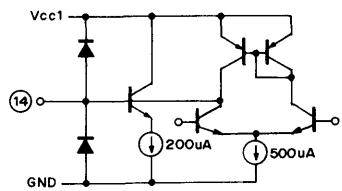
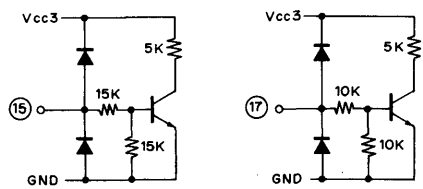
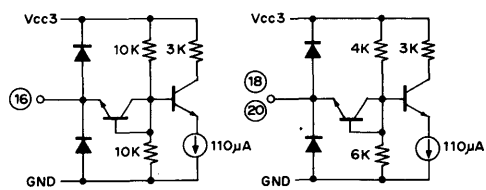
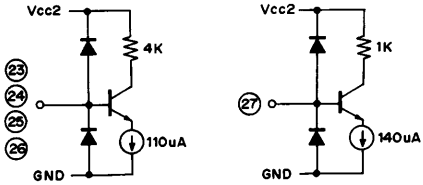
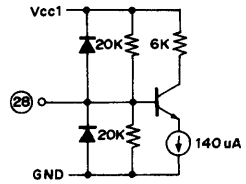
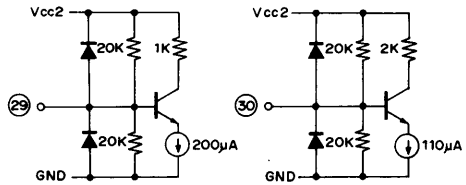
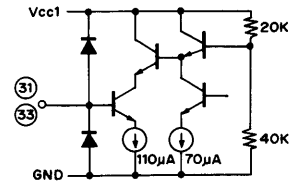
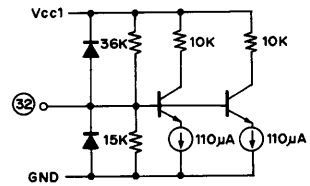


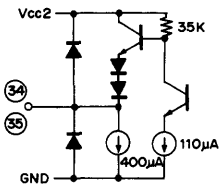
Fig. 3

Standard Circuit Design Materials (Ta=25°C, V_{CC}=8.5V, V_{CC2}=V_{CC3}=SV)

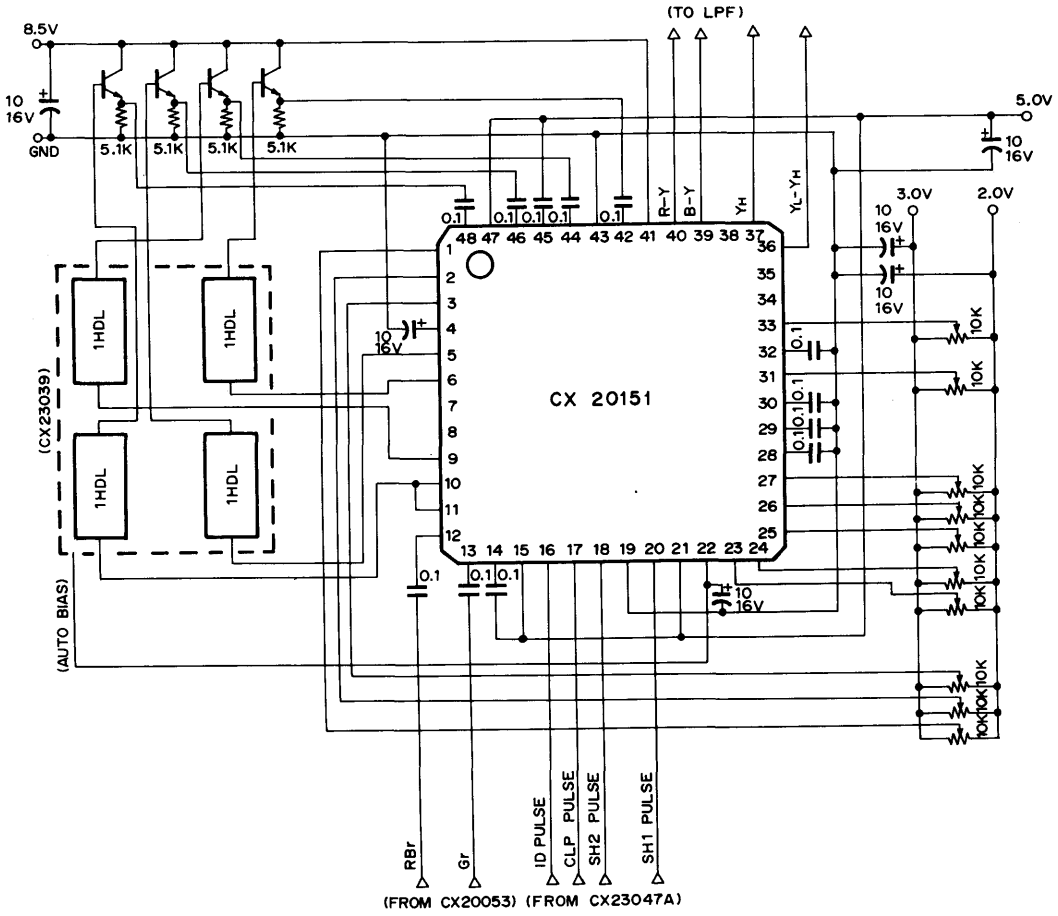
No.	Symbol	Equivalent circuit	DC potential
1	R-Y Mix C.		1.8V
2	B-Y Mix C.		
3	APERTURE C.		
4	CI.P DC		2.7V
5	R0/B0 OUT		
6	R1/B1 OUT		
9	C1 OUT		
10	C0 OUT		
36	Y_L-Y_H OUT		
37	Y_H OUT		
38	-Y_L OUT		
39	B-Y OUT		
40	R-Y OUT		
7	R2/B2 OUT		
8	C2 OUT		

No.	Symbol	Equivalent circuit	DC potential
11	COM. IN		
22	DC ADJ for DL		
12	R0/B0 r IN		
13	C0 r IN		
42	R2/B2 In		
44	C2 IN		
45	Dummy DC		
46	R1/B1 IN		
48	C1 IN		
14	C		
15	BLK PULSE		
17	CLP PULSE		
16	ID PULSE		
18	SH2 PULSE		
20	SH1 PULSE		
19	GND 1		
21	Vcc 3		5.0V

No.	Symbol	Equivalent circuit	DC potential
23	G1 GAIN ADJ		
24	R1/B1 GAIN ADJ		
25	G2 GAIN ADJ		
26	R2/B2 GAIN ADJ		
27	MPX DC ADJ		
28	Y_H OFFSET		4.25V
29	R-Y OFFSET		2.5V
30	B-Y DC OFFSET		
31	R-Y GAIN ADJ		
33	B-Y GAIN ADJ		
32	REFERENCE		2.5V

No.	Symbol	Equivalent circuit	DC potential
34	G-R OUT		
35	G-B OUT		
41	Vcc 1		8.5V
43	GND 2		
47	Vcc 2		5.0V

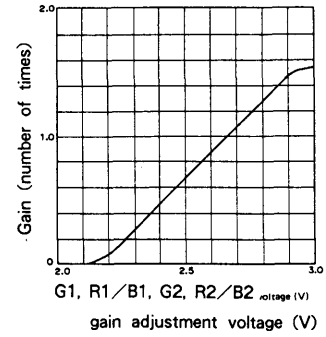
Application Circuit



* Decoupling is performed to 0.1μF capacitors 28, 29, 30 and 31 (Can do without decoupling).

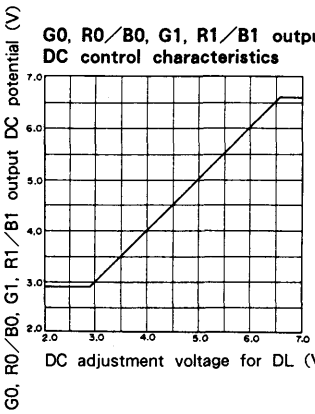
Fig. 4

G1, R1/B1, G2, R2/B2 gain control characteristics



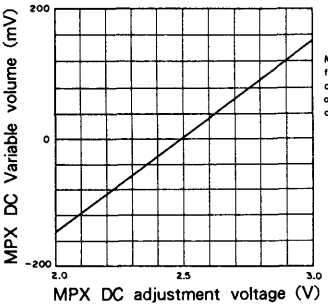
Measuring has been carried out by fluctuating the bias of E2 to E5 within the range of 2.0V to 3.0V, under the SW condition of G3 of the aforementioned Electrical Characteristics.

G0, R0/B0, G1, R1/B1 output DC control characteristics



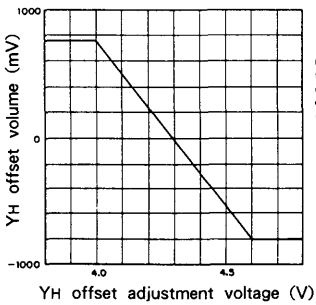
Measuring has been carried out by fluctuating the bias of E1 within the range of 2.0V to 7.0V, under the SW condition of DC8 of the aforementioned Electrical Characteristics.

MPX DC adjustment characteristics



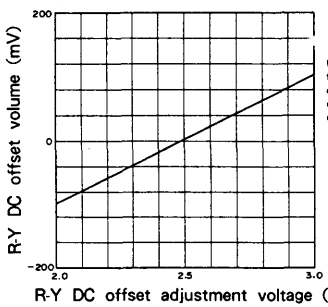
Measuring has been carried out by fluctuating bias of E6 within the range of 2.0V to 3.0V, under the SW condition of DC17 of the aforementioned Electrical Characteristics.

Y_H offset characteristics



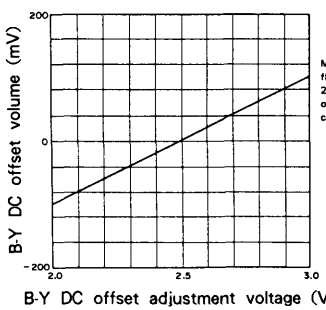
Measuring has been carried out by fluctuating bias of E7 within the range of 3.8V to 4.8V, under the SW condition of DC24 of the aforementioned Electrical Characteristics.

R-Y DC offset characteristics



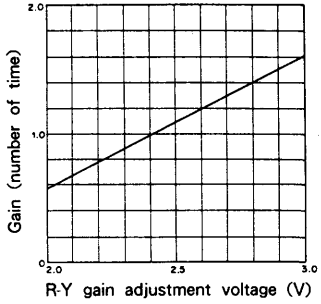
Measuring has been carried out by fluctuating bias E8 within the range of 2.0V to 3.0V, under the SW condition of DC19 of the aforementioned Electrical Characteristics.

B-Y DC offset characteristics



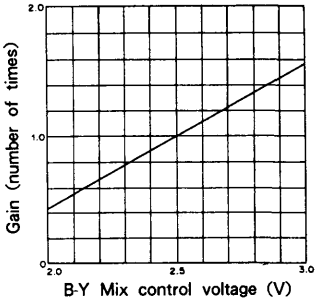
Measuring has been carried out by fluctuating bias E9 within the range of 2.0V to 3.0V, under the SW condition of DC21 of the aforementioned Electrical Characteristics.

R-Y gain control characteristics



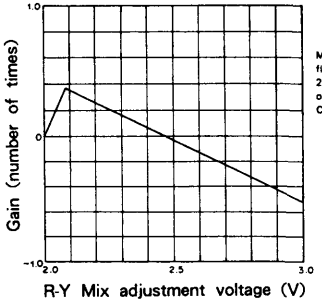
Measuring has been carried out by fluctuating bias E10 within the range of 2.0V to 3.0V, under the SW condition of G12 of the aforementioned Electrical Characteristics.

B-Y gain control characteristics



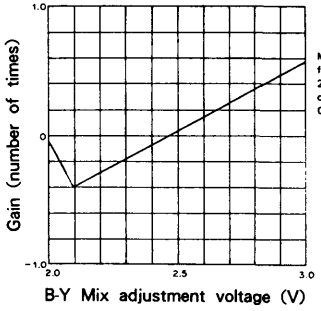
Measuring has been carried out by fluctuating bias E12 within the range of 2.0V to 3.0V, under the SW condition of G16 of the aforementioned Electrical Characteristics.

R-Y mix gain control characteristics



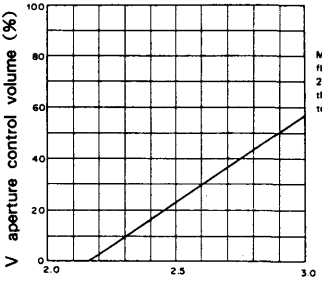
Measuring has been carried out by fluctuating bias E13 within the range of 2.0V to 3.0V, under the SW condition of G18 of the aforementioned Electrical Characteristics.

B-Y mix gain control characteristics



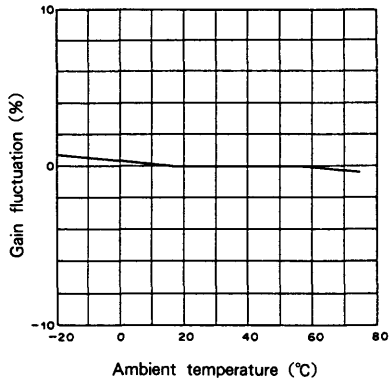
Measuring has been carried out by fluctuating bias E14 within the range of 2.0V to 3.0V, under the SW condition of G14 of the aforementioned Electrical Characteristics.

V aperture control gain control characteristics

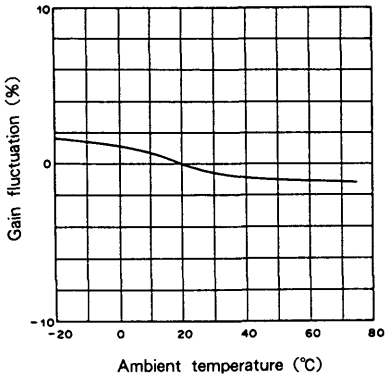


Measuring has been carried out by fluctuating bias E15 within the range of 2.0V to 3.0V, under the G21 method of the aforementioned Electrical Characteristics.

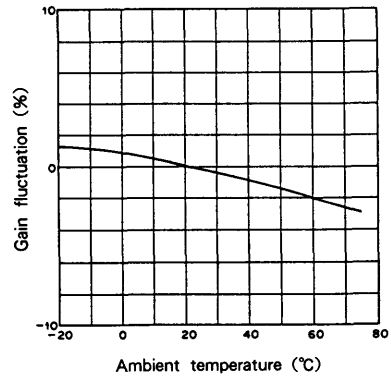
G0, R0/B0 OUT temperature characteristics



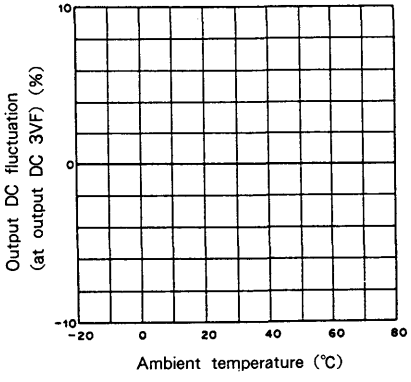
G1, R1/B1 OUT temperature characteristics



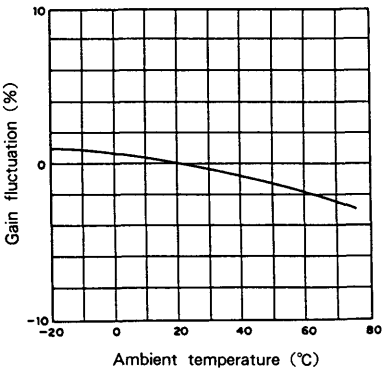
G2, R2/B2 OUT temperature characteristics



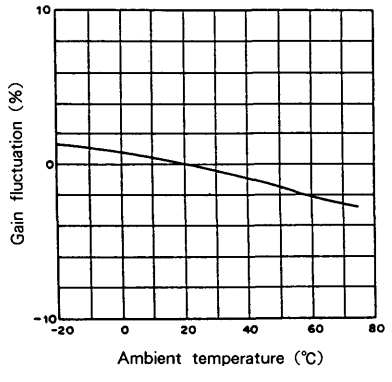
Auto bias temperature characteristics for DL



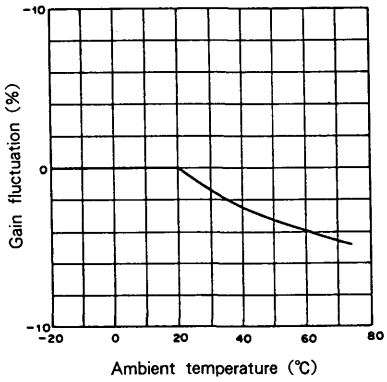
G-R OUT temperature characteristics



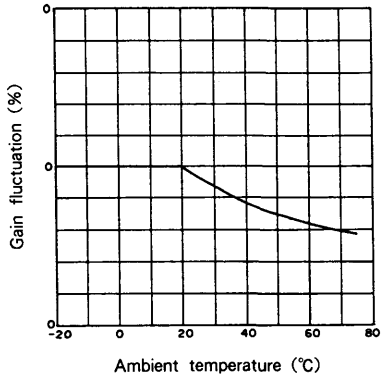
G-B OUT temperature characteristics



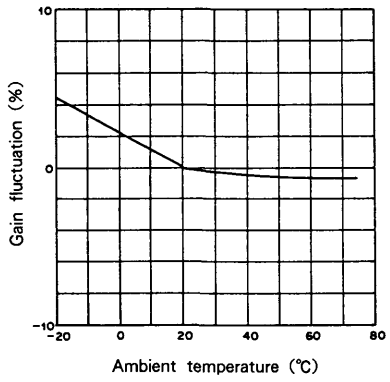
R-Y OUT temperature characteristics



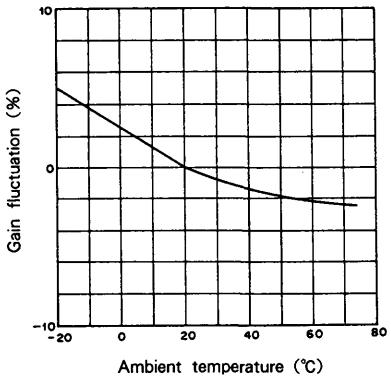
B-Y OUT temperature characteristics



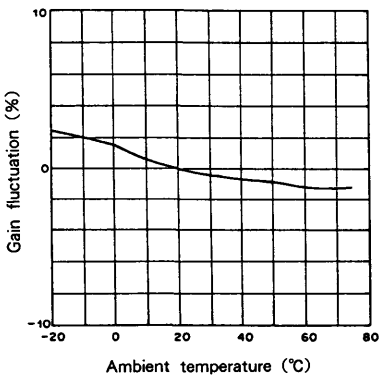
R-Y mix temperature characteristics (at B-Y OUT)



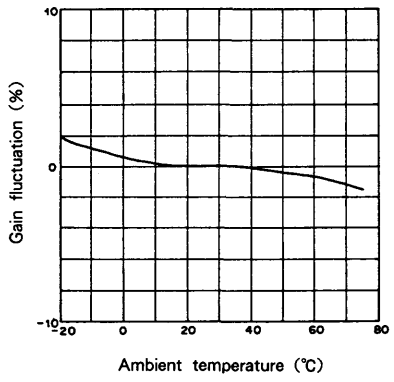
B-Y mix temperature characteristics (at R-Y OUT)



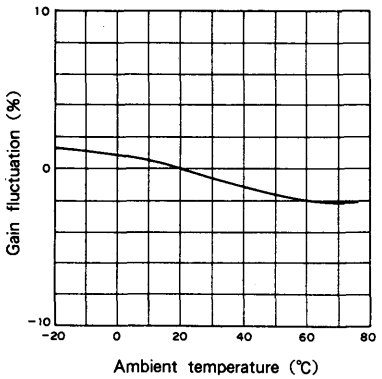
Y_H OUT temperature characteristics



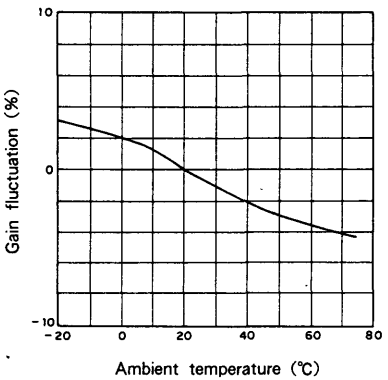
Y_L-Y_H OUT temperature characteristics



– Y_L OUT temperature characteristics

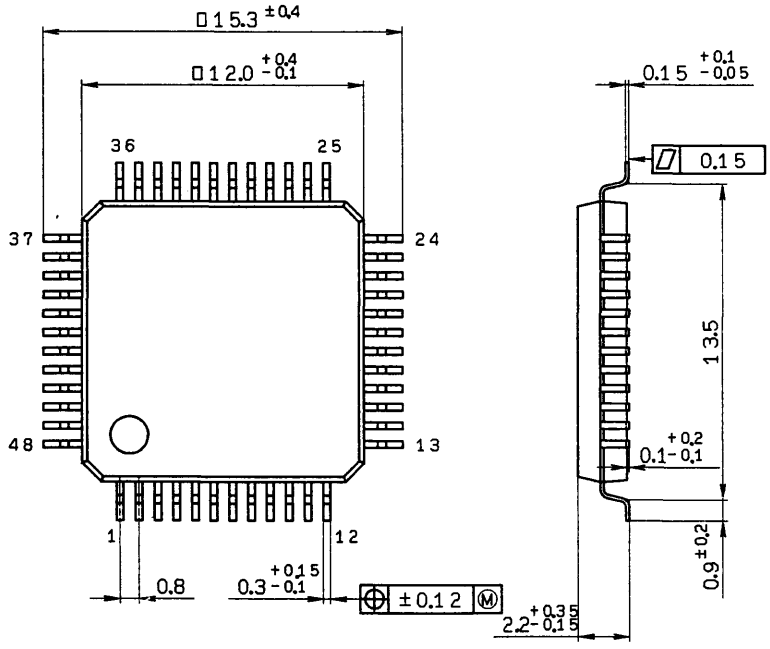


V aperture control volume temperature characteristics



Package Outline Unit : mm

CX20151 48 pin QFP (Plastic) 0.7g



QFP-48P-L04

1H × 4 CCD Delay line IC

Description

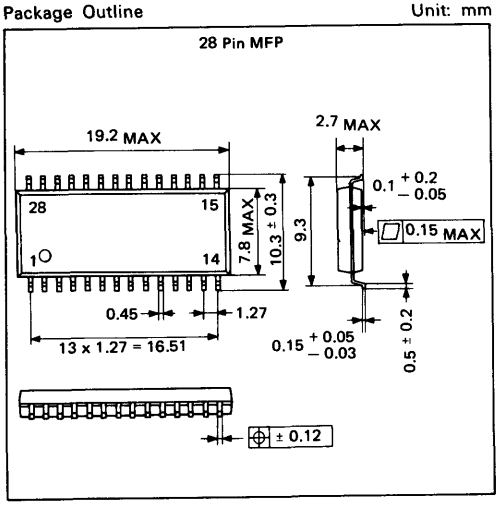
The CX23039 is a CMOS CCD signal processor which has been developed for the CCD camera.

The IC contains four 1H delay lines, clock drivers, the autobias circuit, and the pedestal clamp circuit, etc.

Features

- Low power consumption (Typ. 210mW)
- On Chip peripheral circuits

Package Outline Unit: mm



Absolute Maximum Ratings (Ta=25°C)

• Power supply voltage	V_{DD}	11	V
	V_{CL}	6	V
• Operating temperature	Topr	−10 ~ +60	°C
• Storage temperature	Tstg	−55 ~ +150	°C
• Allowable power dissipation	P_D	500	mW

Recomended Power Supply Conditions

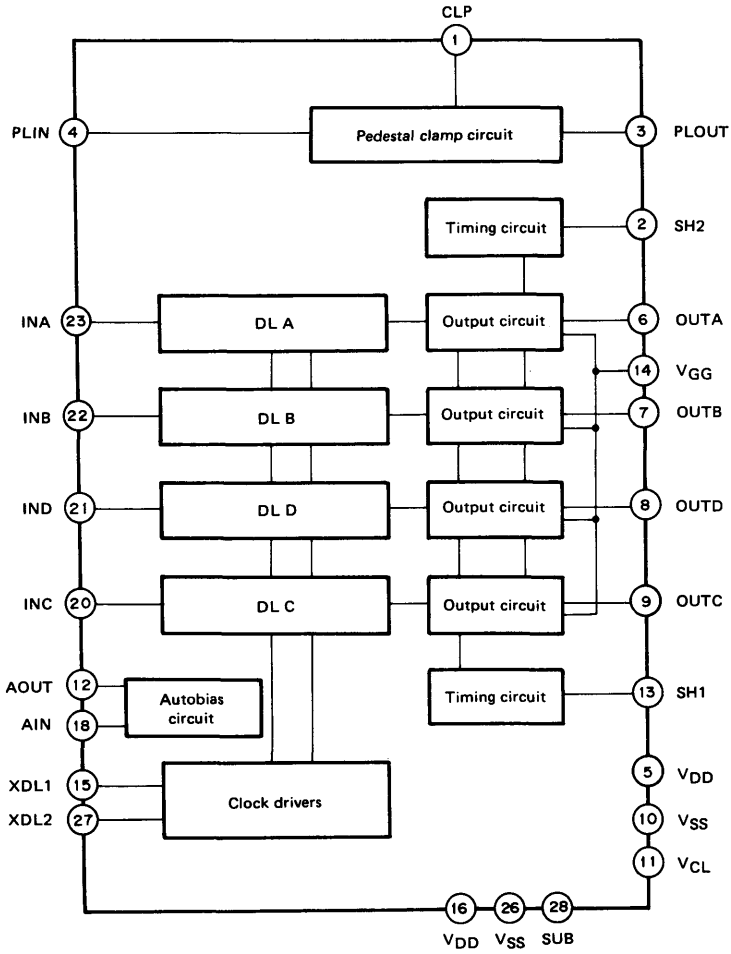
• Power supply voltage 1	V_{DD}	8.75 ~ 9.25	V
• Power supply voltage 2	V_{CL}	4.75 ~ 5.25	V

Recomended Clock Conditions

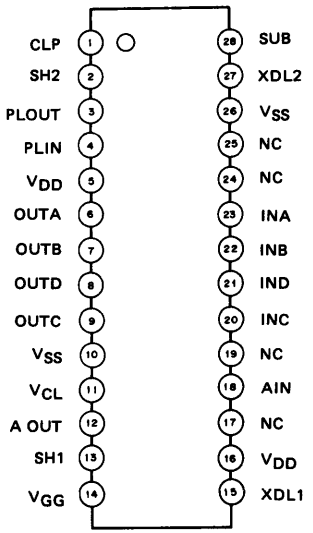
		Min.	Typ.	Max.	
• Clock voltage Low	V_L		0	0.4	V
• Clock voltage High	V_H	V_{CL}—1.0			V
• Clock frequency	f_{CL}		4.77		MHz

50169-ST

Block Diagram



Pin Configuration



(Top View)

Pin Description

Pin No.	Symbol	I/O	Description	Impedance [Ω]
1	CLP	I	Clamp pulse input	>100K
2	SH2	I	Sampling pulse input 2	>100K
3	PLOUT	O	DC feedback output	50K
4	PLIN	I	DC feedback input	>100K
5	V_{DD}		Power supply 1	
6	OUTA	O	Signal output A	1.2K
7	OUTB	O	Signal output B	1.2K
8	OUTD	O	Signal output D	1.2K
9	OUTC	O	Signal output C	1.2K
10	V_{SS}		GND	
11	V_{CL}		Power supply 2	
12	AOUT	O	Autobias circuit output	20K
13	SH1	I	Sampling pulse input 1	>100K
14	V_{GG}	I	Output circuit bias	>100K
15	XDL1	I	Clock pulse input 1	>100K
16	V_{DD}		Power supply 1	
17	NC			
18	AIN	I	Autobias circuit input	>100K
19	NC			
20	INC	I	Signal input C	>100K
21	IND	I	Signal input D	>100K
22	INB	I	Signal input B	>100K
23	INA	I	Signal input A	>100K
24	NC			
25	NC			
26	V_{SS}		GND	
27	XDL2	I	Clock pulse input 2	>100K
28	SUB		GND	

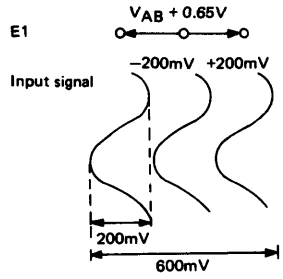
Electrical Characteristics

($Ta=25°C$, $V_{DD}=9V$, $V_{CL}=5V$, $V_{SS}=0V$, SUB=0V, $f_{CL}=4.77MHz$)

Item	Symbol	Measuring point	SW condition				Bias condition		Condition	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4	E1	E2					
Supply current 1	I_{DD}	A1	a	a	a	a					19	28	mA
Supply current 2	I_{CL}	A2	a	a	a	a					8	12	mA
Autobias voltage	V_{AB}	V1	a	a	a	a				4	5	6	V
Gate bias voltage	V_{GB}	V2	a	a	a	a				1	4	5.5	V
Voltage gain	G	V4	b	b	b	a-d	$V_{AB}+0.3$	V_{GB}		−3.3	0	+3.3	dB
Frequency response	fr	V4	c	b	b	a-d	$V_{AB}+0.3$	V_{GB}	$20\log\frac{\text{Output amplitude (SIN=2MHz, 600mVp-p)}}{\text{Output amplitude (SIN=200kHz, 600mVp-p)}}$	−4.5	3	0	dB
Linearity 1	L1	V4	d	b	b	a-d	$V_{AB}+0.65$	V_{GB}	Note 1 SIN=1 MHz, 200mVp-p		5	15	%
Linearity 2	L2	V4	d	b	b	a-d	$V_{AB}+0.3$	V_{GB}	Note 1 SIN=1 MHz, 200mVp-p		5	15	%
Linearity 3	L3	V4	d	b	b	a-d	$V_{AB}+0.2$	V_{GB}	Note 1 SIN=1 MHz, 200mVp-p		5	15	%
Output DC voltage	V_{DC}	V3	c	b	b	a-d	$V_{AB}+0.3$	V_{GB}		3	4	5	V
Gain mismatch	ΔG								Note 2		5	15	%
Linearity mismatch 1	ΔL1								Note 3		2	3	%
Linearity mismatch 2	ΔL2								Note 3		2	3	%
Linearity mismatch 3	ΔL3								Note 3		3	5	%
Output DC voltage difference between channels	ΔV_{DC}								Note 4		0.15	0.40	V

Note 1 Measuring method of L1, L2 and L3

In the measurement of L1, set input bias E1 to V_{AB}+0.65V first, and then set it to V_{AB} +0.85V and V_{AB} +0.45V by shifting ±200mV from the first value respectively. Then input the sine wave of S_{IN}=1 MHz and 200mVp-p, and compare the three output amplitudes.

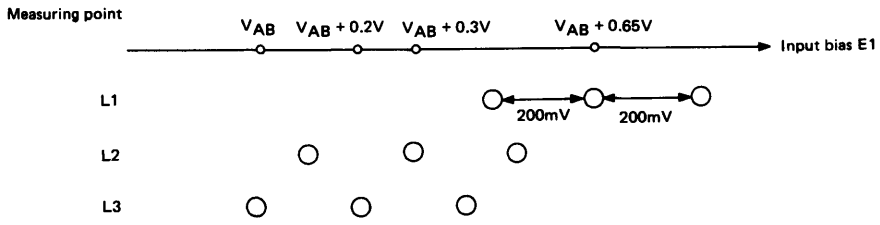


Define the maximum output amplitude as S_{OUTmax}, and minimum output amplitude as S_{OUTmin}, and output amplitude on E1=V_{AB}+0.65V as S_{OUTm} and define L1 as follows:

$$L1 = \frac{S_{OUTmax} - S_{OUTmin}}{S_{OUTm}} \times 100[\%] .$$

Similarly, define L2 and L3 by changing E1.

Accordingly, measurement is performed at nine points by changing the input bias level at each delay line.



Note 2 The voltage gain of A channel is defined as follows:

$$G(A)=20 \log \frac{OUTA}{INA}.$$

Similary, voltage gains of channels B, C and D are defined as G(B), G(C) and G(D) respectively.
The gain mismatch (ΔG) is defined as follows:

$$\Delta G = \frac{10^{\frac{Gmax}{20}} - 10^{\frac{Gmin}{20}}}{10^{\frac{Gmax}{20}} + 10^{\frac{Gmin}{20}}} \times 200 \quad [\%]$$

where Gmax is the maximum value of G(A), G(B), G(C) and G(D), and Gmin is the minimum value of G(A), G(B), G(C) and G(D).

Note 3 Define the linearity 1 values of channels A, B, C and D as L1(A), L1(B), L1(C) and L1(D). Define the maximum value of L1(A), L1(B), L1(C) and L1(D) as L1max and minimum value of those as L1min. The linearity mismatch 1(ΔL1) is defined as follows:

$\Delta L1 = L1\,max - L1\,min$ [%]

Similarly, define the maximum values of the 4 channels A, B, C and D of linearity 2 as L2 max and L3 max respectively and define minimum values of those as L2min and L3min respectively.
The linearity mismatch 2(ΔL2) and the linearity mismatch 3(ΔL3) are defined as follows:

$\Delta L2 = L2max - L2min$ [%]

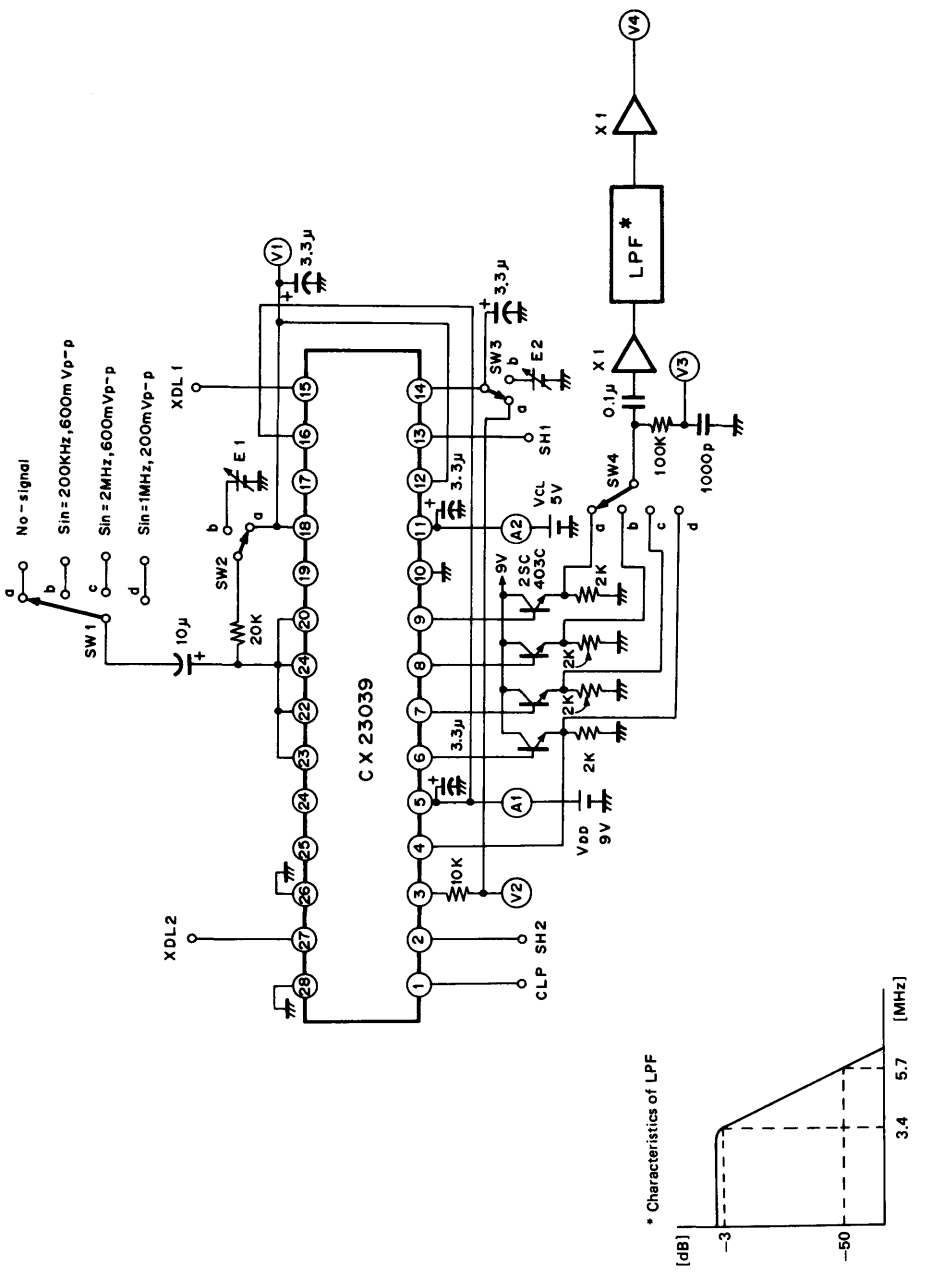
$\Delta L3 = L3max - L3min$ [%]

Note 4 Set input bias to E1=V_{AB}+0.3V. Define output DC voltage of cannels A, B, C and D as V_{DC}(A), V_{DC}(B), V_{DC}(C) and V_{DC}(D) respectively. The output DC voltage difference between channels (ΔV_{DC}) is defined as

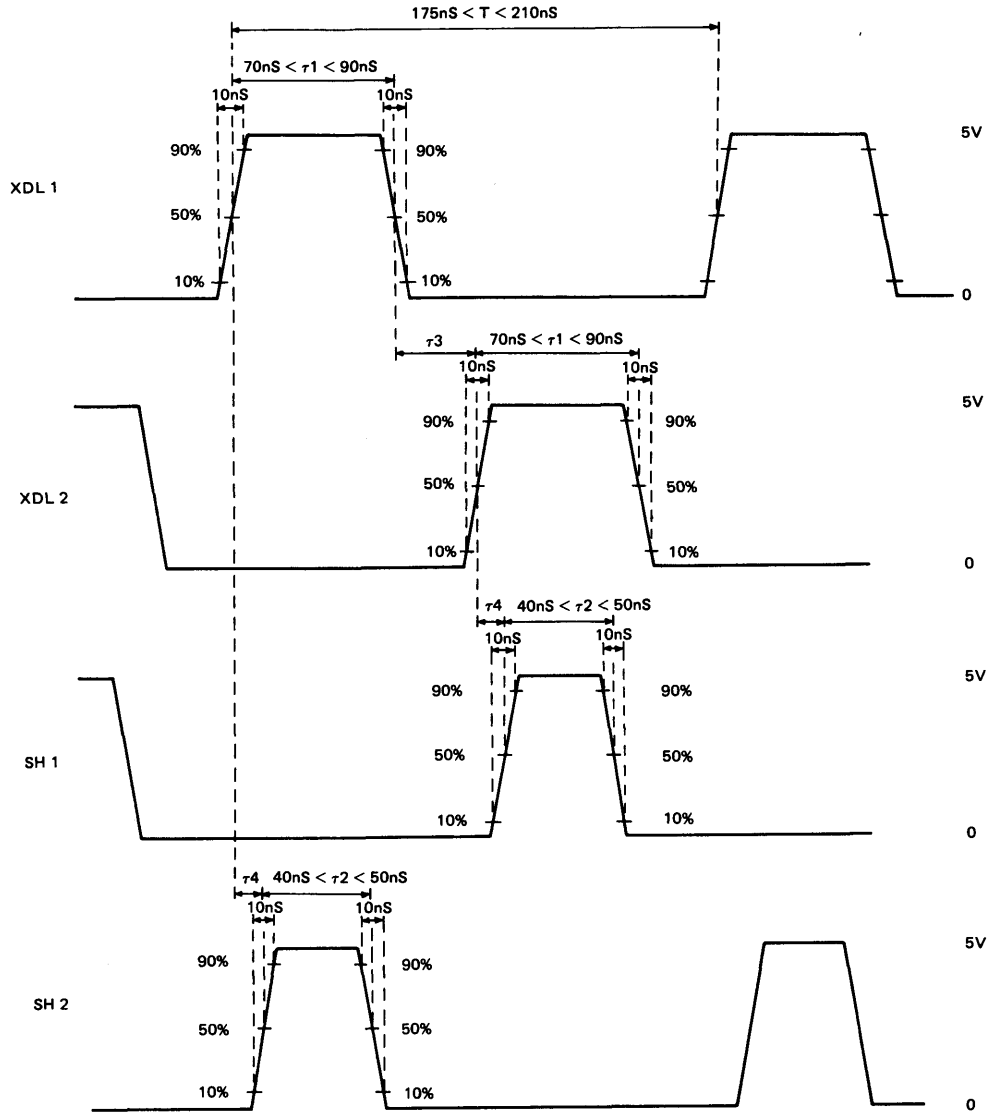
$$\Delta V_{DC} = V_{DCmax} - V_{DCmin}$$

where V_{DCmax} is the maximum value of V_{DC}(A), V_{DC}(B), V_{DC}(C) and V_{DC}(D) and V_{DCmin} is the minimum value of V_{DC}(A), V_{DC}(B), V_{DC}(C) and V_{DC}(D).

Electrical Characteristics Measuring Circuit



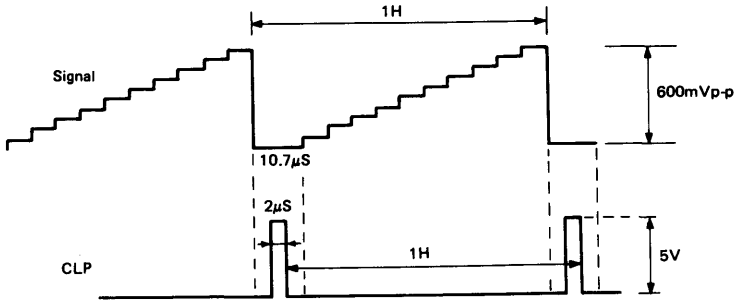
Clock Waveform and Timing Diagram

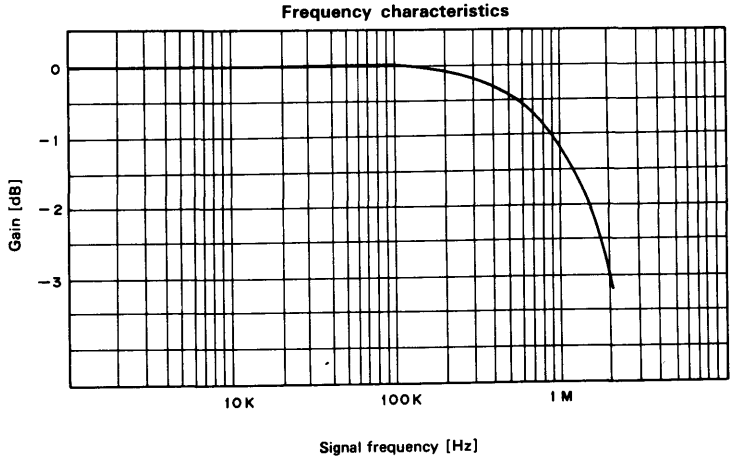


$$\tau 3 = \frac{T - 2 \times \tau 1}{2}$$

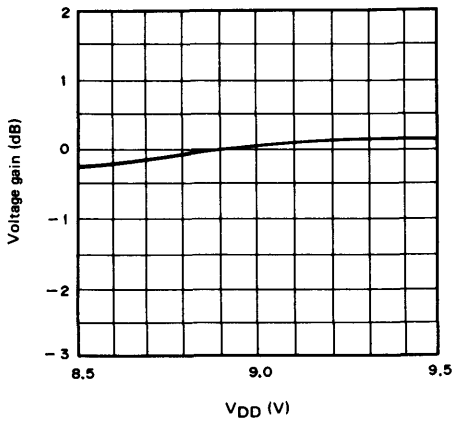
$$\tau 4 = \frac{\tau 1 - \tau 2}{2}$$

Clamp Pulse Waveform and Timing Diagram

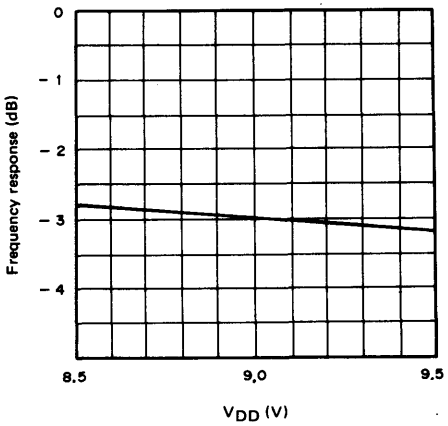




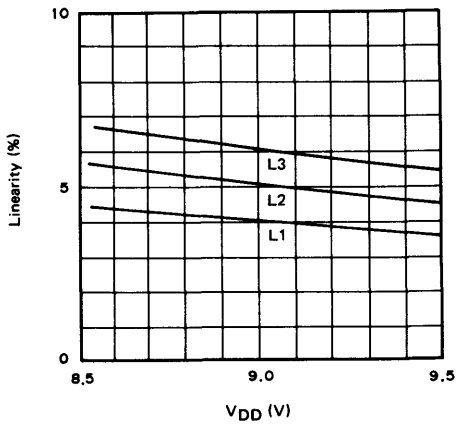
Voltage gain vs V_{DD}



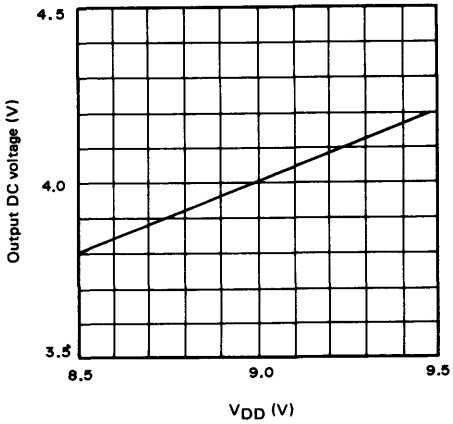
Frequency response vs V_{DD}



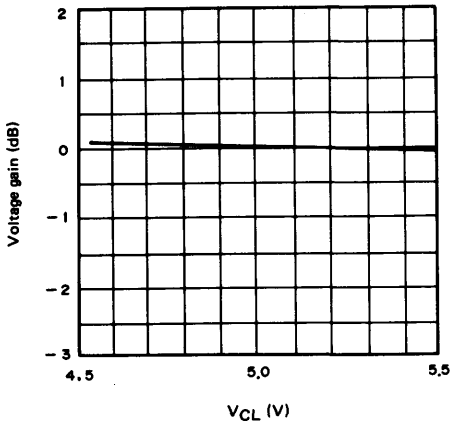
Linearity vs V_{DD}



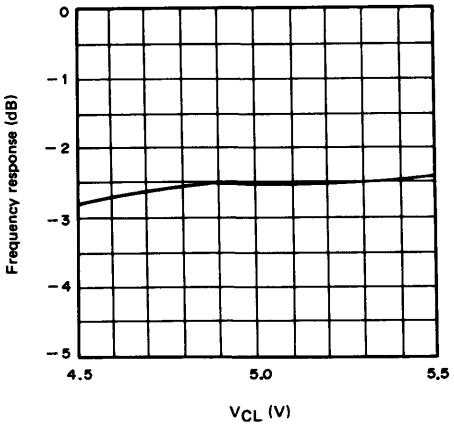
Output DC voltage vs V_{DD}



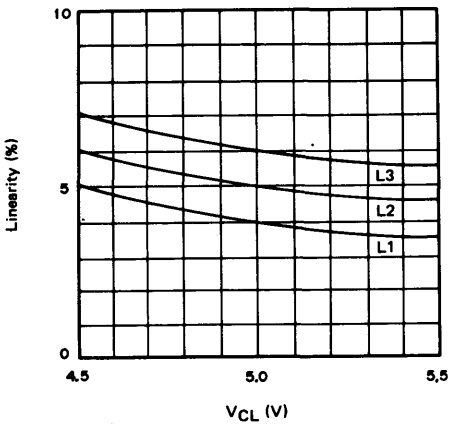
Voltage gain vs V_{CL}



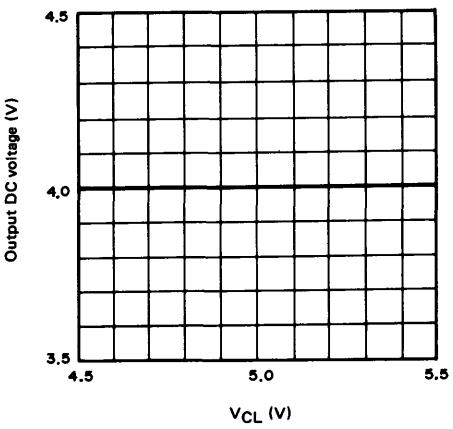
Frequency response vs V_{CL}



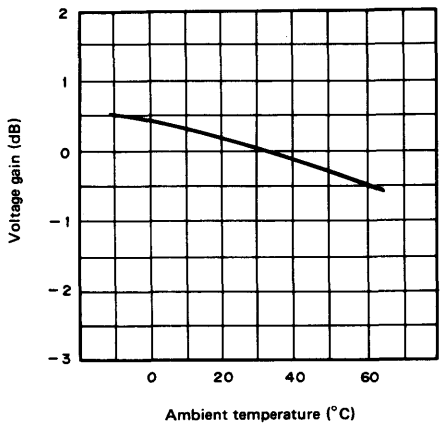
Linearity vs V_{CL}



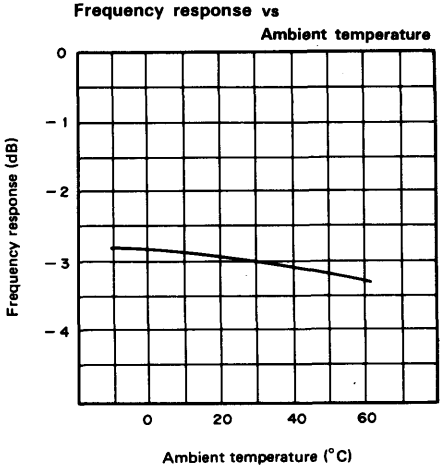
Output DC voltage vs V_{CL}



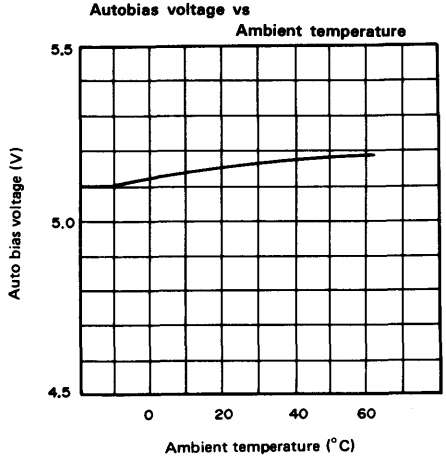
Voltage gain vs Ambient temperature



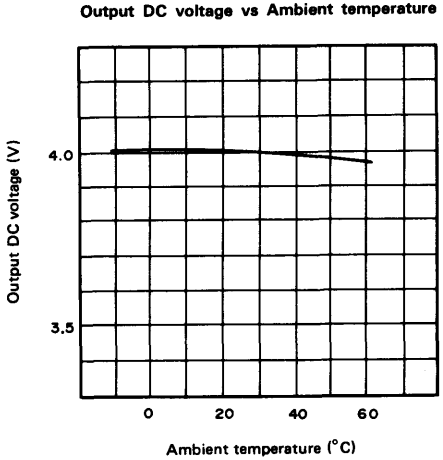
Frequency response vs Ambient temperature



Autobias voltage vs Ambient temperature



Output DC voltage vs Ambient temperature



SONY® CXA1337Q-Z/R

Processing system of a CCD Video Cameras

Description

CXA1337Q-Z/R is designed to extract signals from the CCD output of stripe CCD cameras during signal processing.
This bipolar IC executes correlated double sampling, AGC and color separation.

Features

- Through the double sampling function it can inhibit low band noise in CCD signals.
- A wide coverage AGC amplifier enhances the camera sensitivity.
- Has output effective for image making such as : Iris adjustment output and High brightness detection output.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	600	mW (QFP)
		950*	mW (VQFP)

*When mounted on the glass epoxy board 40 mm x 40 mm t = 0.8 mm

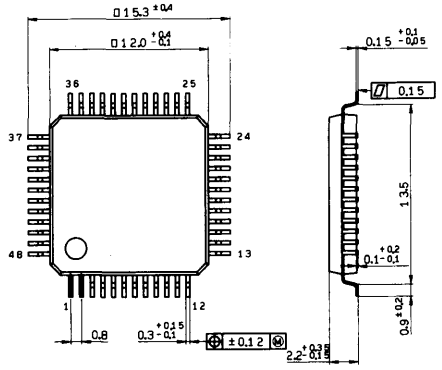
Recommended Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V

Package Outline

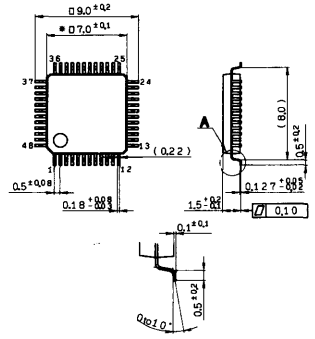
Unit: mm

CXA1337Q-Z 48 pin QFP (Plastic)



QFP-48P-L04

CXA1337R 48 pin VQFP (Plastic)

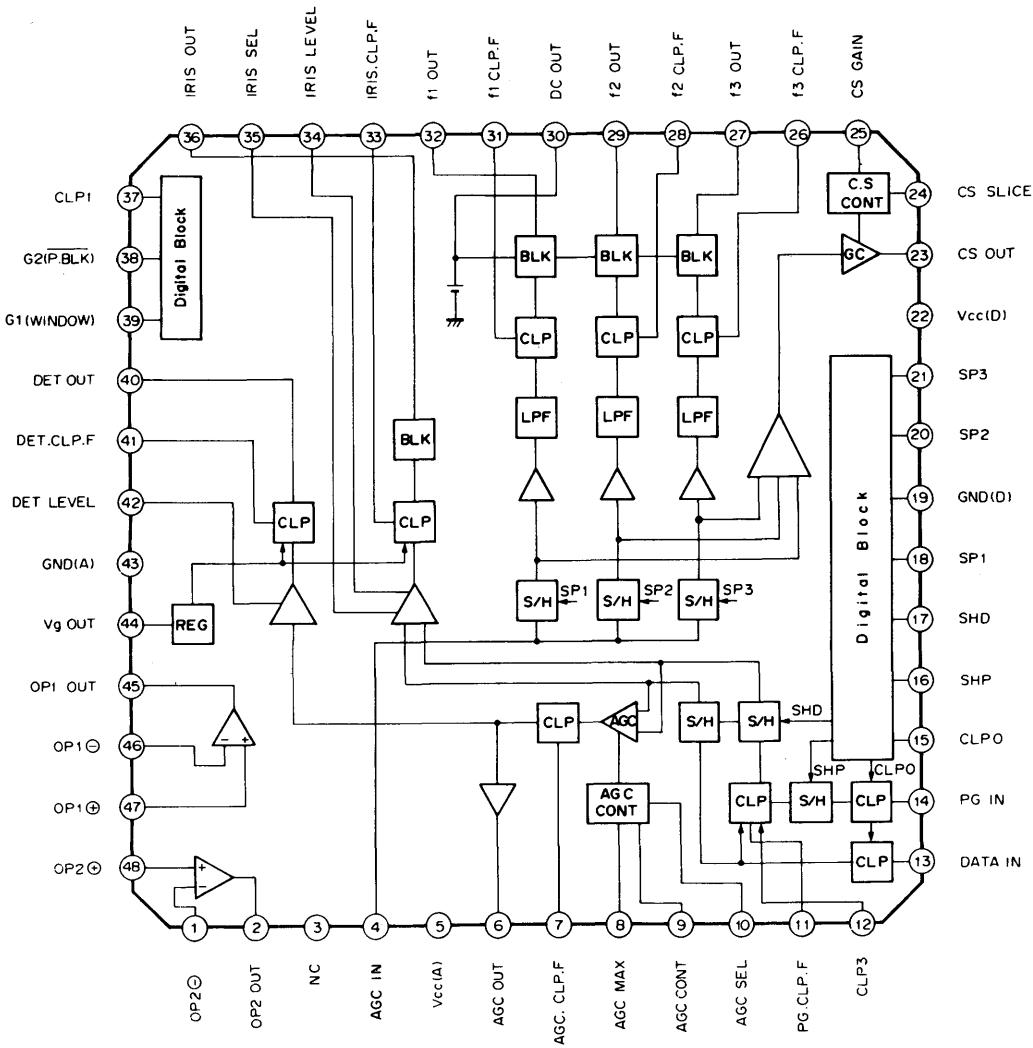


Detailed diagram of A.
Note) Dimension with * mark shows the status without residual resin.

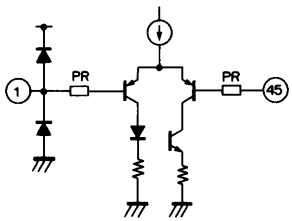
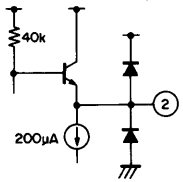
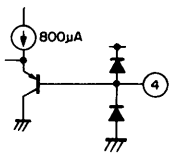
VQFP-48P-L04

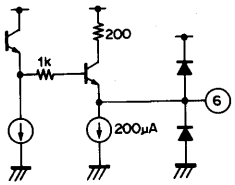
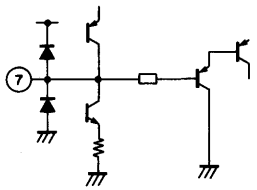
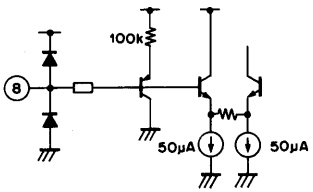
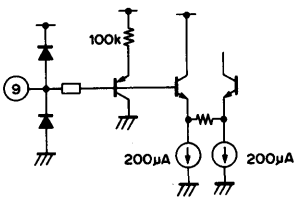
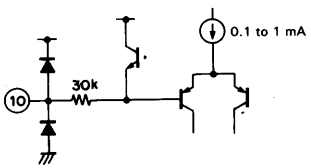
80502-YA

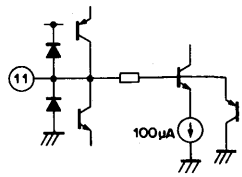
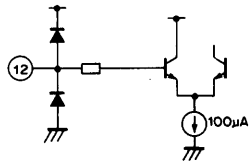
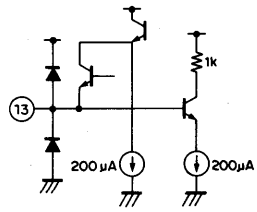
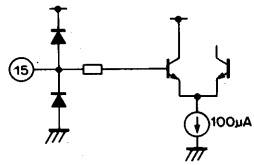
Pin Description

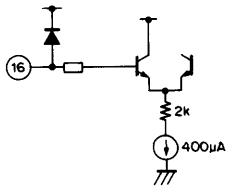
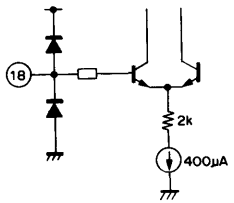


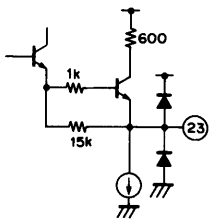
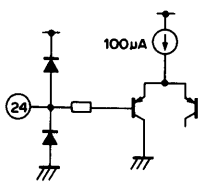
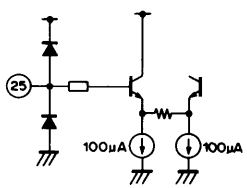
Pin Description and Equivalent Circuit (Vcc = 5V)

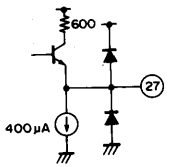
No.	Symbol	Standard DC	Equivalent Circuit	Description
1	OP2 ⊖	0.7 to 3.5V		Inverted operational. amplifier input.
2	OP2 OUT	1 to 4V		Operational amplifier output.
3	N.C.			
4	AGC IN	1.8 V		Color separation input
5	Vcc (A)	5V		Power supply for analog signal processing.

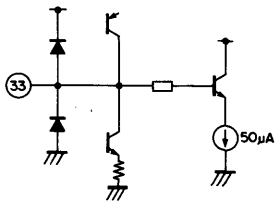
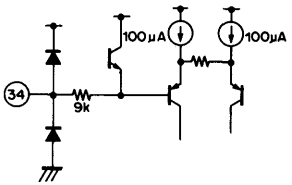
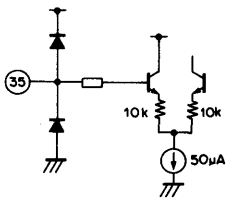
No.	Symbol	Standard DC	Equivalent Circuit	Description
6	AGC OUT	1.8V		AGC amplifier output
7	AGC.CLP.F	2.3V		Connecting pin for the AGC clamping capacitor.
8	AGC.MAX	2 to 4V		Maximum gain control pin for AGC amplifier.
9	AGC CONT	2 to 4V		Gain control pin for AGC amplifier.
10	AGC SEL	0 to 5V		Gain control range shifting pin for the AGC amplifier H: 4V or more, high gain mode L: 1V or less, low gain mode

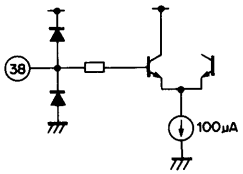
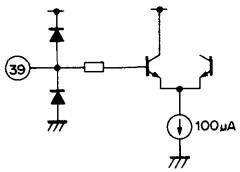
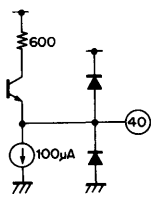
No.	Symbol	Standard DC	Equivalent Circuit	Description
11	PG.CLP.F	3.3V		Pin connecting the CLP 3 clamping circuit capacitor.
12	CLP3	—		CLP 3 pulse input (active H) H: 3V or more L: 2V or less
13	DATA IN	3.3V		CCD signal input
14	PG IN	3.3V	Same as pin 13 (DATA IN)	CCD signal input
15	CLP0	—		CLP 0 pulse input (active H) H: 3V or more L: 2V or less

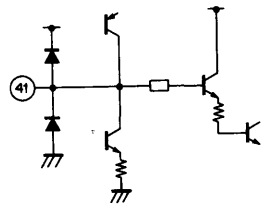
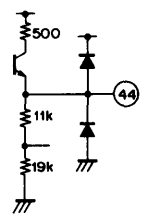
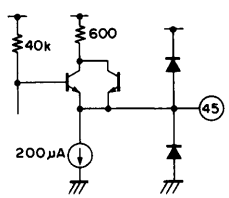
No.	Symbol	Standard DC	Equivalent Circuit	Description
16	SHP	—		SHP pulse input (active H) H: 3V or more L: 2V or less
17	SHD	—	Same as pin 16 (SHP)	SP1 pulse input (active H) H: 3V or more L: 2V or less
18	SP1	—		SP 1 pulse input (active H) H: 3V or more L: 2V or less
19	GND(D)	GND		Ground for digital (pulse) block
20	SP2	—	Same as pin 18 (SPI)	SP2 pulse input (active H) H: 3V or more L: 2V or less

No.	Symbol	Standard DC	Equivalent Circuit	Description
21	SP3	—	Same as pin 18 (SPI)	SP3 pulse input (active H) H: 3V or more L: 2V or less
22	Vcc(D)	5V		Power supply for digital (pulse) block.
23	CS.OUT	2.1V		High brightness detection output.
24	CS.SLICE	1.8 to 3.3V		Level adjustment pin for high brightness detection.
25	CS.GAIN	2 to 4V		Output level adjustment pin for high brightness detection.

No.	Symbol	Standard DC	Equivalent Circuit	Description
26	f_3 CLP.F	1.4V	Same as pin 7 (AGC.CLP.F)	Pin connecting the f_3 output clamping capacitor.
27	f_3 OUT	1.9V		f_3 output (signal output from AGC output, sample-hold and color separated at SP3.)
28	f_2 CLP.F	1.4V	Same as pin 7 (AGC.CLP.F)	Pin connecting the f_2 output clamping capacitor.
29	f_2 OUT	1.9V	Same as pin 27 (f_3 OUT)	f_2 output (signal output from AGC output, sample-hold and color separated at SP2.)
30	DC OUT	1.9V	Same as pin 27 (f_3 OUT)	Black level DC output of f_1, f_2 and f_3 outputs.

No.	Symbol	Standard DC	Equivalent Circuit	Description
31	f_1 CLP.F	1.4V	Same as pin 7 (AGC.CLP.F)	Pin connecting the f_1 output clamping capacitor.
32	f_1 OUT	1.9V	Same as pin 27 (f_3 OUT)	f_1 output (signal output from AGC output, sample-hold and color separated at SP1.)
33	IRIS.CLP.F	3.3V		Pin connecting the iris output clamping capacitor.
34	IRIS.LEVEL	1 to 3V		Iris output gain control pin (effective only when G_1 (pin 39) is L level.)
35	IRIS SEL	0 to 5V		Gain control range shifting pin for iris output. H: 4 V or more, High gain mode L: 1 V or less, Low gain mode

No.	Symbol	Standard DC	Equivalent Circuit	Description
36	IRIS OUT	1.9V	Same as pin 27 (f_3 OUT)	Iris output (iris control signal output)
37	CLP1	—	Same as pin 12 (CLP3)	CLP pulse input (active H) H: 3V or more L: 2V or less
38	G2	—		Blanking pulse input (active L) H: 3V or more L: 2V or less
39	G1	—		Window pulse input (active L) H: 3V or more L: 2V or less
40	DET OUT	1.9V		Detection signal output for AGC loop formation (DET output)

No.	Symbol	Standard DC	Equivalent Circuit	Description
41	DET.CLP.F	3.3V		Pin connecting the detection input clamping capacitor.
42	DET LEVEL	1 to 3V	Same as pin 34 (IRIS LEVEL)	Detection output gain control pin (effective only when G1 (pin 39) is L level.)
43	GND(A)	GND		Ground for analog signal processing.
44	Vg OUT	3V		Regulator output Output current: +1mA (outgoing direction) −80μA (incoming direction)
45	OP1 OUT	1 to 4V		Operational amplifier output

No.	Symbol	Standard DC	Equivalent Circuit	Description
46	CP1 ⊖	0.7 to 3.5V	Same as pin 1 (OP2 ⊖)	Inverted operational amplifier input.
47	OP1 ⊕	0.7 to 3.5V	Refer to pin 1.	Non-inverted operational amplifier input
48	OP2 ⊕	0.7 to 3.5V	Refer to pin 1.	Non-inverted operation amplifier input.

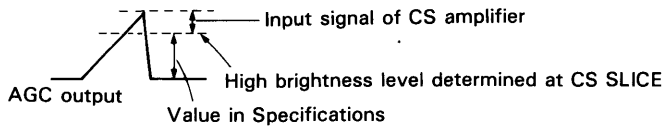
Electrical Characteristics

Vcc = 5V, Ta = 25°C

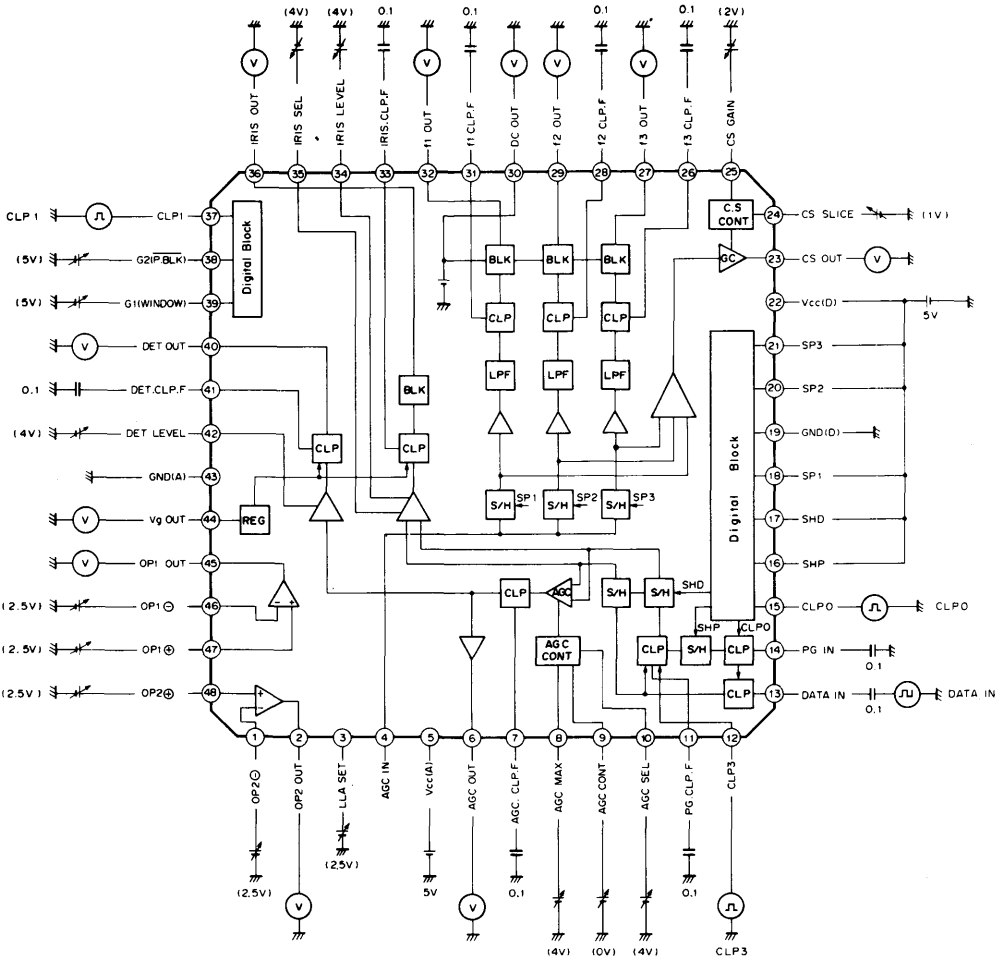
Item	Rate value	Test condition	Min.	Typ.	Max.	Unit
Power consumption	ID		45	60	75	mA
AGC amplifier		AGC OUT/DATA IN				
Gain control	ACONT Min.	AGC CONT = 2V, AGC.MAX = 4V, AGC SEL = 4V	0.5	2	3.5	dB
	ACONT Max.	AGC CONT = 4V, AGC.MAX = 4V, AGC SEL = 4V	28	30	32	dB
Maximum gain control	AMAX Min.	AGC CONT = 4V, AGC.MAX = 2V, AGC SEL = 4V	13.5	15.5	17.5	dB
Low gain mode	AG LOW	AGC CONT = 3V, AGC.MAX = 4V, AGC SEL = 2V	10.7	12.7	14.7	dB
Fixed gain mode	ACONT F	AGC CONT = 0V, AGC.MAX = 4V, AGC SEL = 4V	4.5	6.5	8.5	dB
Fixed maximum gain mode	AMAX F	AGC CONT = 4V, AGC.MAX = 0V, AGC SEL = 4V	19.5	21.5	23.5	dB
Color separator		f1 output/AGC output				
f1 channel gain	f1 G		−1.8	−1	−0.2	dB
Matching between channels	Δf	f2 output/f1 output and f3 output/f1 output	−0.6	0	+0.6	dB
DC OUT	DC	Output voltage at DC OUTPUT (30-pin)	1.8	1.9	2.0	V
Iris amplifier		Iris output/DATA IN				
Window control	IR Min.	IRIS LEVEL = 1V, G1 = 0V, G2 = 5V, IRIS SEL = 4V			−30	dB
	IR Max.	IRIS LEVEL = 4V, G1 = 0V, G2 = 5V, IRIS SEL = 4V	4	5.5	7.0	dB
Low gain mode	IR LOW	IRIS LEVEL = 4V, G1 = 0V, G2 = 5V, IRIS SEL = 1V	−0.7	0.3	1.3	dB
Clamp voltage	IR DC		1.8	1.9	2.0	V
Maximum output level	IR MAX		1.5			V

Item		Rate value	Test condition	Min.	Typ.	Max.	Unit
Detection amplifier			Detection output/AGC output				
Window control		DET Min	DET LEVEL = 1V, G1 = 0V, G2 = 5V			−30	dB
		DET Max	DET LEVEL = 4V, G1 = 0V, G2 = 5V	−1.5	0	+1.5	dB
Clamp voltage		DET DC		1.8	1.9	2.0	V
Maximum output level		DET Max.		1.4			V
CS amplifier			CS output/AGC output				
Gain control		C CONT Min.	CS GAIN = 2V, CS SLICE = 1V	−5	−3.5	−2	dB
		C CONT Max.	CS GAIN = 4V, CS SLICE = 1V	5.5	7.5	9.5	dB
High brightness detection level (slice control)		SLICE	Detection level calculated as AGC output with 2.5 V CS slice.*	410	570	730	mV
Operational amplifier			Maximum output with no load, OP1 ⊕ − OP1 ⊖ ≧ 10 mV				
OP1	high level	OP1 H		4.1			V
	low level	OP1 L	Minimum output with no load, OP1 ⊕ − OP1 ⊖ ≦ −10 mV	0.9	1.0	1.1	V
OP2	high level	OP2 H	Maximum output with no load, OP2 ⊕ − OP2 ⊖ ≧ 10 mV	4			V
	low level	OP2 L	Minimum output with no load, OP2 ⊕ − OP2 ⊖ ≦ −10 mV			1.1	V
Vg OUT		VG	Regulator output with no load	2.9	3.0	3.1	V
ΔVg		ΔVG	Regulator output variation when Vcc varies from 5V to 4.5V with no load.	−60	−30	0	mV

***Note)** Voltage between the black level of the AGC output (main line signal) and the high brightness level determined by the voltage at CS SLICE pin.

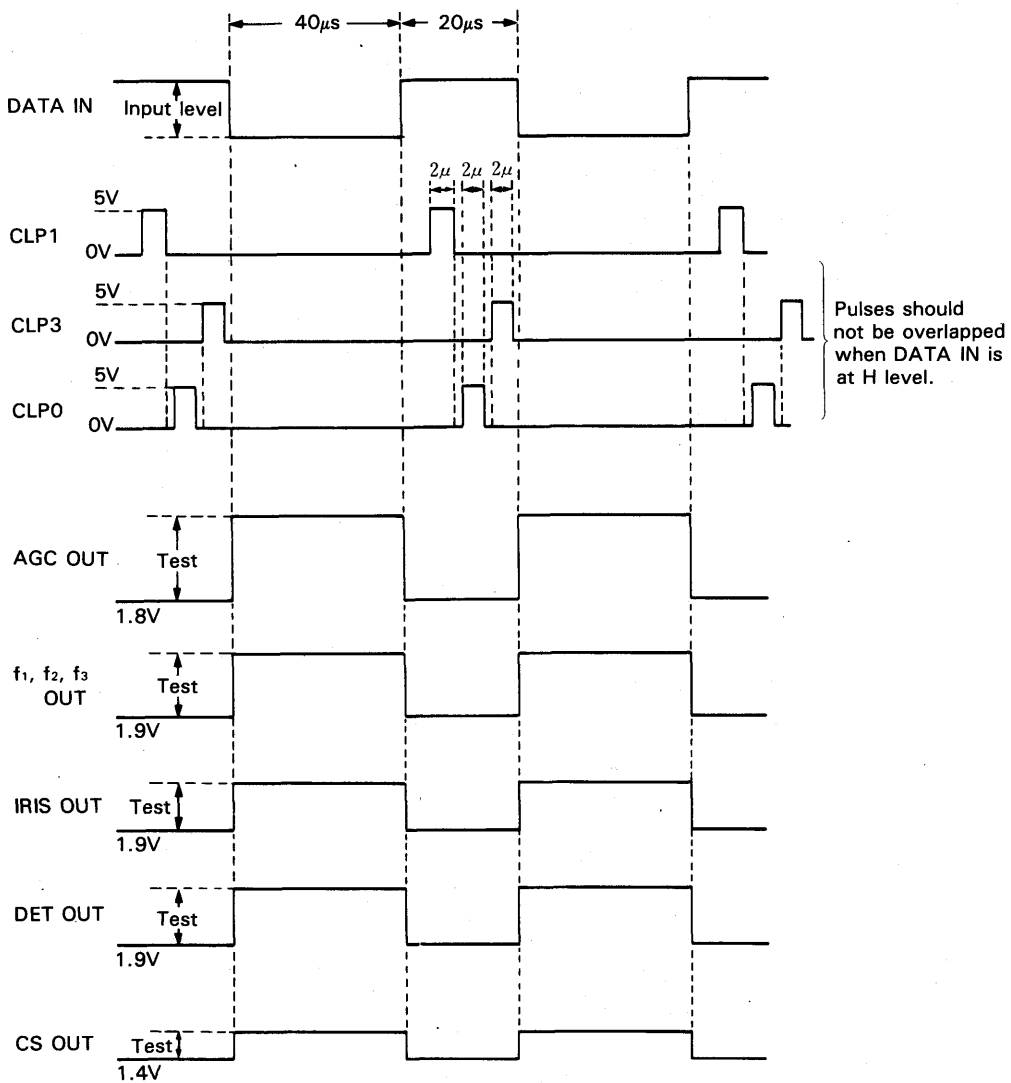


Electrical Characteristics Test Circuit

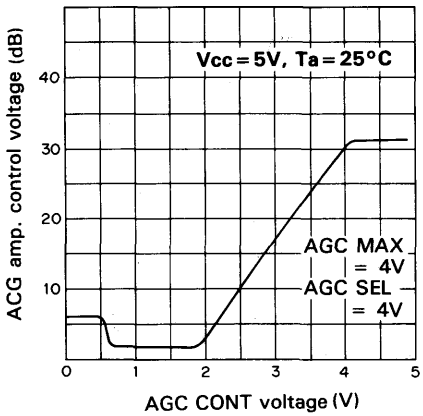


***Note)** 1. The capacitor unit value is μF.
2. Voltages in parentheses are those not specified in "Test condition" of the Electrical Characteristics.
3. Ⓥ indicates a test pin. (Test of AC and DC voltages)

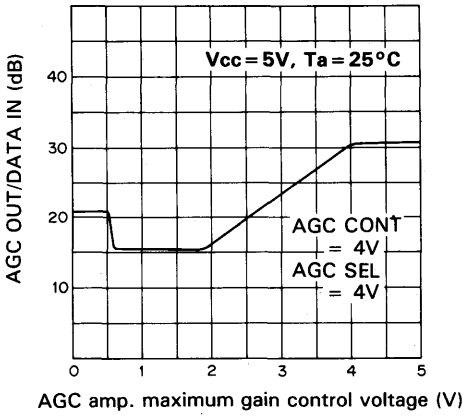
I/O Waveform for the Electrical Characteristics Test Circuit



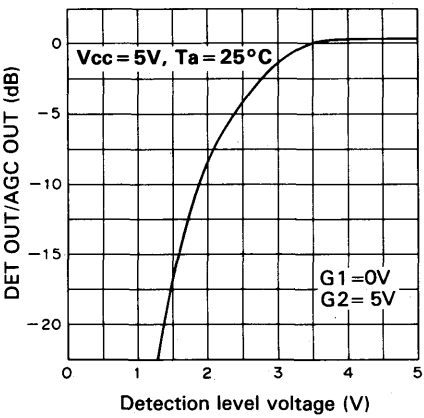
ACG Amplifier gain control characteristics



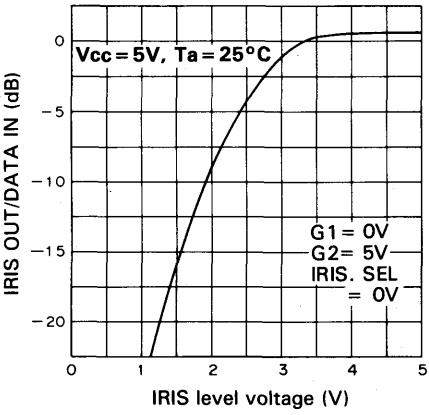
AGC Amplifier maximum gain control characteristics



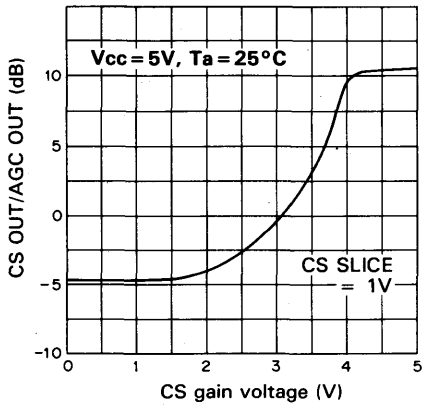
Detection amplifier window control characteristics

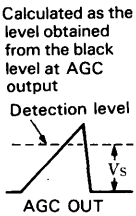


Iris amplifier window control characteristics (low gain mode)

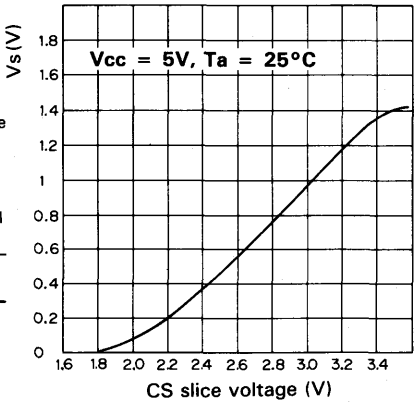


CS amplifier gain control characteristics

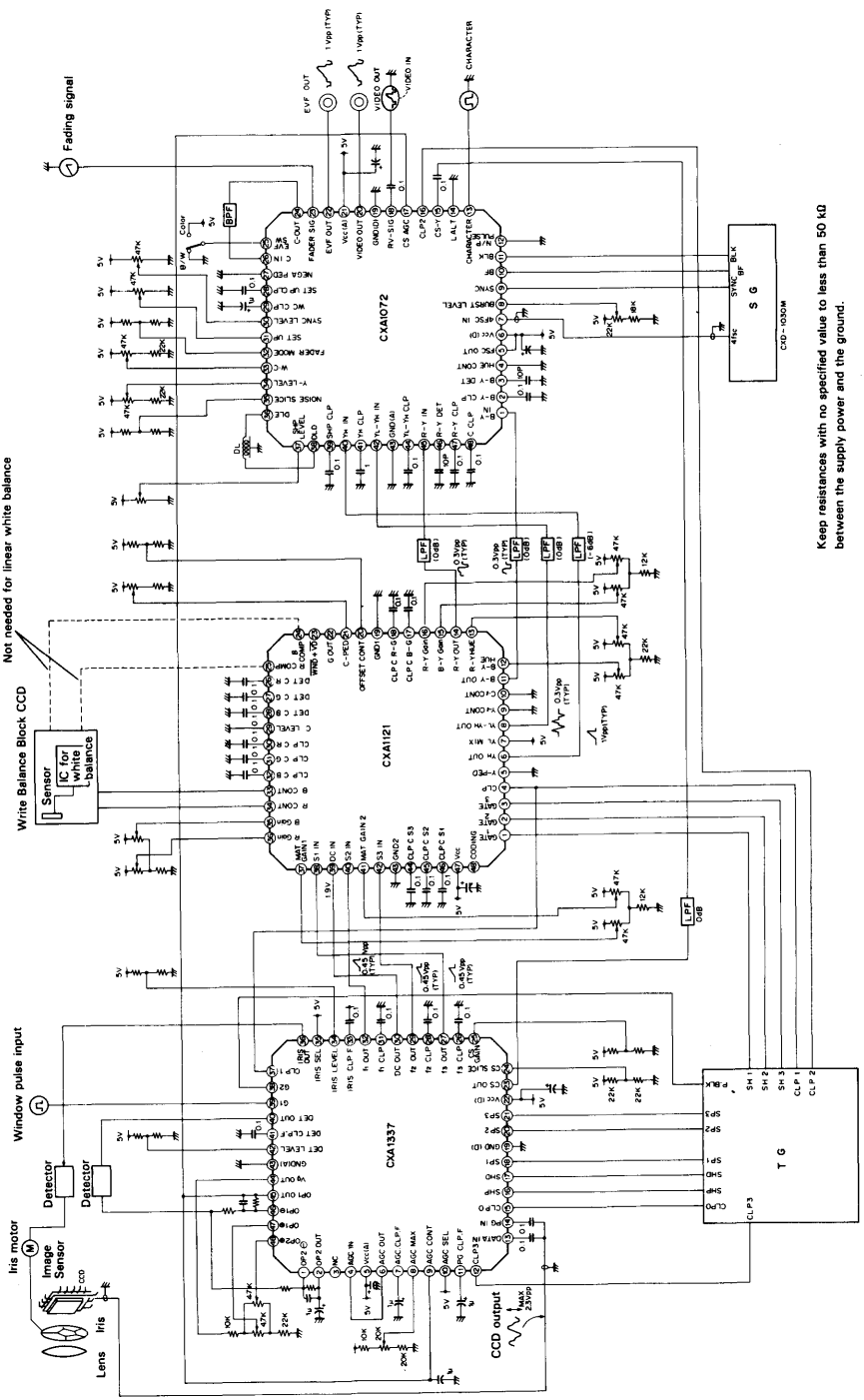




CS Amplifier slice control characteristics (high brightness detection level)



760 H Complementary Color Stripe CCD Video Camera System



SONY

CXA1338Q-Z/R

CCD Camera Matrix

Description

CXA1338Q-Z and CXA1338R are matrix ICs for CCD cameras and are used for the system with complementary color checkers coding imager ICX026AK. They perform the vertical correlation process by using 1HDL and outputs the RGB signal from the magenta, green, yellow, and cyan input signals.

Features

- Excellent color reproduction as a result of the primary color separation system.
- Two modes are provided for the matrix factor ; PRESET and CONTROL.
- The aperture signal in the V direction is output.
- The chroma suppress signal is output.
- The Y_H and Y_L-Y_H signals are output.

Structure

Bipolar silicon monolithic IC

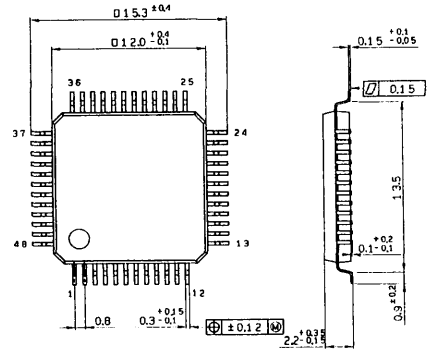
Application

- Complementary color checkers CCD color camera

Package Outline

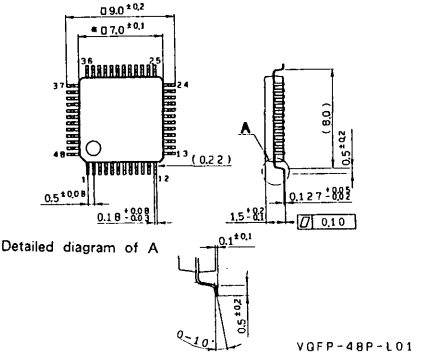
Unit : mm

CXA1338Q-Z 48 pin QFP (Plastic)



QFP-48P-L04

CXA1338R 48 pin VQFP (Plastic)



VQFP-48P-L01

Note) Dimensions marked with * does not include residual resin.

Absolute Maximum Ratings (Ta=25℃)

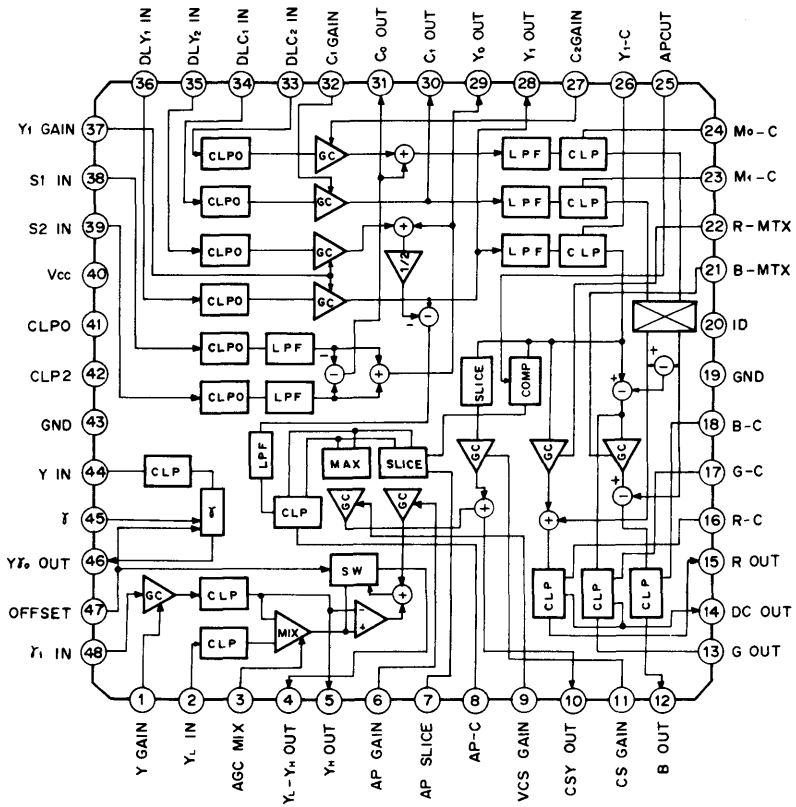
• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−55 to +150	℃
• Operating temperature	Topr	−20 to +75	℃
• Allowable power dissipation	P_D	600	mW

Recommended Operating Condition

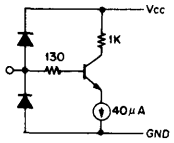
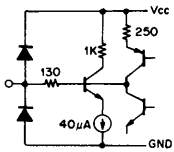
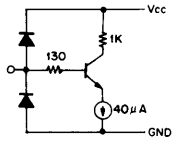
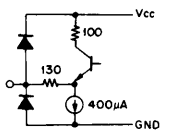
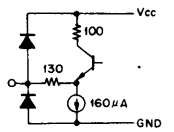
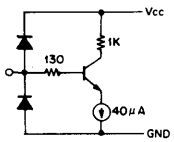
• Supply voltage	Vcc	4.75 to 5.25	V

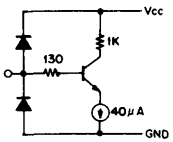
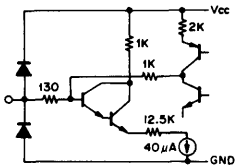
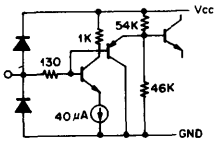
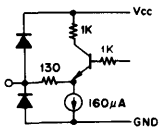
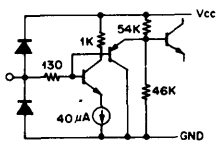
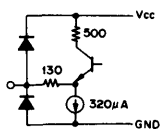
80712-ST

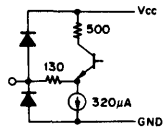
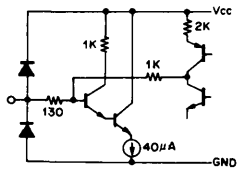
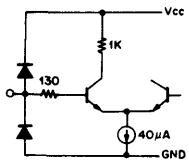
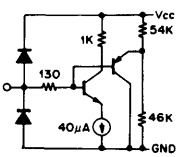
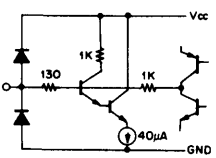
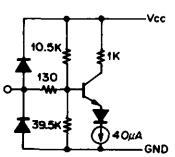
Block Diagram and Pin Configuration

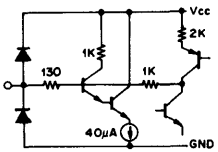
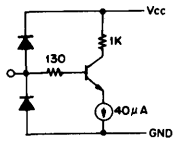
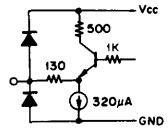
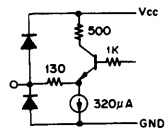
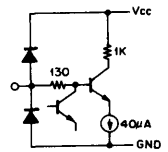
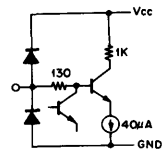
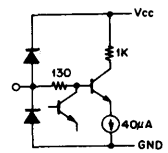


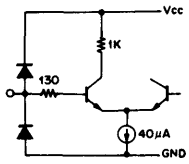
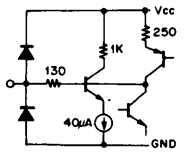
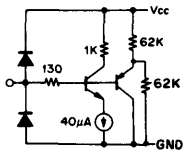
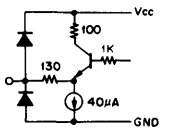
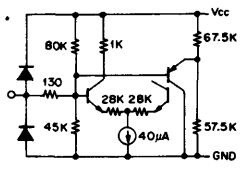
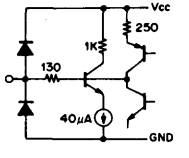
Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	Y GAIN	3.0V		Gain control pin for the signal input to Y $_{Y}$ 1IN. 1.8V (Min.) to 5.0V (Max.)
2	Y_L IN	3.4V		Y_L input, which is clamped by the input connected to the capacitor. 250mV (Typ.)
3	AGC MIX	3.0V		Y_M factor (Y_L/Y_H ratio) control. 3.0V (Y_L) to 4.0V (Y_H)
4	Y_L-Y_H OUT	2.9V		Y_L-Y_H signal and V aperture signal output pin. Black level 3V. If the 47 pin OFFSET pin is set to GND in test mode, Y_M signal (that has mixed Y_L and Y_H) is output.
5	Y_H OUT	2.2V		Y_H output. 1000mV (Typ.), 1300mV (Max.) Black level 2.4V
6	AP GAIN	3V		V aperture gain control. 1.8V (Max.) to 5.00V (OFF)

No.	Symbol	Voltage	Equivalent circuit	Description
7	AP SLICE	3V		V aperture slice level control. 1.8V (Min.) to 5.0V (Max.)
8	AP-C	3.7V		Pin that connects the V aperture signal capacitor CLP capacitor.
9	VCS GAIN	3V		Chroma suppress signal level control with V aperture. 1.8V (Min.) to 5.0V (Max.) GND : OFF
10	CSY OUT	2.1V		Chroma suppress signal output.
11	CS GAIN	3V		Chroma suppress signal level control with Y signal. 1.8V (Min.) to 5.0V (Max.) GND : OFF
12 13 15	B OUT G OUT R OUT	1.9V 1.9V 1.9V		R, G, B output pin. Black level 1.9V. If the 21-pin B MTX pin is set to GND in test mode, each pin outputs a signal as shown below. R OUT ··· C_R signal B OUT ··· C_B signal G OUT ··· Y signal The C_R, C_B, and Y signal are provided before the matrix.

No.	Symbol	Voltage	Equivalent circuit	Description
14	DC OUT	1.9V		DC output of 1.9V that is equivalent to R, G, B OUT black level.
16 17 18	R-C G-C B-C	3.2V 3.3V 3.3V		Pin that is connected to the R, G, B OUT clamping capacitor.
19	GND	0V		
20	ID			Inverted pulse is input every 1H. The C1 signal is output to B OUT for HI. The C1 signal is output to R OUT for LOW. V_{TH} = 2.5V
21 22	B MTX R MTX	3V 0V		Matrix factor control for B and R. 1.8V (Max.) to 3.9V (Min.) In test mode : B MTX : C_R/C_B mode with GND R MTX : MTX preset mode with GND
23 24	M_1-C M_0-C	3.0V 3.0V		M_1-C : Connects the 1H line chroma signal clamping capacitor. M_0-C : Connects the 0H/2H line chroma signal clamping capacitor.
25	APCUT	3.95V		Controls the level that suppresses the V aperture signal. Internally biased to 3.95V in preset mode.

No.	Symbol	Voltage	Equivalent circuit	Description
26	Y_1-C	3.0V		Pin that connects the 1H line Y signal clamping capacitor.
27 32 37	C_2- GAIN C_1- GAIN Y_1- GAIN	3V 3V 3V		C_1, C_2, Y_1 signal gain control. 1.8V (Min.) to 5.0V (Max.)
28 29	Y_1 OUT Y_0 OUT	2.6V 2.6V		1H/0H line Y signal output. Inverted output 200mV (Typ.)
30 31	C_1 OUT C_0 OUT	2.6V 2.6V		1H/0H line chroma signal output. Inverted output ± 100mV (Typ.)
33 34	DLC_2 IN DLC_1 IN	2.9V 2.9V		2H/1H line chroma signal input. Positive phase input ± 75mV (Typ.)
35 36	DLY_2 IN DLY_1 IN	2.9V 2.9V		2H/1H line Y signal input. Positive phase input 150mV (Typ.)
38 39	S_1 IN S_2 IN	3.3V 3.3V		S_1/S_2 signal input. 500mV (Typ.) 1500mV (Max.)

No.	Symbol	Voltage	Equivalent circuit	Description
40	Vcc	5V		Vcc
41 42	CLP0 CLP2	5V 0V 5V 0V		Clamp pulse input VTH = 2.5V
43	GND	0V		GND
44	Y IN	2.7V		Y signal input. 220mV (Typ.) 660mV (Max.)
45	γ	0V		γ curve control. 1.8V to 5.0V GND : Preset
46	Yγo OUT	3.0V		Yγ signal output. Inverted output 400mV (Typ.) 520mV (Max.)
47	OFFSET	1.8V		γ offset control. 1.8V to 5.0V If the pin is set to OPEN, bias to 1.8V is internally performed. If the pin is set to GND in test mode, the YM signal is output from the 4 pin, YL-YH OUT pin.
48	Yγ1 IN	2.9V		1H line Yγ signal output. 150mV (Typ.)

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	Vcc=5V	20	33	45	mA
S_1, S_2 LPF	$F_{S1, S2}$	4.77MHz gain for ㊳ S_1 IN→㉙ Y_O OUT 300kHz	−28	−20	−11	dB
S_1-Y_O gain	$G_{S1\text{-}YO}$	㊳ S_1IN→ ㉙ Y_O OUT gain	−14.2	−13.0	−11.8	dB
Gain difference between S_1 -Y_O and S_2-Y_O	Δ G_{YO}	Gain difference between ㊳ S_1 IN→㉙ Y_OOUT and ㊴ S_2IN→ ㉙ Y_OOUT	−0.7	0	0.7	dB
S_1-C_O gain	$G_{S1\text{-}SO}$	㊳ S_1 IN→㉛ C_OOUT gain	−3.2	−1.9	−0.8	dB
Gain difference between S_1-C_O and S_2-C_O	Δ G_{CO}	Gain difference between ㊳ S_1 IN→ ㉛ C_OOUT and ㊴ S_2IN→㉛ C_OOUT	−0.7	0	0.7	dB
Y_1 gain Min.	G_{Y1}Min.	㊱ DLY_1 IN→㉘ Y_1 OUT gain ㉗ Y_1 GAIN=1.8V	−	−2.5	−1.3	dB
Y_1 gain Max.	G_{Y1}Max.	㊱ DLY_1 IN→㉘ Y_1 OUT gain ㉗ Y_1 GAIN=5V	8.8	12.0	−	dB
C_1 gain Min.	G_{C1} Min.	㉞ DLC_1 IN→㉚ C_1 OUT gain ㉜ C_1 GAIN=1.8V	−	−2.5	−1.3	dB
C_1 gain Max.	G_{C1} Max.	㉞ DLC_1 IN→㉚ C_1 OUT gain ㉜ C_1 GAIN=5V	8.8	12.0	−	dB
C_2 gain Min.	G_{C2} Min.	㉞ DLC_1 IN→⑮ ROUT GAIN that is twice as much as ㉝ DLC2IN →⑮ ROUT, ㉑ BMTX=GND, ⑳ ID=GND, ㉗ C_2GAIN=1.8V for ㉑ BMTX=GND, ID=5V⑳	−	−2.8	−1.3	dB
C_2 gain Max.	G_{C2} Max.	㉞ DLC_1 IN→⑮ ROUT Gain that is twice as much as ㉝ DLC_2 IN →⑮ ROUT, ㉑ BMTX=GND, ⑳ ID=GND, ㉗ C_2GAIN=1.8V for ㉑ BMTX=GND, ⑳ ID=5V	8.8	12.0	−	dB
Y_2 gain Min.	G_{Y2}Min.	Ratio of the output of ㉟ DLY_2 IN· (200mV) →④ Y_L-Y_HOUT, ㊲ Y_1 GAIN=1.8V to the output of ㊱ DLY_1 IN (100mV) → ④ Y_L-Y_HOUT, ㊲ Y1GAIN=1.8V	−1.4	0	1.4	dB
Y_2 gain HI	G_{Y2}Max.	Ratio of the output of ㉟ DLY_2 IN (100mV) →④ Y_L-Y_HOUT, ㊲ Y_1 GAIN=1.8V to the output of ㊱ DLY_1 IN (50mV) → ④ Y_L-Y_HOUT, ㊲ Y GAIN=3.9V	−1.4	0	1.4	dB
C_O LPF	F_{CO}	4.77MHz gain for ㉝ DLC_2IN→⑮ ROUT, ⑳ ID=GND, 300kHz	−28	−18	−8	dB
C_1 LPF	F_{C1}	4.77MHz gain for ㉞ DLC_2IN→⑮ ROUT, ⑳ ID=5V, 300kHz	−28	−18	−8	dB

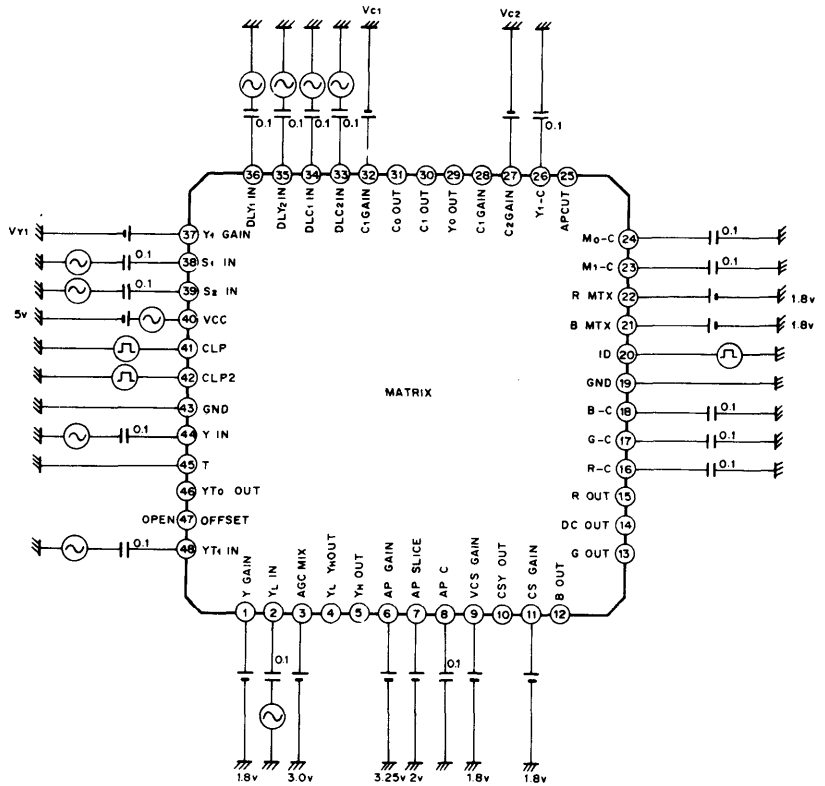
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Y_1 LPF	F_{Y1}	4.77MHz gain for ㊱ DLY1 IN→⑬ GOUT, 300kHz	−28	−18	−8	dB
V apperture LPF	F_{AP}	4.77MHz gain for ㊱ DLY_1 IN→ ④ Y_L-Y_H OUT, 300kHz	−28	−18	−8	dB
DLY_1 → Y_L-Y_H gain	G_{DLY1}	㊱ DLY1 IN (100mV) →④ Y_L-Y_H OUT gain ⑥ APGAIN=3.25V	6	8.3	11	dB
V aperture level Max.	G_{AP}Max.	㊱ DLY1 IN (30mV) →④ Y_L-Y_HOUT Output level ratio for ⑥ APGAIN=3.25V to 1.5V	8	11	−	dB
V aperture slice Mid.	V_{APS} Mid.	㊱ DLY1 IN (100mV) →④ Y_L-Y_H OUT Output level difference between ⑦ APSLICE=2V and 3V	85	120	155	mV
V aperture cutting input level	V_{APCUT}	㊱ DLY1 IN input level when the ④ Y_L-Y_HOUT output is cut ⑥ APGAIN=1.5V	225	260	295	mV
Chroma suppress Y output level Max.	V_{CSY} Max.	㊱ DLY1 IN (350mV) →⑩ CSYOUT ⑨ VCSGAIN=GND, ⑪ CSGAIN=1.8V	400	760	−	mV
Chroma suppress Y gain Min.	G_{CSY} Min.	㊱ DLY1 IN (350mV) →⑩ CSYOUT ⑨ VCSGAIN=GND Output level ratio for ⑪ CSGAIN=5V to 1.8V	−14.2	−12.0	−10.8	dB
Chroma suppress VAP level Max.	V_{CSVAP} Max.	㊱ DLY1 IN (50mV) →⑩ CSYOUT ⑪ CSGAIN=GND, ④ VCSGAIN=5V	740	920	−	mV
Chroma suppress VAP gain Min.	G_{CSVAPM} Min.	㊱ DLY1 IN (50mV) →⑩ CSYOUT ⑪ CSGAIN=GND Output level ratio for ⑨ VCSGAIN=5V to 1.8V	−14.2	−12.0	−9.3	dB
C_R gain	G_{CR}	㉞ DLC1 IN→⑮ ROUT gain ㉒ RMTX=GND	3.6	5.3	7.0	dB
RMTX Y factor presetting	K_{RY}	㉞ DLC1 IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY IN (220mV) →⑮ ROUT, ⑳ ID=5V ㉑ RMTX=GND output level set to V_2 (V_2/V_1) ×1/8 is calculated.	0.094	0.12	0.131	V/V
C_B gain	G_{CB}	㉞ DLC1 IN→⑫ BOUT gain ⑳ ID=GND, ㉒ RMTX=GND	3.6	5.3	7.0	dB
BMTX Y factor presetting	K_{BY}	㉞ DLC1 IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㊱ DLY_1 IN (220mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_2 (V_2/V_1) ×1/8 is calculated.	0.173	0.20	0.222	V/V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BMTX C_R factor	K_{BCR}	㉞ DLC1IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㉞ DLC1IN (100mV) →⑫ BOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_2 V_2/V_1	0.173	0.20	0.222	V/V
Y_1 gain	G_{Y1}	㊱ DLY1 IN→⑬ GOUT gain ⑳ ID=5V, ㉒ RMTX=GND	6.6	8.3	10.0	dB
GMTX C_R factor	K_{GCR}	㊱ DLY1 IN (220mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㉞ DLC1IN (100mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_2 $V_2/V_1 \times 8$	0.78	1.0	1.22	V/V
GMTX C_B factor	K_{GCB}	㊱ DLY1IN (220mV) →⑬ GOUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㉞ DLC1IN (100mV) →⑬ GOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_2 $V_2/V_1 \times 8$	0.78	1.0	1.22	V/V
RMTX Y factor HI	K_{RYMI}	㉞ DLC1IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) ⑮ ROUT, ⑳ ID=5V ㉒ RMTX=1.8V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.192	0.225	0.253	V/V
BMTX Y factor LOW	K_{RYLO}	㉞ DLC1IN (100mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) →⑮ ROUT, ⑳ ID=5V ㉒ RMTX=3.9V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.042	0.056	0.070	V/V
BMTX Y factor HI	K_{BYMI}	㉞ DLC1 IN (100mV) →⑫ BOUT, ⑳ ID=GMD ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) →⑫ BOUT, ⑳ ID=GND ㉑ BMTX=1.8V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.337	0.380	0.413	V/V
RMTX Y factor LOW	K_{BYLO}	㉞ DLC1IN (100mV) →⑫ BOUT, ⑳ ID=GND ㉒ RMTX=GND output level set to V_1 ㊱ DLY1 IN (220mV) →⑫ BOUT ⑳ ID=GND ㉑ BMTX=3.9V output level set to V_2 $(V_2/V_1) \times 1/8$ is calculated.	0.068	0.09	0.117	V/V
DC OUT DC	Vcc	⑭ DCOUT pin voltage	1.73	1.85	1.97	V
R, G, B OUT offset	V_{RGBO}	Potential difference between ⑮ ROUT/ ⑬ GOUT, ⑫ BOUT and ⑭ DCOUT	−10	0	10	mV
γ preset standard level	$V_{\gamma PRE}$	㊹ YIN (220mV) →㊻ Y γ OUT	365	410	455	mV

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
γ preset curve	$G_{\gamma PPE}$	Ratio of ㊶ YIN (55mV) →㊻ Y γ OUT output level to ㊶ YIN (220mV) → ㊻ Y γ OUT output level	−8.2	−7.0	−5.8	dB
Y_HOUT DC	$V_{\gamma HOUT}$	⑤ Y_HOUT pin voltage	2.0	2.3	2.6	V
Y_H gain Min. (Y_HOUT)	G_{YH}Min1	㊽ Y γ1IN→⑤ Y_HOUT gain ① YGAIN=1.8V ③ AGCMIX=4V ㊼ OFFSET=GND	−	10	12.2	dB
Y_H gain Max. (Y_HOUT)	G_{YH}Max1	㊽ Y γ1IN→⑤ Y_HOUT gain ① YGAIN=5V ③ AGCMIX=4V ㊼ OFFSET=GND	20.8	23.0	−	dB
Y_L-Y_HOUT DC	V_{YL}OUT	Y_L-Y_H pin voltage	2.6	2.9	3.2	V
Y_H gain Min. (Y_L-Y_HOUT)	G_{YH}Min2	㊽ Y γ1IN→④ Y_L-Y_H OUT gain ① YGAIN=1.8V ③ AGCMIX=4V ㊼ OFFSET=GND	−	2.1	4.2	dB
Y_H gain Max. (Y_L-Y_HOUT)	G_{YH}Max2	㊽ Y γ1IN→④ Y_L-Y_H OUT gain ① YGAIN=5V ③ AGCMIX=4V ㊼ OFFSET=GND	12.8	15.0	−	dB
Y_L gain	G_{YL}	② Y_LIN→④ Y_L-Y_H OUT gain ③ AGCMIX=3V	4.3	6.0	7.7	dB

Electrical Characteristics Test Circuit

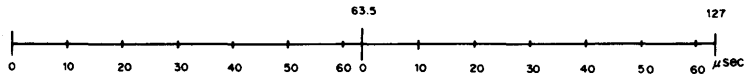
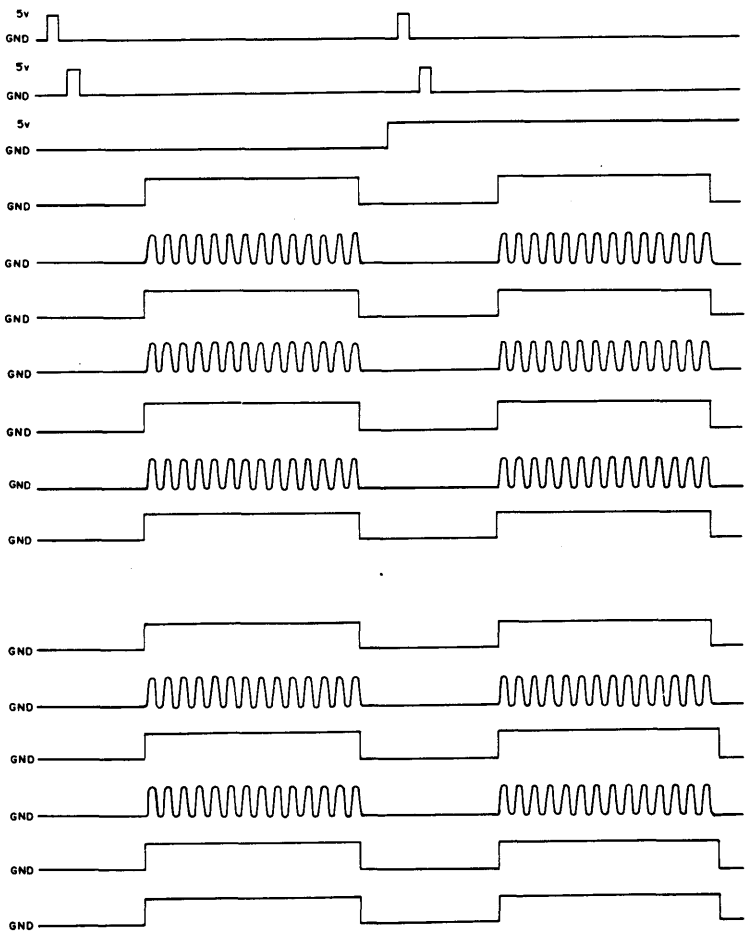
Standard setting conditions



Note)

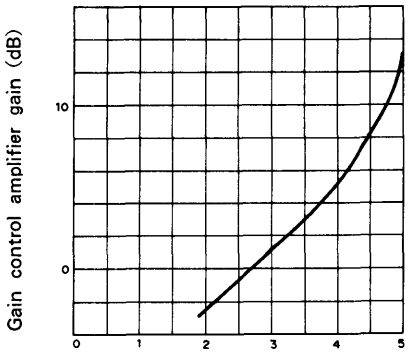
1. Conditions only that are different from standard setting conditions are described.
2. Adjust V_{C1}, V_{C2}, and V_{Y1} so that the signal levels will be equivalent between DLC_1IN and C_1OUT, DLC_2IN and between DLY_1IN and Y_1OUT.
3. Signal sources other than ID, CLP0, and CLP2 are not input in standard setting but set to GND.
4. If measurement conditions specify ID=5V and ID=GND, measure at the ID=5V timing and ID=GND timing.

Input Signal Timing Chart

Pin	Input signal
	
41 CLPO	
42 CLP2	
20 ID	
38 S_1 IN	
39 S_2 IN	
36 DLY_1 IN	
35 DLY_2 IN	
34 DLC_1 IN	
33 DLC_2 IN	
44 YIN	
48 Y_{Y1} IN	

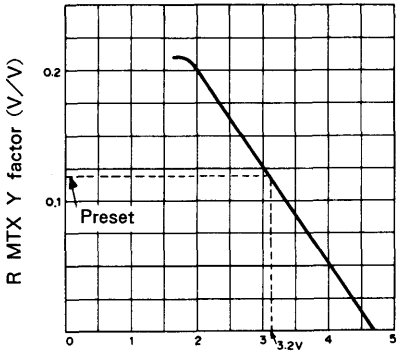
Note) 1. The signal level and frequency are listed in another table.
2. The sine wave intermittent signal is used for measurement of LPF characteristics .

Delay line gain control amplifier characteristics



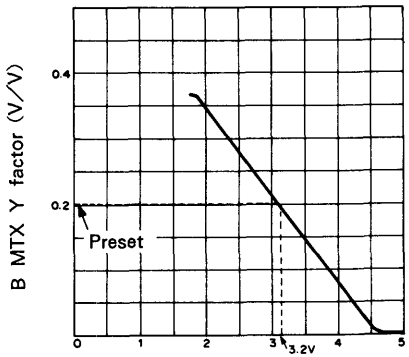
37, 32, 27 pins Y_1, C_1, C2GAIN pins (Y)

R MTX control characteristics (Y factor)



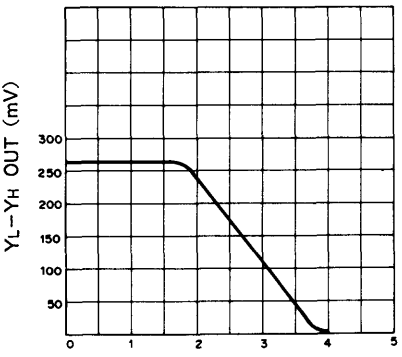
22 pin RMTX (V)

B MTX control characteristics (Y factor)



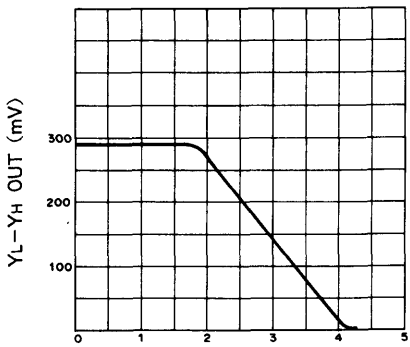
21 pin BMTX (V)

AP GAIN control characteristics



6 pin AP GAIN (V)

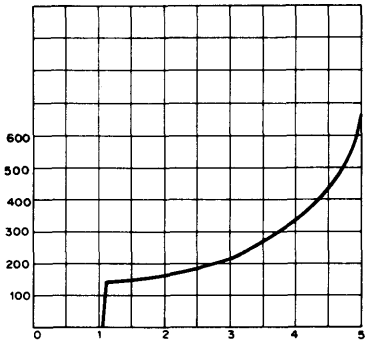
AP SLICE control characteristics



7 pin AP SLICE (V)

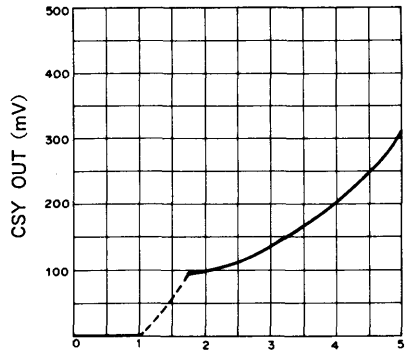
(6 pin AP GAIN=3.25V
Input pin 36 DLY1IN 100mV)

CSY GAIN control characteristics



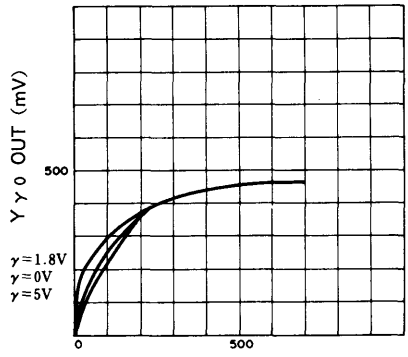
11 pin CS GAIN (V)
(Input pin 36 DLY1IN=350mV)

CSY VAP control characteristics



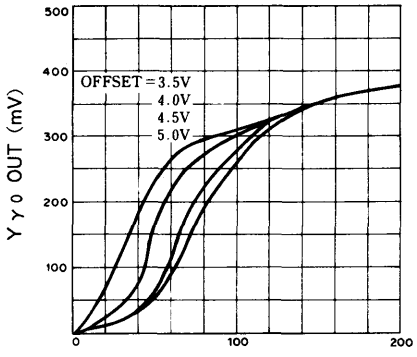
9 pin VCS GAIN pin (V) (Input pin 36 DLY1IN=50mV)

γ control characteristics



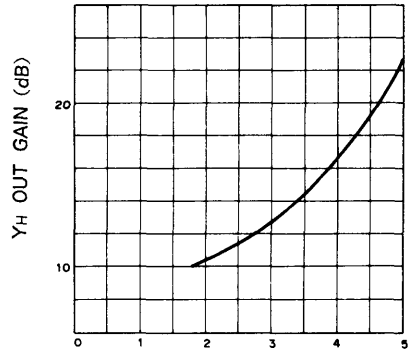
44 pin YIN input level (mV)

γ OFFSET control characteristics (γ = 1.8V)



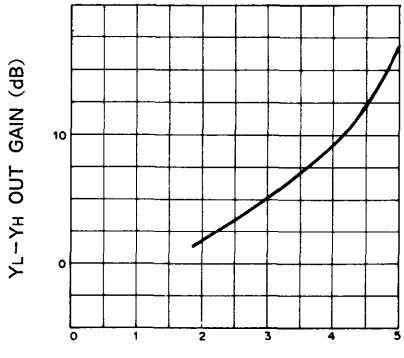
44 pin YIN input level (mV)

YH GAIN control characteristics



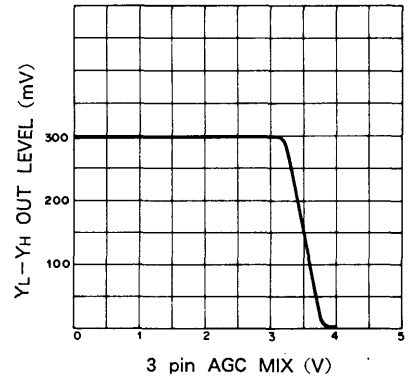
1 pin Y GAIN pin (V)

YM GAIN control characteristics



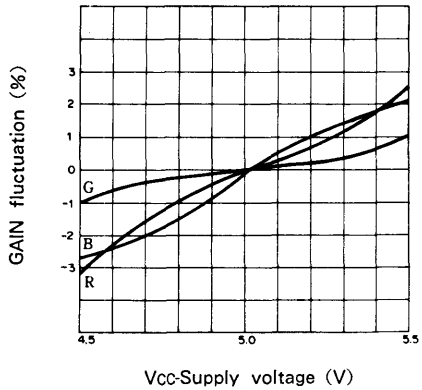
1 pin Y GAIN pin (V)

YL MIX control characteristics

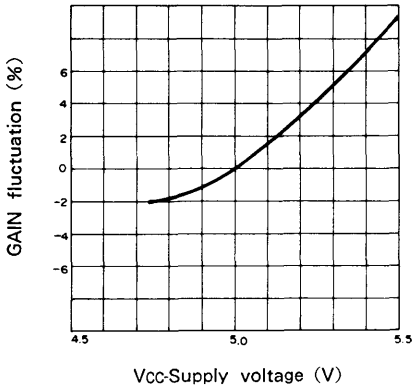


3 pin AGC MIX (V)

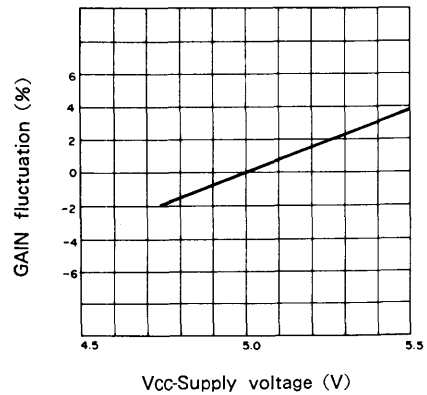
S1, S2, Y-R, G, B GAIN Vcc characteristics



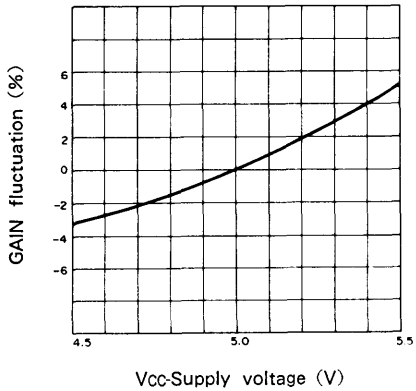
YIN – YH GAIN Vcc characteristics



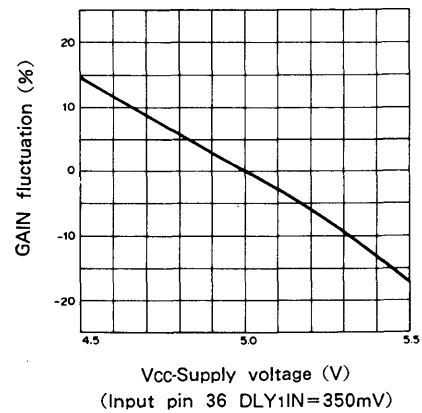
YIN – YL-YH GAIN Vcc characteristics



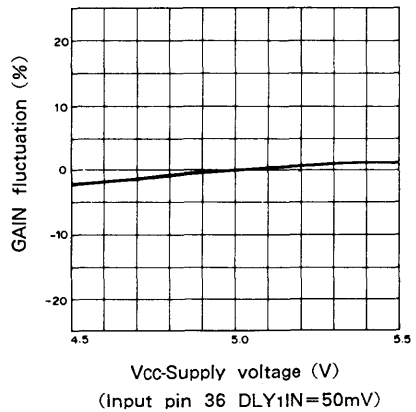
YIN – YL GAIN Vcc characteristics



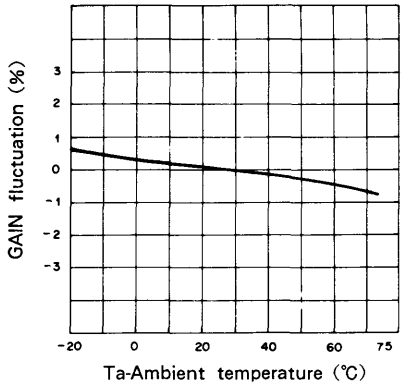
CSY GAIN Vcc characteristics



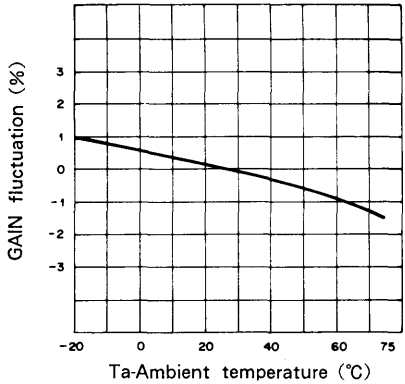
VCS GAIN Vcc characteristics



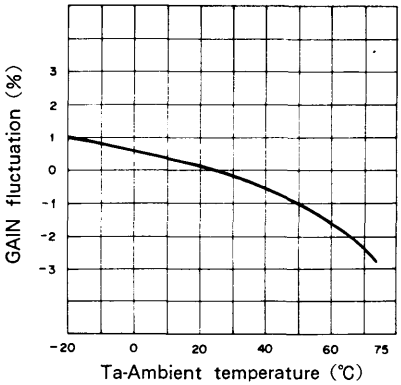
S_1, S_2 IN → C_0, Y_0 OUT Gain temperature characteristics



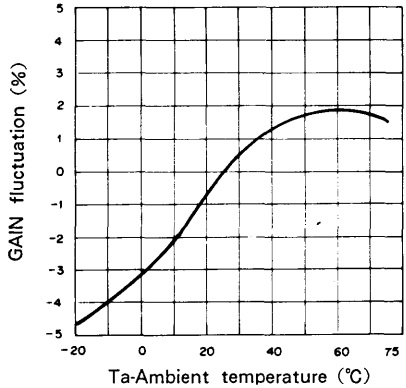
DLY_1, DLC_1 IN → Y_1, C_1 OUT gain temperature characteristics (0dB)



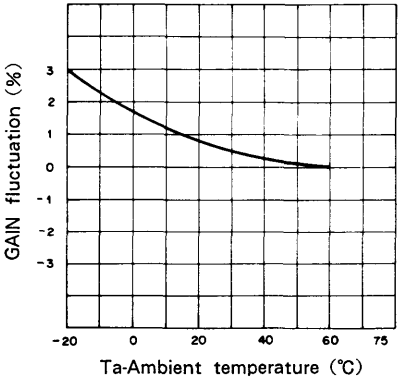
DLC_1 IN → R, B OUT gain temperature characteristics



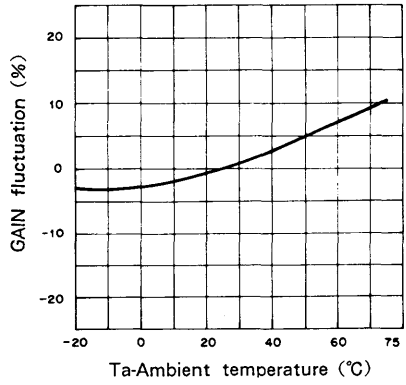
Y IN (220mV) → Y_Y OUT gain temperature characteristics



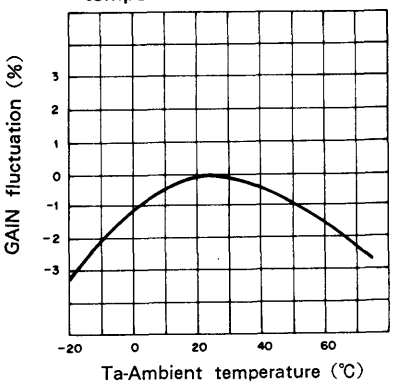
Y_{Y1} IN → Y_H OUT gain temperature characteristics



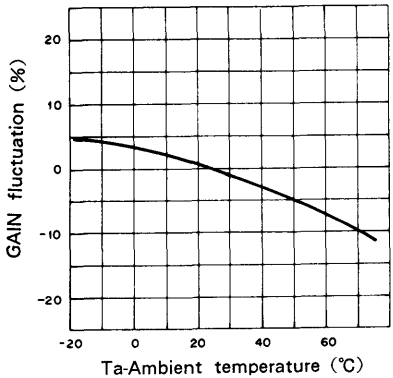
DLY_1 IN → Y_L - Y_H OUT aperture gain temperature characteristics



DLY1 IN (350mV) → YL - YH OUT CSY temperature characteristics.



DLY1 IN (50mV) → YL - YH OUT CSY VAP temperature characteristics.



Operation

CXA1151 is an IC that outputs RGB, YL - YH, YH, and CSY from the signal that sampled and held the complementary color checker coding imager. .

1. S1 and S2 input → RGB OUT

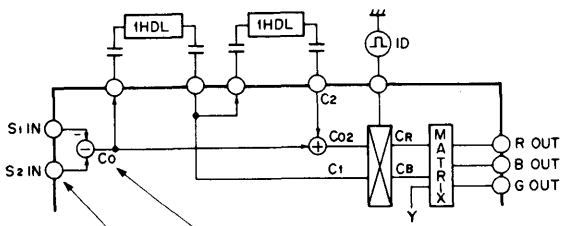


Table-1 Imager coding

Mg	G	Mg	G	0H
Ye	Cy	Ye	Cy	
G	Mg	G	Mg	1H
Ye	Cy	Ye	Cy	
Mg	G	Mg	G	2H
Ye	Cy	Ye	Cy	
S_2	S_1	S_2	S_1	

Table-2 Chroma signal

	0H(C_0)	1H(C_1)	2H(C_2)
C	2R−G	−(2B−G)	2R−G

Table-3 S1 and S2 signals

	0H	1H	2H
S_1	G+Cy	Mg+Cy	G+Cy
S_2	Mg+Ye	G+Ye	Mg+Ye

1) Imager
The coding imager shown in Table-1 is used.

2) S1 and S2 inputs
The signals that sampled and held the imager output are input. By using the imager shown in Table-1, field reading is performed to obtain signals shown in Table-3. G+Cy and G+Ye, or Mg+Ye and Mg+Cy are alternately input to S1 and S2 every hour.

3) Chroma signal
The chroma signal (C) is acquired from S_2 - S_1. As shown in Table-2, a signal that alternates 2R-G and 2B-G is obtained.

4) C_{02} and C_1 signals
To make the RGB signal in the matrix circuit, 2R-G and 2B-G are required at the same time. By using 1HDL, signal C_1 that 1 hour behind and signal C_2 that is 2 hours behind are created. By averaging C_0 and C_2 with the same period as 2B-G of C_1, 2R-G is created.

5) Multiplexing
2R-G and 2B-G are alternately sent every hour to C_1 and C_{02}, so 2R-G (C_R) and 2B-G (C_B) are separated by the ID pulse that inverts "L" to "H", or vice versa every 1 hour.

6) Matrix
RGB is made from C_R, C_B, and Y. The theoretical formulae shown below are applied.
$R=C_R+0.12Y$
$B=-C_B+0.20\ (Y-C_R)$
$G=Y-C_R+C_B$
Coefficients, 0.12 and 0.20, are adjustable. (RMTX and BMTX Pins)

7) RGB output
The RGB output is a clamped output. The clamped DC is output to the DC pin. From the R OUT, B OUT, and G OUT pins, the C_R, C_B, and Y signals to be fed to the matrix can be output.

2. Y IN, Y_L IN → Y_L - Y_H OUT
As Y_L that is output from Y_L - Y_H OUT, ② Y_L signal and ㊹ Y IN signal can be linearly switched with ③ AGC MIX pin of the MIX amplifier.

1) Y IN signal
$Y=Mg+G+Ye+Cy$ ((f_3) out of CXA1337), as the AGC output, is input.

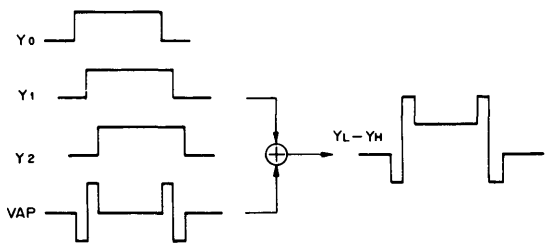
2) γ
The γ curve is adjustable, and presetting is available.

3) OFFSET
It is used in the negative mode. If GND is set, the output of the MIX amplifier comes out of Y_L - Y_H OUT. (For adjustment)

4) Y_L - Y_H OUT
By controlling the AGC MIX Pin, α (Y_L IN - Y IN) ($0 \leqq \alpha \leqq 1$) is output. The aperture signal is added and output.

3. V aperture signal
The V aperture signal is synthesized from $\frac{Y_0+Y_2}{2}-Y_1$

The signal is made at a ratio of 1 : 1 between plus and minus.



After aperture signal VAP is synthesized, the signal whose level around noise is sliced and controlled by the aperture slicing circuit is added to the Y_L - Y_H signal.

The aperture signal is not output when the Y signal exceeds a reference level.

That reference level has been preset but it can be adjusted with ㉕ AP CUT Pin.

If ㉕ AP CUT is set to GND, the aperture signal is not output at all.

4. Chroma suppressing Y signal

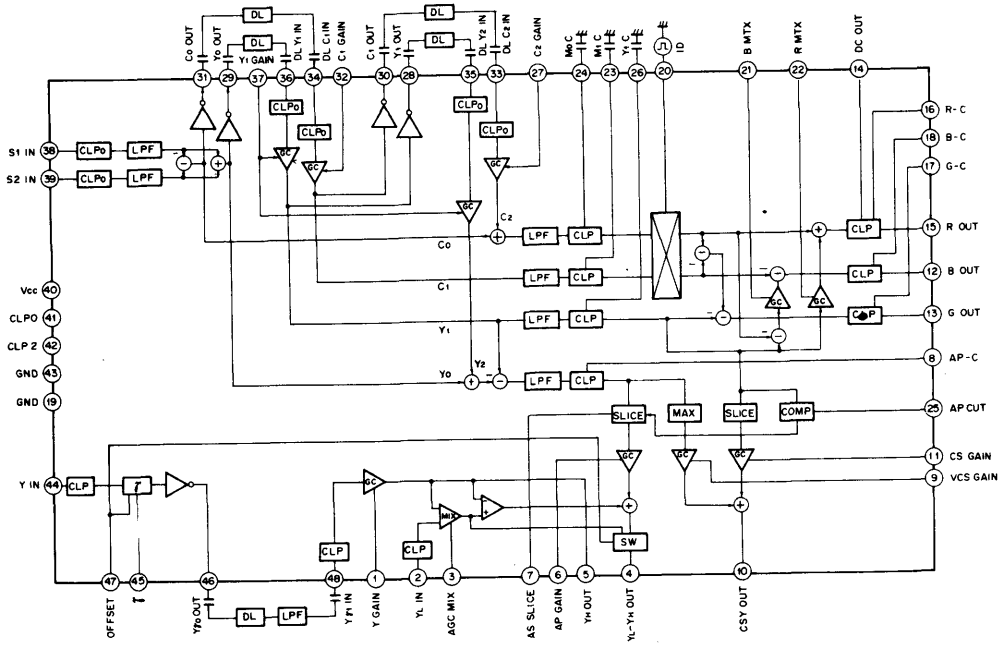
Depending on the Y signal level, a signal that suppresses the chroma signal is output.

The chroma suppressing Y (CSY) signal is made by mixing the following two signals :

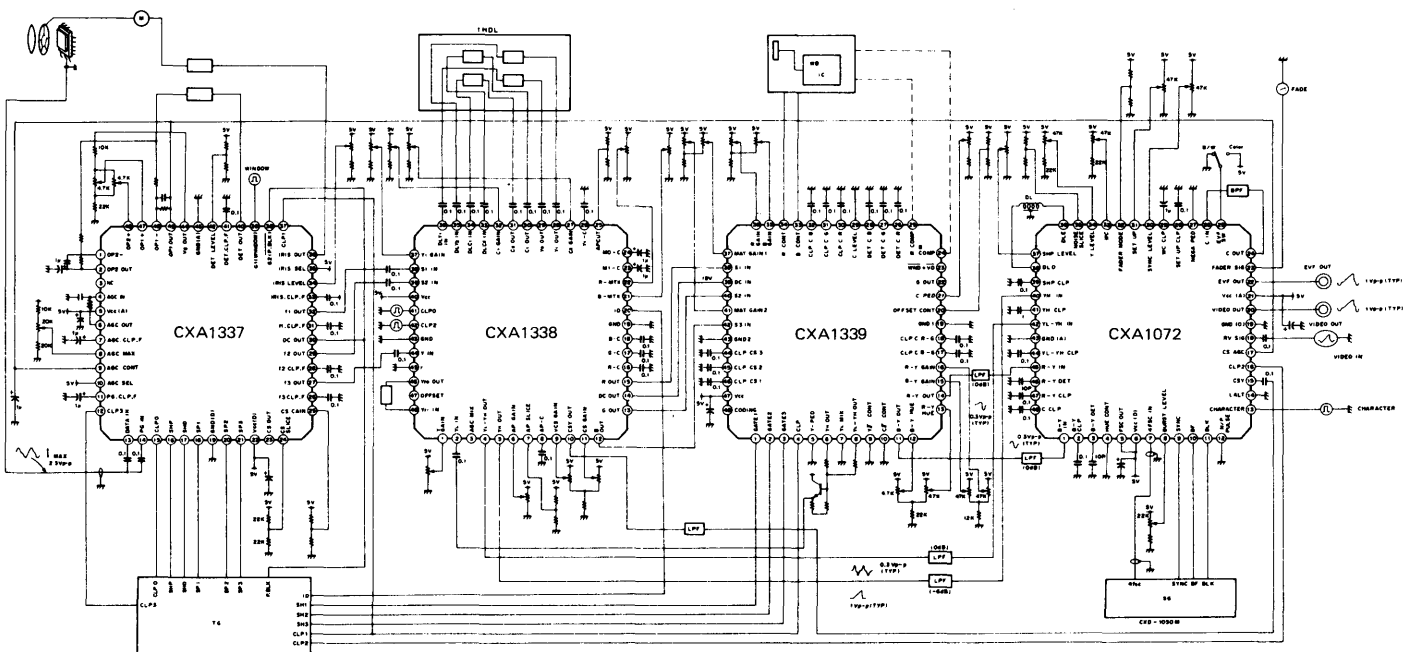
1) The amount of the Y signal exceeding a reference level (1.2 times of the reference signal) is output.

   The sliced amount is fixed. After slicing, the signal is gain-controlled and output.

2) The absolute value of the aperture signal is output as the CSY signal.



Application Circuit



- It is recommended to set the resistance with no value indicated to 50k Ω and below between Vcc and GND.
- Unspecified capacity unit is μF

SONY CXA1339Q-Z/R

CCD Camera Processor

Description

CXA1339Q-Z and CXA1339R are processor ICs for CCD color cameras. These execute color coding, white balance, γ compensation, HUE control and other signal processing to color separated input signals. γ compensated R-Y, B-Y and YH, YL-YH signals are also shaped.

Features

- The built-in color coding circuit makes it compatible with both types of CCD color filters, complementary color or primary color.
- Realizes high resolution through the adoption of YL-YH, and YH's Y signal processing.
- Compatible with negative/positive inversion.
- White balance is compatible with both automatic and one push button.
- Control pins have preset function.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	600	mW

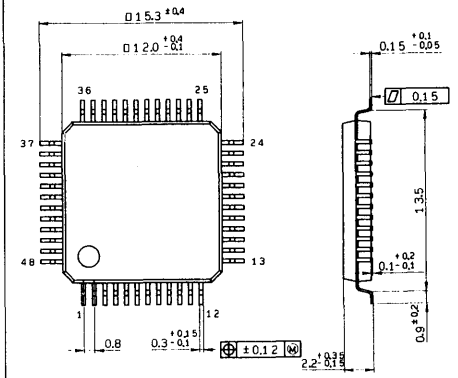
Recommended Operating Condition

• Supply voltage	Vcc	5±0.25	V

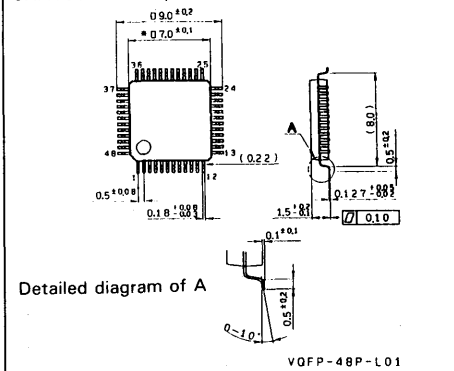
Package Outline

Unit: mm

CXA1339Q-Z 48 pin QFP (Plastic)



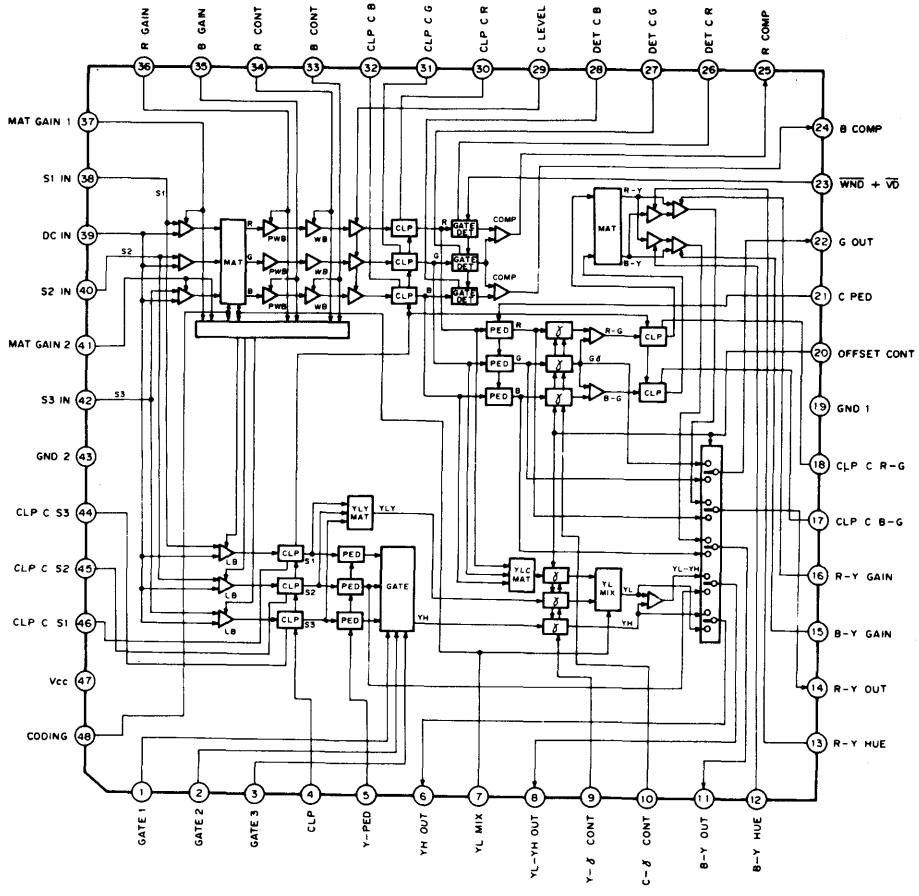
CXA1339R 48 pin VQFP (Plastic)



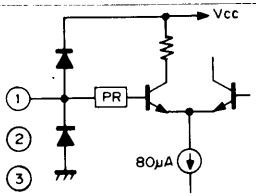
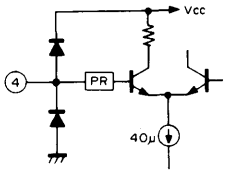
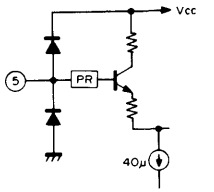
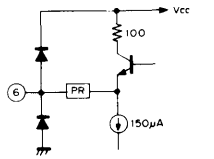
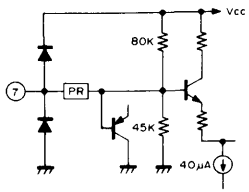
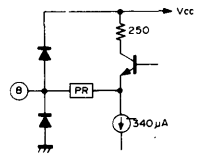
Note) Dimensions marked with* does not include residual resin.

80706-ST

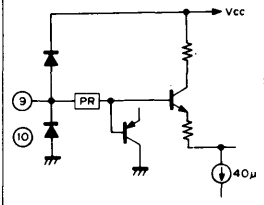
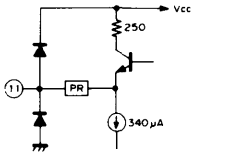
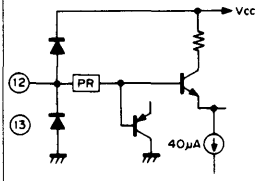
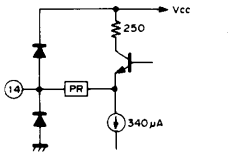
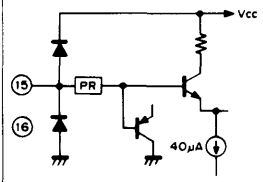
Block Diagram



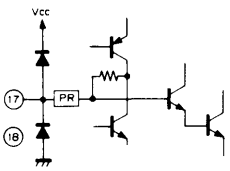
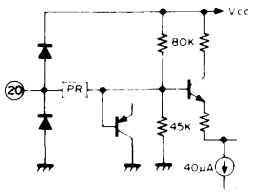
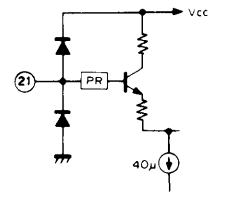
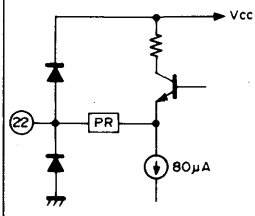
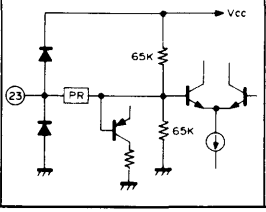
Pin Description

No.	Symbol	Equivalent circuit	Voltage	Description
1 2 3	GATE 1 GATE 2 GATE 3		3.1 to 5V* HI LEVEL 0 to 1.9V* LO LEVEL	With the gate pulse input of YH GATE, when GATE 1 turns to HI, YH=S1 when GATE 2 turns to HI, YH=S2. when GATE 3 turns to HI, YH=S3. It is active at HI.
4	CLP		3.1 to 5V* HI LEVEL 0 to 1.9V* LO LEVEL	This is the clamp pulse input pin for signals R, G, B, S1, S2, S3, R-G and B-G. It is active at HI.
5	Y PED		1.6 to 5V*	This is the Y signal dark slice level control pin.
			0 to 0.4V*	Preset mode pin (Y-PED OFF).
6	YH OUT		2.5V	When pin 20>1.6V YH output is on and when pin 20 <0.4V YL output is on.
7	YL MIX		1.6 to 5V*	This is the YLY and YLC MIX RATIO control pin. Color coding in complementary mode.
			0 to 0.4V*	Color coding in primary color mode. MIX ratio of YLY and YLC is YL 100% MAT GAIN 1 and 2 reach the same gain as S2 channel.
8	YL-YH OUT		3.0V	YL-YH output output when pin 20>1.6V.YTP output when pin 20<0.4V.

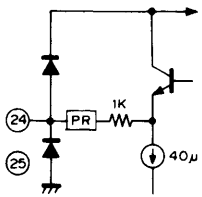
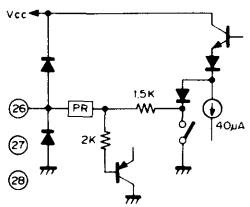
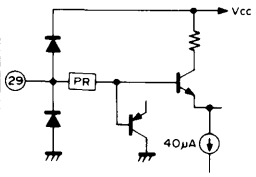
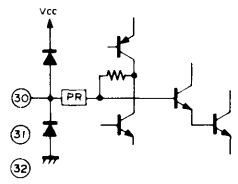
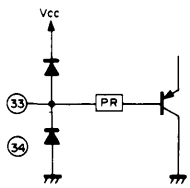
***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
9 10	Y-γ CONT C-γ CONT		1.6 to 5V*	Y signal, chroma signal γ control.
			0 to 0.4V*	Preset mode (Typ. γ curve)
11	B-Y OUT		3.0V	When pin 20>1.6V B-Y output. When pin 20<0.4V B output.
12 13	B-Y HUE R-Y HUE		1.6 to 5V*	HUE control of B-Y, R-Y
			0 to 0.4V*	Preset mode (HUE OFF)
14	R-Y OUT		3.0V	When pin 20>1.6V R-Y output. When pin 20<0.4V R output.
15 16	B-Y GAIN R-Y GAIN		1.6 to 5V*	Gain control of B-Y, R-Y.
			0 to 0.4V*	Preset mode. Pin 14 R-G output. Pin 11, B-G output.

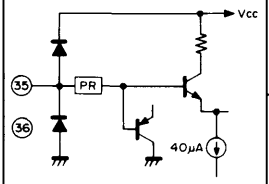
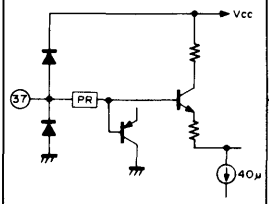
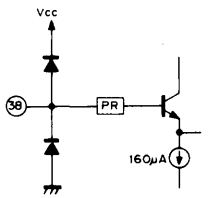
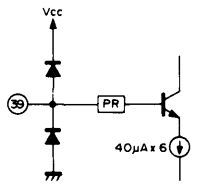
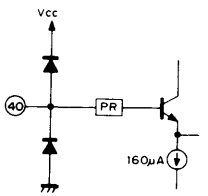
***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
17 18	CLP C B-G CLP C R-G		——	Capacitor connecting pin for B-G, R-G signal clamp.
19	GND1		GND*	GND pin for other than YH GATE part.
20	OFFSET CONT		1.6 to 5V*	Offset control during negative, positive inversion function. (For both Y and chroma systems)
			0 to 0.4V*	Output of pins 6, 8, 11, 14 and 22 changes.
21	C-PED		1.6 to 5V*	Dark slice level control of chroma signal.
			0 to 0.4V*	Preset mode (C-PED OFF)
22	G OUT		3.0V	When pin 20>1.6V Gγ output. When pin 20<0.4V G output.
23	$\overline{WND}$+$\overline{VD}$		2.5V 4.1 to 5V* WINDOW ON 0 to 0.9V* RESET ON	Pulse input pin for one push white balance system.

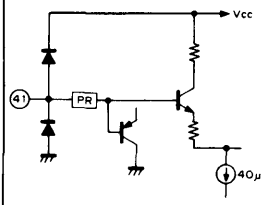
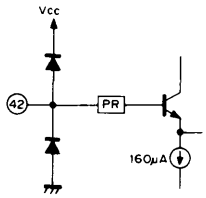
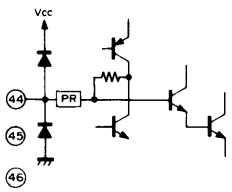
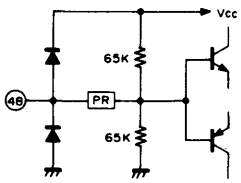
***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
24 25	B COMP R COMP		V_H>4V V_L<1V	Comparator output V_H is the output when B<G and R<G. V_L is the output when B>G and R>G.
26 27 28	DET C R DET C G DET C B		——	Connecting of capacitor for R, G, B signals peak detection.
29	C LEVEL		1.6 to 5V*	Chroma level control.
			0 to 0.4V*	Preset mode (0 dB for primary color mode, 6 dB for complementary color mode)
30 31 32	CLP C R CLP C G CLP C B		——	Connecting pin of capacitor for R, G, B signals clamp.
33 34	B CONT R CONT		0.4 to 2.5V*	White balance control.

***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
35 36	B GAIN R GAIN		1.6 to 5V*	Prewhite balance control.
			0 to 0.4V*	Preset mode (same gain as G channel)
37	MAT GAIN 1		1.6 to 5V*	Control of matrix amplifier 1.
			0 to 0.4V*	Preset mode (same gain as S2 channel)
38	S1 IN		—	For S1 signal input.
39	DC IN		1.9V*	Differential input vs S1 to S3 input.
40	S2 IN		—	For S2 signal input.

***Note)** External voltage applied

No.	Symbol	Equivalent circuit	Voltage	Description
41	MAT GAIN 2		1.6 to 5V*	Control of matrix amplifier 2.
			0 to 0.4V*	Preset mode (same gain as S2 channel)
42	S3 IN		——	For S3 signal input.
43	GND2		GND*	GND pin of YH GATE part.
44 45 46	CLP C S3 CLP C S2 CLP C S1		——	Capacitor connecting pin for S1, S2, and S3 signals clamp.
47	Vcc		5V*	Supply pin.
48	CODING		——	Mode control for color coding, effective only in complementary color mode (YL MIX>1.6V). Compatible codings are as follows.
			4.6 to 5V*	W, Ye, Cy mode
			2.5V	Ye, G, Cy mode
			0 to 0.4V*	W, Ye, G mode

***Note)** External voltage applied

Electrical Characteristics

Vcc=5V, Ta=25°C

No.	Item		Symbol	Input level (mV) S1	S2	S3	Pin conditions that differ from Electrical test circuit		Conditions formula of typical value	Test pin	Min.	Typ.	Max.	Unit	Test explanation, Remarks
1	Consumption current		Icc							47	20	33	46	mA	
2	White balance amplifier output level	Primary color mode G level	GM1		500					22	300	400	500	mV	Test of matching between channel and output level when the output signal is set to Pin 22: G out Pin 14: R out Pin 11: B out by means of the output switch SW.
3		Primary color mode R.G matching	RM1	500					14 Pin OUT/GM1	14	−2.2	0	2.2	dB	
4		Primary color mode B.G matching	BM1			500			11 Pin OUT/GM1	11	−2.2	0	2.2	dB	
5		W.Ye.G mode G level	GM2			250	YL MIX=OPEN CODING=0V			22	300	400	500	mV	
6		W.Ye.G mode R.G matching	RM2	250					14 Pin OUT/GM2	14	−2.2	0	2.2	dB	
7		W.Ye.G mode B.G matching	BM2		250				11 Pin OUT/GM2	11	−2.2	0	2.2	dB	
8		Ye.G.Cy mode G level	GM3			250	YL MIX=OPEN			22	300	400	500	mV	
9		Ye.G.Cy mode B.G matching	BM3	250					11 Pin OUT/GM3	11	−2.2	0	2.2	dB	
10		Ye.G.Cy mode R.G matching	RM3		250				14 Pin OUT/GM3	14	−2.2	0	2.2	dB	
11		W.Ye.Cy mode R level	RM4		250		YL MIX=OPEN CODING=5V			14	300	400	500	mV	
12		W.Ye.Cy mode B.R matching	BM4		250				11 Pin OUT/RM4	11	−2.2	0	2.2	dB	
13		W.Ye.Cy mode G1.R matching	GM4	250					22 Pin OUT/RM4	22	−2.2	0	2.2	dB	
14		W.Ye.Cy mode G2.R matching	GM5			250			22 Pin OUT/RM4	22	−2.2	0	2.2	dB	
15	MAT GAIN1	MIN GAIN	M1 MIN	250			YL MIX=OPEN CODING=0V	MAT GAIN1=1.6V	14 Pin OUT/RM2 14 Pin OUT	14			−1.4	dB	Ratio with output level when MAT GAIN1, 2 in preset mode at MAT GAIN 1 and 2 variable range test.
16		MAX GAIN	M1 MAX	250				MAT GAIN1=5V	14 Pin OUT/RM2 14 Pin OUT	14	2.5			dB	
17	MAT GAIN2	MIN GAIN	M2 MIN			250		MAT GAIN2=1.6V	22 Pin OUT/GM2	22			−1.4	dB	
18		MAX GAIN	M2 MAX			250		MAT GAIN2=5V	22 Pin OUT/GM2	22	2.5			dB	

V_{CC}=5V, Ta=25°C

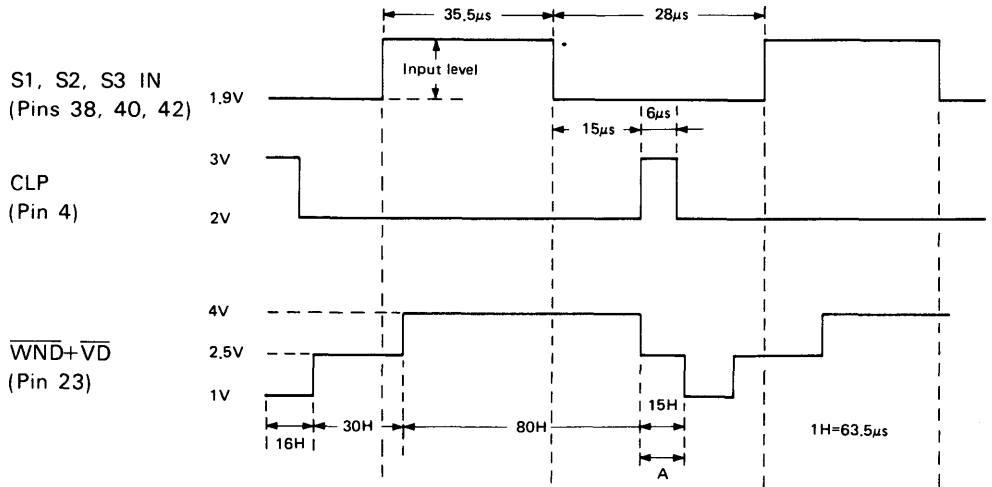
No.		Item	Symbol	Input level (mV) S1	S2	S3	Pin conditions that differ from Electrical test circuit	Conditions formula of typical value	Test pin	Min.	Typ.	Max.	Unit	Test explanation, Remarks
19	R GAIN	MIN GAIN	RGA MIN	500			R GAIN=5V	14 Pin OUT/RM1 14 Pin OUT	14			−1.4	dB	Ratio with output level when R, B GAIN in preset mode at R, B GAIN variable range test.
20	R GAIN	MAX GAIN	RGA MAX	167			R GAIN=1.6V	3×(14 Pin OUT/RM1 14 Pin OUT)	14	9.0			dB	
21	B GAIN	MIN GAIN	BGA MIN			500	B GAIN=5V	11 Pin OUT/BM1 11 Pin OUT	11			−1.4	dB	
22	B GAIN	MAX GAIN	BGA MAX			167	B GAIN=1.6V	3×(11 Pin OUT/BM1 11 Pin OUT)	11	9.0			dB	
23	R CONT	GAIN Linearity 0.4 Times	RC04	1250			R CONT=2.5V	14 Pin OUT/RM1 14 Pin OUT	14	−0.8	0	0.8	dB	Test of linearity of control voltage vs 1/GAIN for R, B CONT refer to diagram 3.
24	R CONT	GAIN Linearity 2.5 Times	RC025	200			R CONT=0.4V	14 Pin OUT/RM1 14 Pin OUT	14	−0.8	0	0.8	dB	
25	B CONT	GAIN Linearity 0.4 Times	BC04			1250	B CONT=2.5V	11 Pin OUT/BM1 11 Pin OUT	11	−0.8	0	0.8	dB	
26	B CONT	GAIN Linearity 2.5 Times	BC025			200	B CONT=0.4V	11 Pin OUT/BM1 11 Pin OUT	11	−0.8	0	0.8	dB	
27	C LEVEL	MIN GAIN	CG MIN		1000		C LEVEL=1.6V	0.5×(22 Pin OUT/GM1)	22			−4.8	dB	Ratio with output level when C LEVEL in preset mode at C LEVEL variable range test.
28	C LEVEL	MAX GAIN	CG MAX		200		C LEVEL=5V	2.5×(22 Pin OUT/GM1)	22	4.8			dB	
29	Comparator output voltage	R COMP LO LEVEL	R COMP1				Input signal where with $\overline{WND}+\overline{VD}$ pulse ON we have R<G and B<G.		25			1.0	V	Test concerns DC output level equipment to the A portion of the $\overline{WND}+\overline{VD}$ input waveform diagram.
30	Comparator output voltage	B COMP LO LEVEL	B COMP1						24			1.0	V	
31	Comparator output voltage	R COMP HI LEVEL	R COMP2				Input signal where with $\overline{WND}+\overline{VD}$ pulse ON we have R>G and B>G.		25	4.0			V	
32	Comparator output voltage	B COMP HI LEVEL	B COMP2						24	4.0			V	
33		Y PED Amount	YP1		500		Y PED=5V	Y PED=0V When 8 Pin OUT=8 Pin OUT	8	100			mV	Amount of dark slice in Y S2 channel.
34		C PED Amount	CPG		500		C PED=5V	GM1 22 Pin OUT	22	80			mV	Amount of dark slice in chroma type G channel.
35	C-γ reference curve	500 mV at input	CγG1		500		OFFSET CONT=OPEN		22	650	800	950	mV	
36	C-γ reference curve	200 mV at input	CγG2		200			22 Pin OUT/CγG1	22	0.48	0.58	0.68		γ I/O characteristics where CγG2 is the ratio with CγG1.

Vcc=5V, Ta=25°C

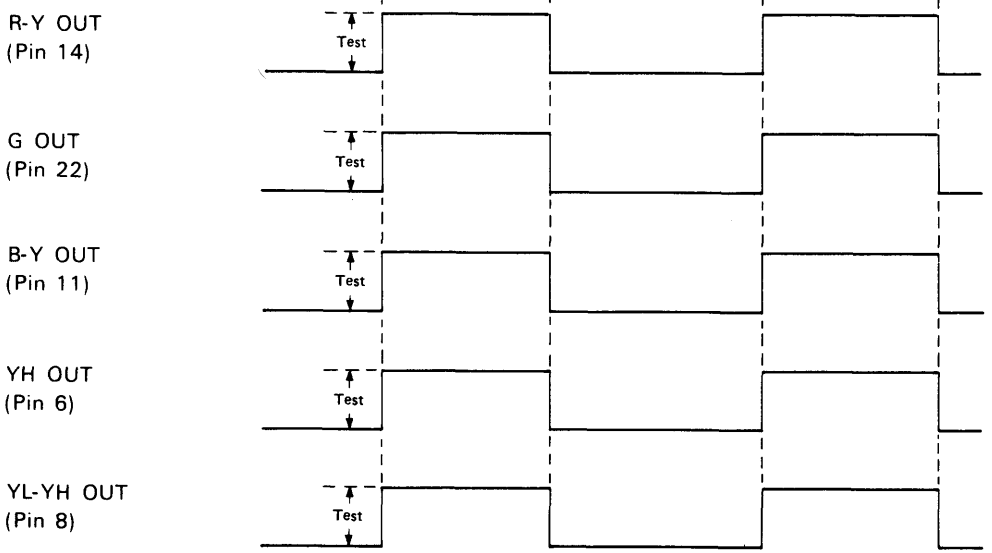
No.	Item	Symbol	Input level (mV) S1	S2	S3	Pin conditions that differ from Electrical test circuit		Conditions formula of typical value	Test pin	Min.	Typ.	Max.	Unit	Test explanation, Remarks
37	YHγ reference curve: 500 mV at input	YHγ1		500		OFFSET CONT =OPEN		6 Pin OUT/YHγ1	6	780	1015	1250	mV	Ratio between YHγ2 and YHγ1 at γ I/O characteristics
38	YHγ reference curve: 200 mV at input	YHγ2		200					6	0.48	0.58	0.68	–	
39	YH OUT DC	YHDC				OFFSET CONT =OPEN			6	2.1	2.5	2.9	V	Output pin DC level
40	YL-YH OUT DC	YLHDC							8	2.6	3.0	3.4	V	
41	R-Y GAIN: MIN GAIN	RY2	200			OFFSET CONT= OPEN	R-Y GAIN =1.6V	14 Pin OUT/R-Y GAIN=0V When 14 Pin OUT	14			−1.8	dB	Ratio between R-Y, B-Y GAIN variable range test.
42	R-Y GAIN: MAX GAIN	RY3	200				R-Y GAIN =5V	14 Pin OUT/R-Y GAIN=0V When 14 Pin OUT	14	7			dB	
43	B-Y GAIN: MIN GAIN	BY2			200	OFFSET CONT= OPEN	B-Y GAIN =1.6V	11 Pin OUT/B-Y GAIN=0V When 11 Pin OUT	11			1.8	dB	
44	B-Y GAIN: MAX GAIN	BY3			200		B-Y GAIN =5V	11 Pin OUT/B-Y GAIN=0V When 11 Pin OUT	11	7			dB	
45	R-Y HUE: MAX	RHU1	500			OFFSET CONT= OPEN	B-Y HUE =5V	$-\tan^{-1}\left(\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right)$	11	22			o	Angle with R-Y axis taken as reference at rotation angle variable range test using R-Y HUE.
46	R-Y HUE: MIN	RHU2	500				B-Y HUE =1.6V	$-\tan^{-1}\left(\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right)$	11			−22	o	
47	B-Y HUE: MAX	BHU1			500	OFFSET CONT= OPEN	R-Y HUE =5V	$\tan^{-1}\left(\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right)$	14	22			o	Angle with B-Y axis taken as reference at rotation angle variable range test using R-Y HUE.
48	B-Y HUE: MIN	BHU2			500		R-Y HUE =1.6V	$\tan^{-1}\left(\frac{11\text{ Pin OUT}}{14\text{ Pin OUT}}\right)$	14			−22	o	
49	R-Y OUT DC	RYDC				OFFSET CONT= OPEN	R-Y GAIN=5V		14	2.6	3.0	3.4	V	Output pin DC level.
50	B-Y OUT DC	BYDC					B-Y GAIN=5V		11	2.6	3.0	3.4	V	

Test Circuit I/O Waveform

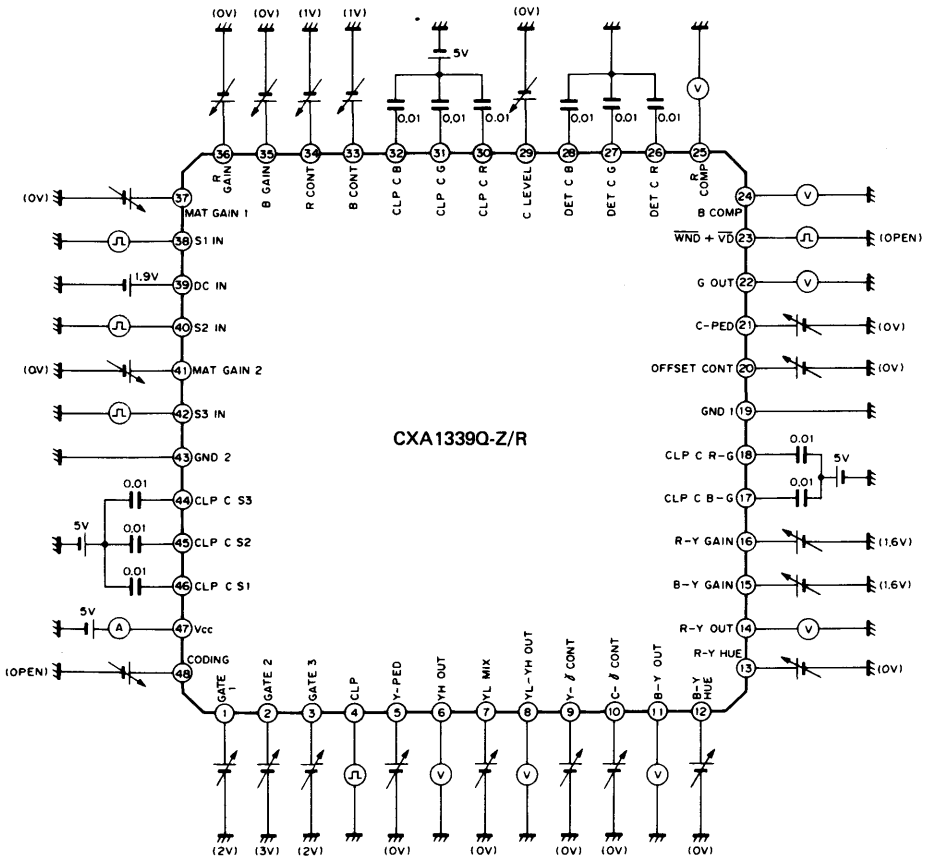
Input waveform



Output waveform



Electrical Characteristics Test Circuit



Note) 1. Capacitor capacity unit μF.

2. In brackets voltage in places not specifies in the descriptions of Electrical characteristics.

3. V indicates test pin. (AC, DC voltage test)

Operation

Color coding

Compatible with the combination of the 4 following color filters. Set through the applicatin of voltage to CODING (Pin 48) and YL MIX (Pin 7). The necessary conditions for the selection of each coding are as follows.

Filter color coding	CODING (Pin 48)	YL MIX (Pin 7)
R.G.B	–	GND
W.Ye.Cy	Vcc	Higher than 1.6V
Ye.G.Cy	OPEN	Higher than 1.6V
W.Ye.G	GND	Higher than 1.6V

W:White, Ye:Yellow, Cy:Cyan

Note) R.G.B modes are selected with YL MIX only and have no relation with the CODING voltage.

Preset mode

By grounding a pin that has the preset function, the control setting by that pin stands at a specified value. This is indicated in the following table.

No.	Symbol	Preset mode
5	Y-PED	Becomes Y-PED OFF.
7	YL MIX	Color coding at R.G.B, YL YLC 100%, MAT GAIN 1 and 2 reaches same gain as S2 channel.
9	Y-γ CONT	Becomes typical Y-γ curve. (See Fig. 11)
10	C-γ CONT	Becomes typical C-γ curve. (See Fig. 10)
12	B-Y HUE	Becomes B-Y HUE OFF.
13	R-Y HUE	Becomes R-Y HUE OFF.
15	B-Y GAIN	B-Y OUT (Pin 11) output becomes B-G.
16	R-Y GAIN	R-Y OUT (Pin 14) output becomes R-G.
20	OFFSET CONT	Pins 6, 8, 11, 14 and 22 of output SWs are switched.
21	C-PED	Becomes C-PED OFF.
29	C LEVEL	C LEVEL AMP gain becomes 0 dB at R.G.B modes. In other modes 6 dB.
35	B GAIN	B GAIN AMP gain becomes same as G channel.
36	R GAIN	R GAIN AMP gain becomes same as G channel.
37	MAT GAIN 1	MAT GAIN 1's gain becomes same as S2 channel.
41	MAT GAIN 2	MAT GAIN 2's gain becomes same as S2 channel.

Output switching SW

By grounding OFFSET CONT (pin 20) output SW of pins, 6, 8, 11, 14 and 22 and output signal becomes as follows.

No.	OFFSET CONT>1.6V output	OFFSET CONT<0.4V output
6	YH	YL
8	YL-YH	YTP (signal that has passed through PED of Y S2 channel)
11	B-Y	B (B signal before entry γ)
14	R-Y	R (R signal before entry γ)
22	G signal with γ applied	G (G signal before entry γ)

White balance control

1) Gain control

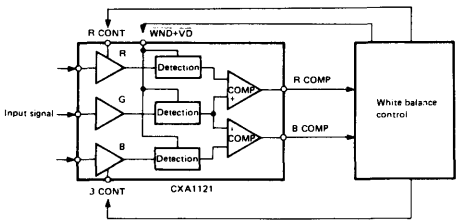
There are 2 types, R GAIN (Pin 36) and B GAIN (Pin 35) for precontrol and R CONT (Pin 34) and B CONT (Pin 33).

Also for R CONT, B CONT. The control voltage and the white balance amplifier gain reverse figures have a ratio relation. It is ideal as the control pin for auto white balance.

2) One push white balance (close loop white balance)

- An example is shown at right

R.G.B signals that have passed through white balance are PEAK detected and output as comparison signals R and G, B and G by means of the comparator. From the comparison signal, GAIN control is executed and by requesting R CONT B CONT to become R=B=G, white balance is completed.



- Detection part operation

$\overline{WND}+\overline{VD}$ (Pin 23) the operation of the detection part by means of external voltage application is as follows.

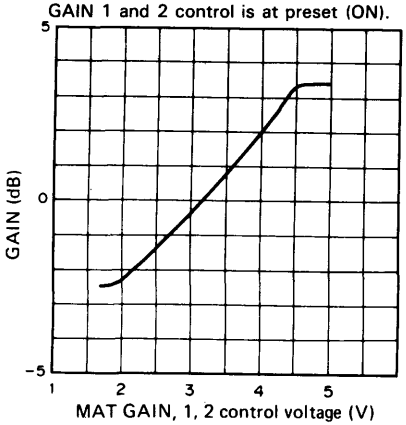
$\overline{WDN}+\overline{VD}>4.1V$: Detects input signal.

$\overline{WND}+\overline{VD}=2.5V$: Just before getting set to 2.5V, detection data is held.

$\overline{WND}+\overline{VD}<0.9V$: Detection data is reset.

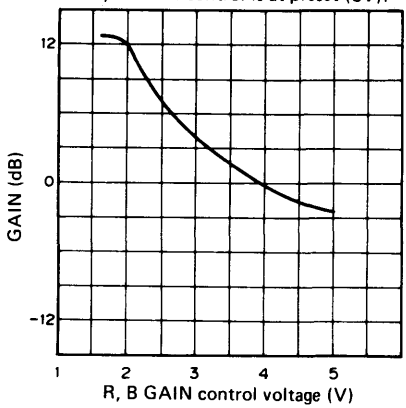
MAT GAIN 1, 2 control characteristics

Output is assumed to be 0 dB when MAT GAIN 1 and 2 control is at preset (ON).



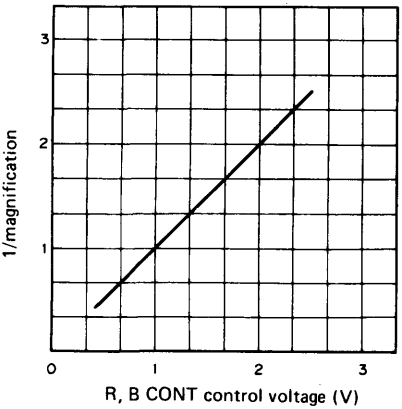
WB R, B GAIN control characteristics

Output is assumed to be 0dB when R, B GAIN control is at preset (0V).



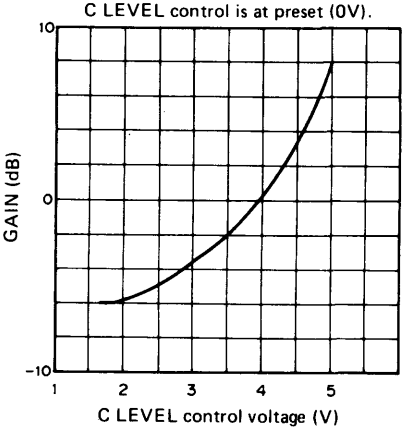
WB R, B CONT control characteristics

Output is assumed to be 1 when, R, B CONT control is at 1V.



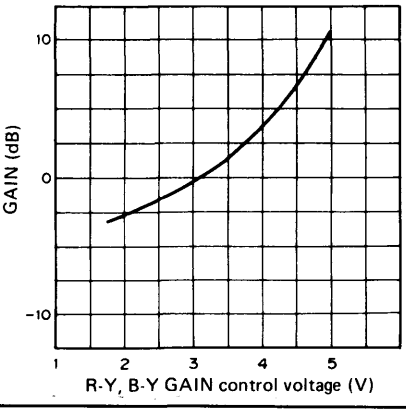
C LEVEL control characteristics

Output is assumed to be 0dB when C LEVEL control is at preset (0V).

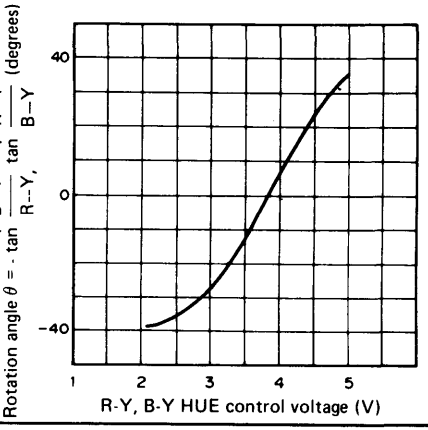


R-Y, B-Y GAIN control characteristics

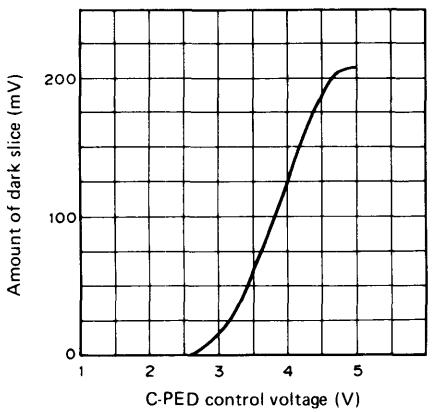
Output is assumed to be 0dB when R-Y, B-Y GAIN control is at preset (0V).



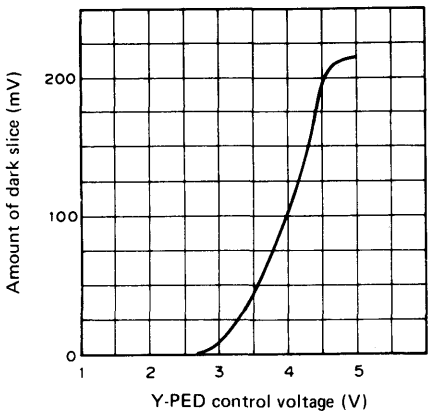
R-Y, B-Y HUE control characteristics



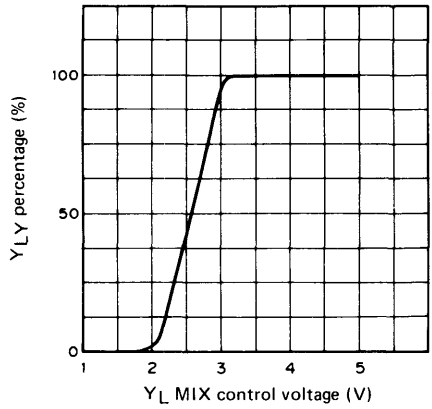
C-PED control characteristics



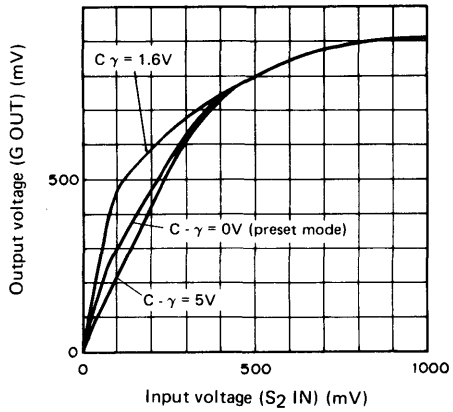
Y-PED control characteristics



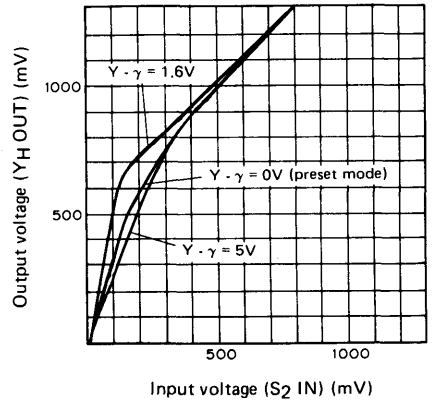
YL MIX control characteristics



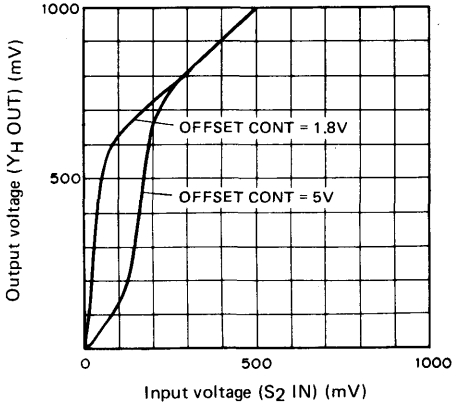
C-γ control characteristics



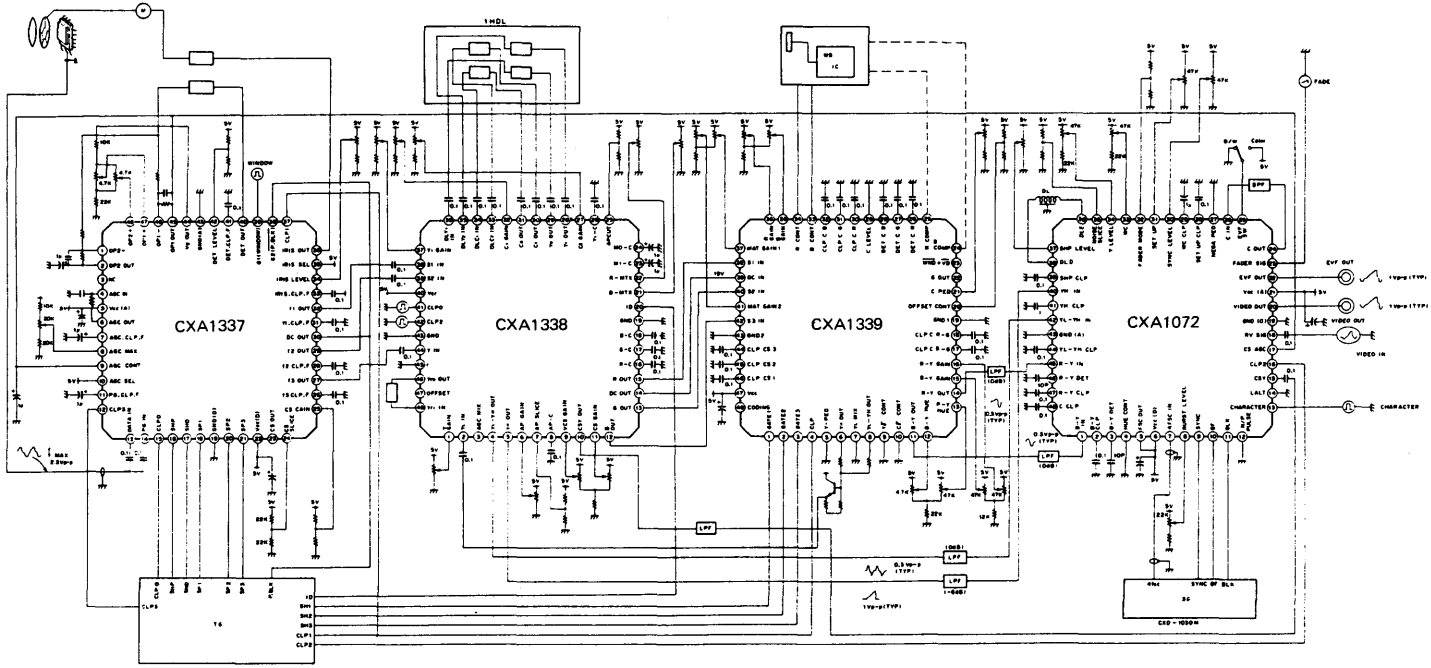
YH-γ OFFSET control characteristics



YH-γ control characteristics



768H Color Compensation Stripe CCD Camera System Diagram



- It is recommended to set the resistance with no value indicated to 50 kΩ and below between Vcc–GND.
- Unspecified capacity unit is μF.

SONY

CXA1072Q-Z/R

Camera Signal Processing

Description

CXA1072Q-Z and CXA1072R are encoder ICs for CCD color cameras.
Luminance and color difference signals are input to be output as composite video signals.
Combined use with system for CCD color cameras.

Features

- Built-in auto carrier balance (carrier balance adjustment unnecessary).
- Compatible with both NTSC/PAL.
- Compatible with Negative/Positive.
- Low consumption (200 mW) (150 mW in B/W mode)
- Low noise

Structure

Bipolar silicon monolithic IC.

Application

CCD color camera

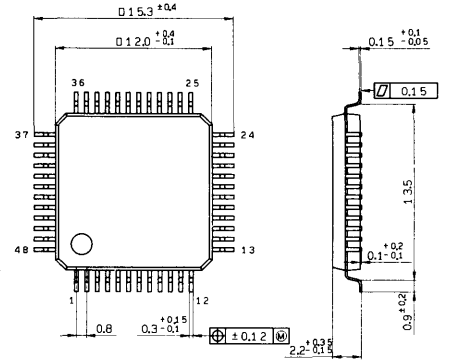
Function

- Set-up level control
- White clip level control
- White fader/black fader
- View finder output
- Character signal (superimpose)
- Sub carrier modulation
- Burst level control
- PAL mode
- Sub carrier output
- Sharpness level control
- Negative mode
- Return video input
- Auto carrier balance
- HUE control
- Sync level control
- Chroma suppress Y, chroma suppress AGC

Package Outline

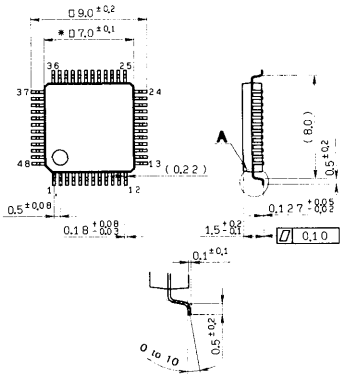
Unit: mm

48 pin QFP (Plastic)



QFP-48P-L04

48 pin VQFP (Plastic)



VQFP-48P-L01

Absolute Maximum Ratings (Ta=25°C)

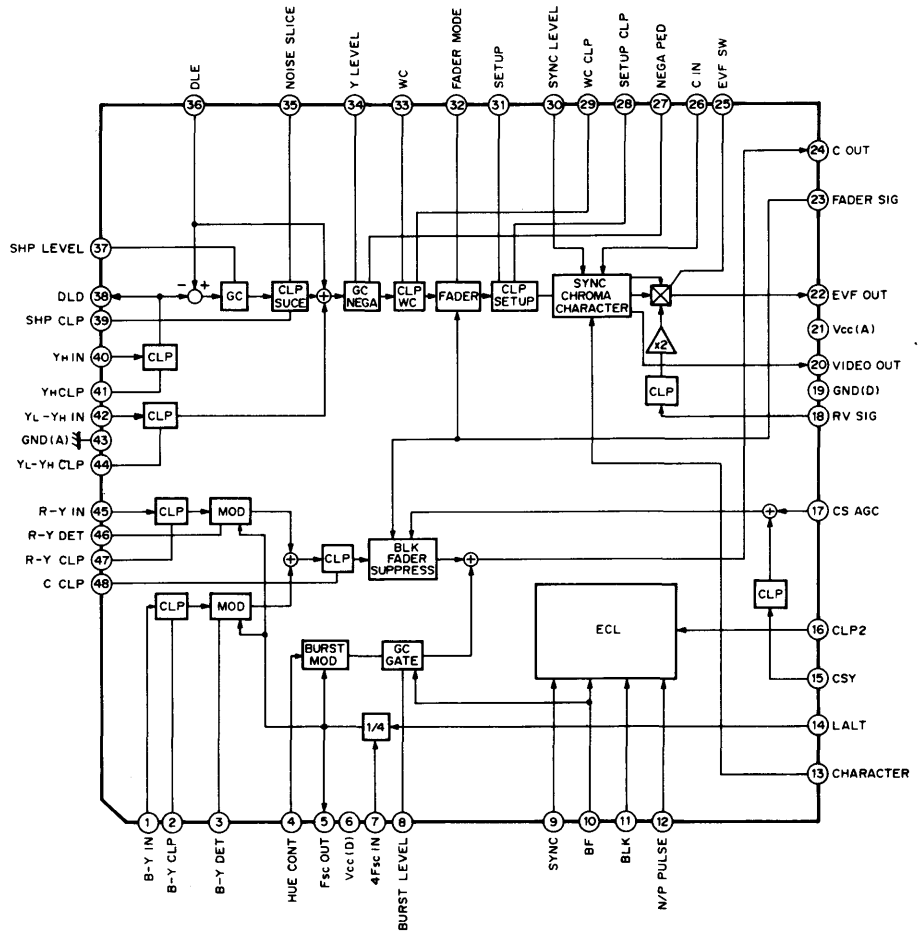
• Supply voltage	Vcc	7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	600	mW

Recommended Operating Condition

• Supply voltage	Vcc	4.75 to 5.25	V

70813A-ST

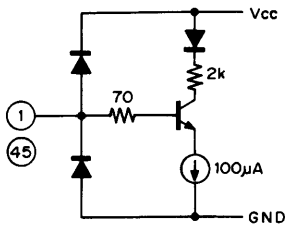
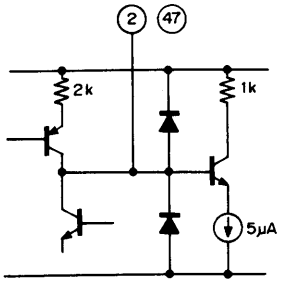
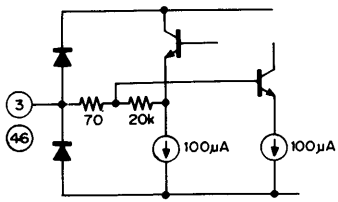
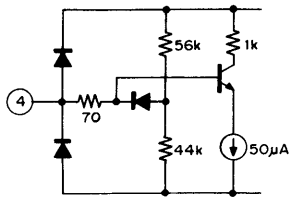
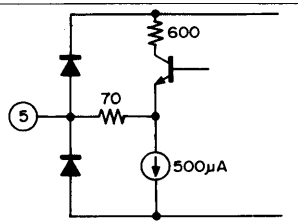
Block Diagram and Pin Configuration

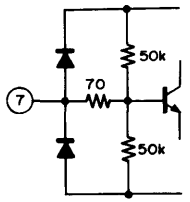
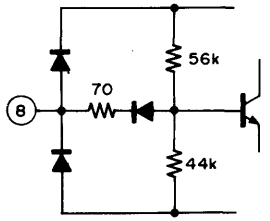
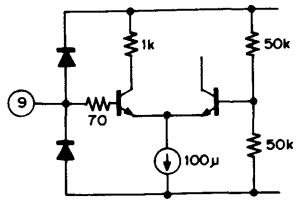
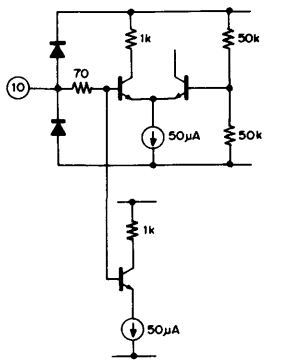


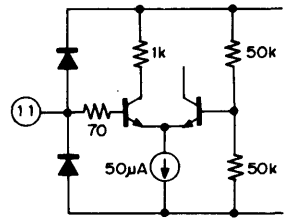
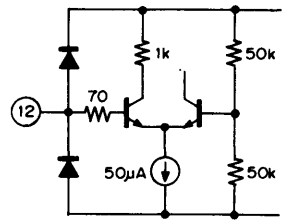
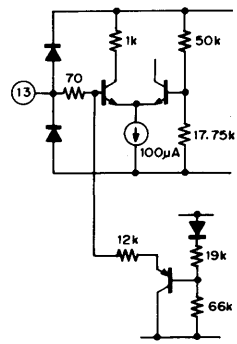
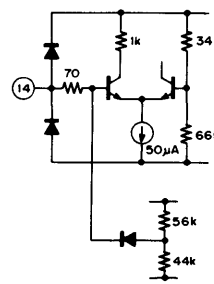
Abbreviations

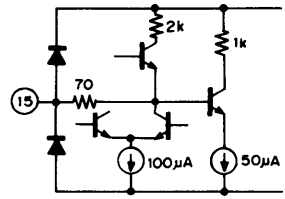
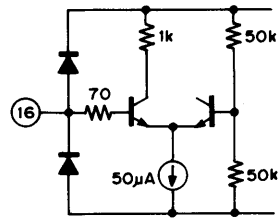
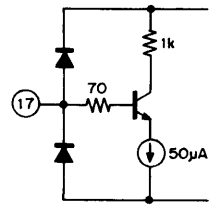
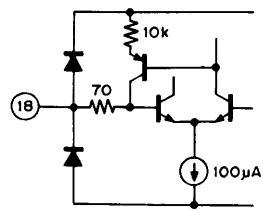
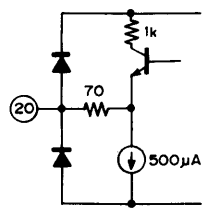
CLP	Clamp	RV	Return Video
DET	Detecter	EVF	Electric View Finder
CONT	Control	CIN	Chroma Input
BF	Burst Frag	PED	Pedestal
BLK	Blanking	WC	White Clip
N/P	Nega/Posi	DLD	Delay Line Drive
LALT	Line Alternate	DLE	Delay Line End
CSY	Chroma Suppres Y	SHP	Sharpness

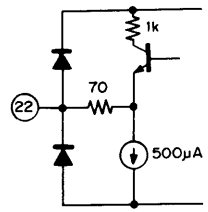
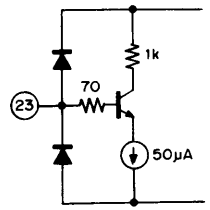
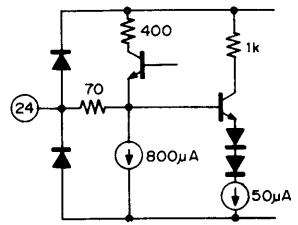
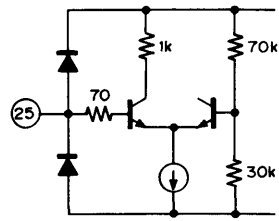
Pin Description and Equivalent Circuit

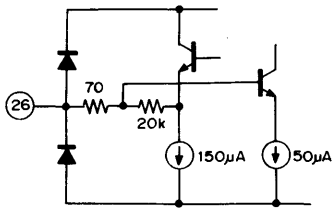
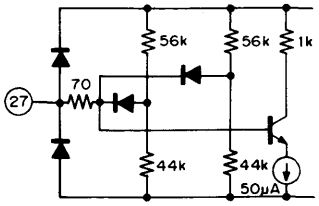
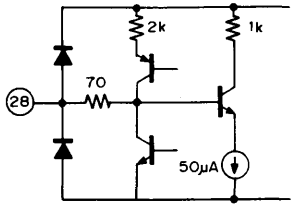
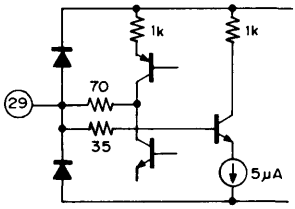
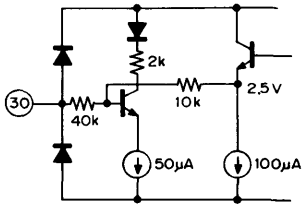
No.	Symbol	Voltage	Equivalent circuit	Description
1 45	B-Y IN R-Y IN	3.0V (External) 3.0V (External)		Color difference signal input pin.
2 47	B-Y CLP R-Y CLP	3.0V 3.0V		Connecting pin to the color signal input CLP capacitor.
3 46	B-Y DET R-Y DET	3.5V 3.5V		Connecting pin to the capacitor for auto carrier balance.
4	HUE CONT	0V (External)		HUE control pin 0V..... HUE OFF 2.5V to 5V..... Control
5	FSC OUT	Low-2.9V Hi-3.6V		Sub carrier output pin

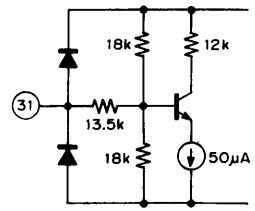
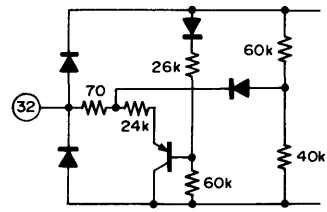
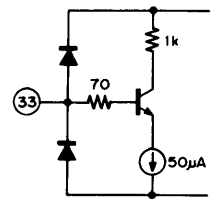
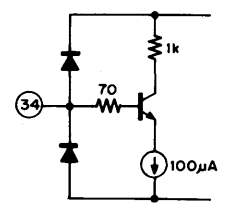
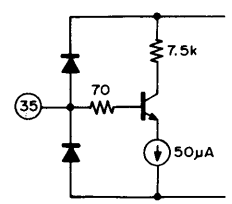
No.	Symbol	Voltage	Equivalent circuit	Description
6	Vcc (D)	5V		Digital circuit supply.
7	4FSC IN	2.5V (When open)		Pin that inputs signals with a frequency 4 times that of the sub carrier
8	BURST LEVEL	3.7V (External)		Burst level control pin Ground when using for analog burst.
9	SYNC	Pulse input		Sync pulse input pin Negative polarity Low: 0 to 2V Hi: 3 to 5V
10	BF	Pulse input		Burst pulse input pin Negative polarity Input 2.5 to 3.5V signal during analog burst usage. 3.5V 2.5V

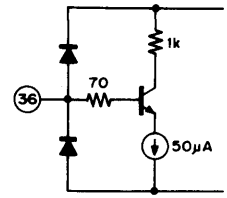
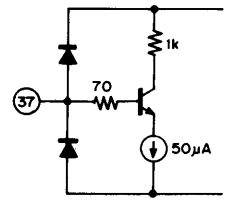
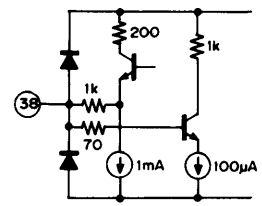
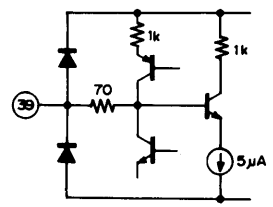
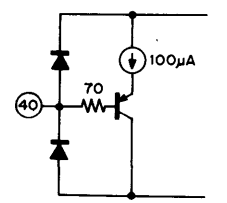
No.	Symbol	Voltage	Equivalent circuit	Description
11	BLK	Pulse input		Blanking pulse input pin Negative polarity Low: 0 to 2V Hi: 3 to 5V
12	N/P PULSE	Pulse input		Pulse input pin in negative mode. At high level negative pedestal. Low: 0 to 2V Hi: 3 to 5V
13	CHARACTER	Pulse input		Character pulse input pin 2.5V 2.0 Input 2.5V to 3.5V signal during analog burst usage.
14	LALT	Pulse input		Line alternate pulse input pin NTSC mode: GND PAL mode: 2H period pulse Low: 2.2 to 2.8V Hi: 3.8 to 5V

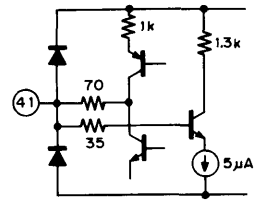
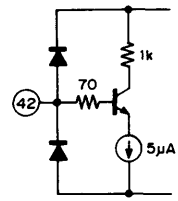
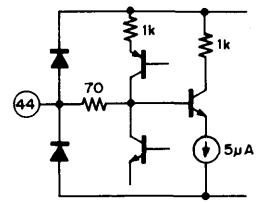
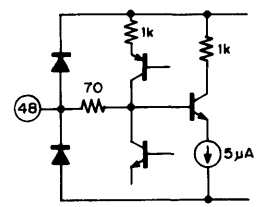
No.	Symbol	Voltage	Equivalent circuit	Description
15	CSY	2.85V		Chroma suppress Y signal input pin
16	CLP2	Pulse input		Clamp pulse input pin ⎍ Positive polarity Low: 0 to 2V Hi: 3 to 5V
17	CS AGC	GND (External)		Chroma suppress AGC signal. Input pin
18	RV SIG	2V		Return video signal input pin
19	GND (D)	0V		
20	VIDEO OUT	2.1V		Video output pin

No.	Symbol	Voltage	Equivalent circuit	Description
21	Vcc (A)	5V		Analog circuit supply
22	EVF OUT	2.1V		View finder output pin
23	FADER SIG	GND (External)		Fader signal input pin
24	C OUT	2.6V		Chroma signal ouput pin  Short waveform is output. In B/W mode by turning the pin to Vcc power saving is possible.
25	EVF SW	5V (External)		EVF output select pin 0V . . . . . Return Video 1.5 to 3.5V . . . . . Color mode 5V . . . . . B/W mode

No.	Symbol	Voltage	Equivalent circuit	Description
26	C IN	2.5V		Chroma signal mixed input pin
27	NEGA PED	0V (External)		NEGA/POSI modes select pin 0V . . . . . POSI 2 to 5V . . . . . Nega pedestal Level control
28	SETUP CLP	2.7V		SETUP CLP capacitor connecting pin
29	WC CLP	2.8V		WC CLP capacitor connecting pin
30	SYNC LEVEL	2.5V		Sync level control pin

No.	Symbol	Voltage	Equivalent circuit	Description
31	SETUP	2.5V (External)		Set-up level control pin Video output pin
32	FADER MODE	0V (Exteranl)		Fader mode select pin 0 to 2V..... Black fader 2 to 3.7V..... White fader White level control
33	WC	3.5V (External)		White clip level control pin
34	Y LEVEL	3.2V (External)		White signal level control pin
35	NOISE SLICE	3V (External)		Noise slice level control pin

No.	Symbol	Voltage	Equivalent circuit	Description
36	DLE	3.4V		Delay line connecting pin for sharpness signal formation.
37	SHP LEVEL	3.5V		Sharpness level control pin Chroma signal mixed input pin
38	DLD	3.4V		Delay line connecting pin for sharpness signal formation.
39	SHP CLP	2.5V		Sharpness clamp capacitor connecting pin
40	Y_H IN	1.2V (External)		Y_H signal input pin

No.	Symbol	Voltage	Equivalent circuit	Description
41	Y_H CLP	2.1V		Y_H clamp capacitor connecting pin
42	Y_L-Y_H IN	3.0V (External)		Y_L-Y_H signal input pin
43	GND (A)	0V		
44	Y_L-Y_H CLP	3V		Y_L-Y_H clamp capacitor connecting pin
48	CHROMA CLP	3.9V		CHROMA clamp capacitor connecting pin

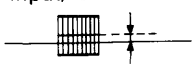
Electrical Characteristics

V=5V, Ta=25°C

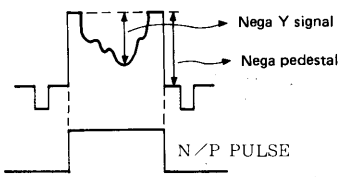
No.	Item	Symbol	Condition	Test point	Min.	Typ.	Max.	Unit
1	Supply current (color)	Icc	Current that flows into Vcc1, Vcc2	Vcc1, Vcc2	31	40	53	mA
2	Supply current (B/W)	Icc (B/W)	Current that flows into Vcc1,Vcc2	Vcc1, Vcc2	22	30	40	mA
3	Y_H level MIN.	Y MIN	Y LEVEL=5V, Y_H IN=500 mV	VIDEO OUT	230	320	410	mV
4	Y_H level MAX.	Y MAX	Y LEVEL=2V, Y_H IN=250 mV	VIDEO OUT	410	770	1240	mV
5	Y_H level MAX/MIN Y_H CLP 2.1V	Y CONT	No.3 and No.4 ratio		8	13	17	dB
6	Y_L-Y_H/Y_H gain difference	Y_L-Y_H	Y_L-Y_H IN=250 mV (I/O gain difference with Y_H IN=500 mV)	VIDEO OUT	−1.1	0	1.1	dB
7	EVF OUT/VIDEO OUT gain difference	EVF	Y_H IN=500 mV (I/O gain difference with the results obtained from VIDEO OUT test)	EVF OUT	−1.1	0	1.1	dB
8	White clip MAX	WC MAX	Y_H IN=500 mV Y LEVEL=2V, WC=5V	VIDEO OUT	870	1140	1430	mV
9	White clip MIN	WC MIN	Y_H IN=500 mV Y LEVEL=2V, WC=2V	VIDEO OUT	440	540	660	mV
10*1	Nega pedestal MAX	NPED MAX	NEGA PULSE input, NEGA PED=5V WC=5V, BLK=5V	VIDEO OUT	880	1030	1220	mV
11	Nega pedestal MIN	NPED MIN	NEGA PULSE input, NEGA PED=2V W/C=5V, BLK=5V	VIDEO OUT	240	330	460	mV
12	Nega Y_H/Posi Y_H gain difference	NEGA Y	NEGA PULSE input, NEGA PED=3.4V Y_H IN=250 mV (I/O gain difference with IN=500 mV in posi mode)	VIDEO OUT	−1.1	0	1.1	dB

No.	Item	Symbol	Condition	Test point	Min.	Typ.	Max.	Unit
13	Sharpness upper side level	SHP UP	Y_H IN=−20 mV Y_L-Y_H IN=250 mV SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V SW2 ON	VIDEO OUT	30	84	140	mV
14	Sharpness up down ratio	SHP LOW	Y_H IN=20 mV Y_L-Y_H IN=250 mV SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V, SW2 ON (Ratio of sharpness upper side level vs. sharpness lower side level)	VIDEO OUT	1.5	2.0	2.5	V/V
15	Nega sharpness upper side level	N SHP UP	Y_H IN=20 mV NEGA PULSE input SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V, SW2 ON	VIDEO OUT	30	84	140	mV
16	Nega sharpness up down ratio	N SHP LOW	Y_H In=−20 mV NEGA PULSE input SET UP=5V, NOISE SLICE=3.0V SHP LEVEL=3.5V SW2 ON	VIDEO OUT	1.5	2.0	2.7	V/V
17	White fader	W FADE	BLK input, FADER SIG=3.5V FADER MODE=2.5V	VIDEO OUT	260	350	440	mV
18	SETUP MAX	SETUP MAX	BLK input, FADER SIG=3.5V SET UP=5V	VIDEO OUT	165	140	185	mV
19	SYNC MAX	SYNC MAX	SYNC input, BLK=0V FADER SIG=3.5V SYNC LEVEL=5V	VIDEO OUT	360	430	520	mV
20	SYNC MIN	SYNC MIN	SYNC input, BLK=0V FADER SIG=3.5V SYNC LEVEL=0V	VIDEO OUT	100	170	250	mV

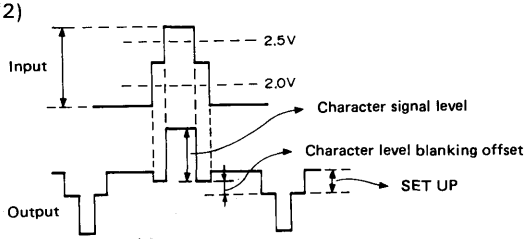
No.	Item	Symbol	Condition	Test point	Min.	Typ.	Max.	Unit
21	SYNC EVF (B/W)—V OUT Difference	SYNC (B/W)	SYNC input, BLK=0V FADER SIG=3.5V SYNC LEVEL=OPEN Ratio with B-Y level No.33	EVF OUT	−70	0	70	mV
22	SYNC EVF (Color)—V OUT Difference	SYNC (COL)	SYNC input, BLK=0V FADER SIG=3.5V, EVF SW=2.5V SYNC LEVEL=OPEN (Difference with the VIDEO OUT Sync under the same conditions)	EVF OUT	−70	0	70	mV
23	Character blanking level offset (V-OUT)	CHA OFF	BLK input, CHARACTER=2.25V	VIDEO OUT	3	100	170	mV
24	Character blanking level offset (EVF B/W)	CHA OFF (B/W)	BLK input, CHARACTER=2.25V	EVF OUT	3	100	170	mV
25	Character blanking level offset (EVF COL)	CHA OFF (COL)	BLK input, CHARACTER=2.25V EVF SW=2.5V	EVF OUT	20	100	190	mV
26*2	Character level (V-OUT)	CHA	BLK input, CHARACTER=3.2V	VIDEO OUT	475	520	595	mV
27	Character level (EVF B/W)	CHA (B/W)	BLK input, CHARACTER=3.2V (Ratio vs. VIDEO OUT character level)	EVF OUT	−1.1	0	1.1	dB
28	Character level (EVF COL)	CHA (COL)	BLK input, CHARACTER=3.2V EVF SW=2.5V (Ratio vs. VIDEO OUT character level)	EVF OUT	−1.1	0	1.1	dB

No.	Item	Condition	Test point	Min.	Typ.	Max.	Unit
29	Return video gain	EVF SW=0V RV SIG IN=350 mV	EVF OUT	4.5	6	7.5	dB
30	FSC OUT amplitude	SW4 ON	FSC OUT	610	710	810	mV
31	Carrier balance 3.58 MHz	B-Y IN, R-Y IN=2.1V and 3.9V	BPF OUT	—	1.3	3.5	mVp-p
32	Carrier balance 500 kHz	4FSC IN=2 MHz B-Y IN, R-Y IN=2.1V and 3.9V	BPF OUT	—	1.2	3.5	mVp-p
33	B-Y level	B-Y IN=300 mV	BPF OUT	400	470	550	mVp-p
34	R-Y level	R-Y IN=300 mV	BPF OUT	400	470	550	mVp-p
35	CHROMA TOTAL GAIN	B-Y IN=300 mV SW3 ON	VIDEO OUT	1.9		2.8	V/V
36	CHROMA GAIN EVF/ V-OUT ratio	B-Y IN=300 mV SW3 ON, EVF SW=2.5V	VIDEO OUT EVF OUT	−1.1	0	1.1	dB
37	CHROMA D-Range	B-Y IN=900 mV	BPF OUT	990	1130	1260	mVp-p
38	CS AGC MAX	B-Y IN=300 mV CS AGC=3.5V (Ratio with B-Y level No.33)	BPF OUT	40	50	60	%
39	BURST MAX	BF=0V, BLK=0V BURST LEVEL=5V	BPF OUT	310	390	480	mVp-p
40	BURST MIN	BF=0V, BLK=0V BURST LEVEL=2.5V	BPF OUT	88	110	132	mVp-p
41	BURST PAL Hi/Low	BF=0V, BLK=0V Ratio LALT=5 when LALT=2.5V	BPF OUT	−3	0	5	%
42	BURST linear MAX	BF=0V, BLK=0V BURST LEVEL=0V	BPF OUT	340	450	560	mVp-p
43	BURST level blanking offset	BF input, BLK=0V 	C OUT	−55	0	55	mV
44	CHROMA BLK level offset	BLK input, BF=5V	C OUT	−55	0	55	mV

*1)

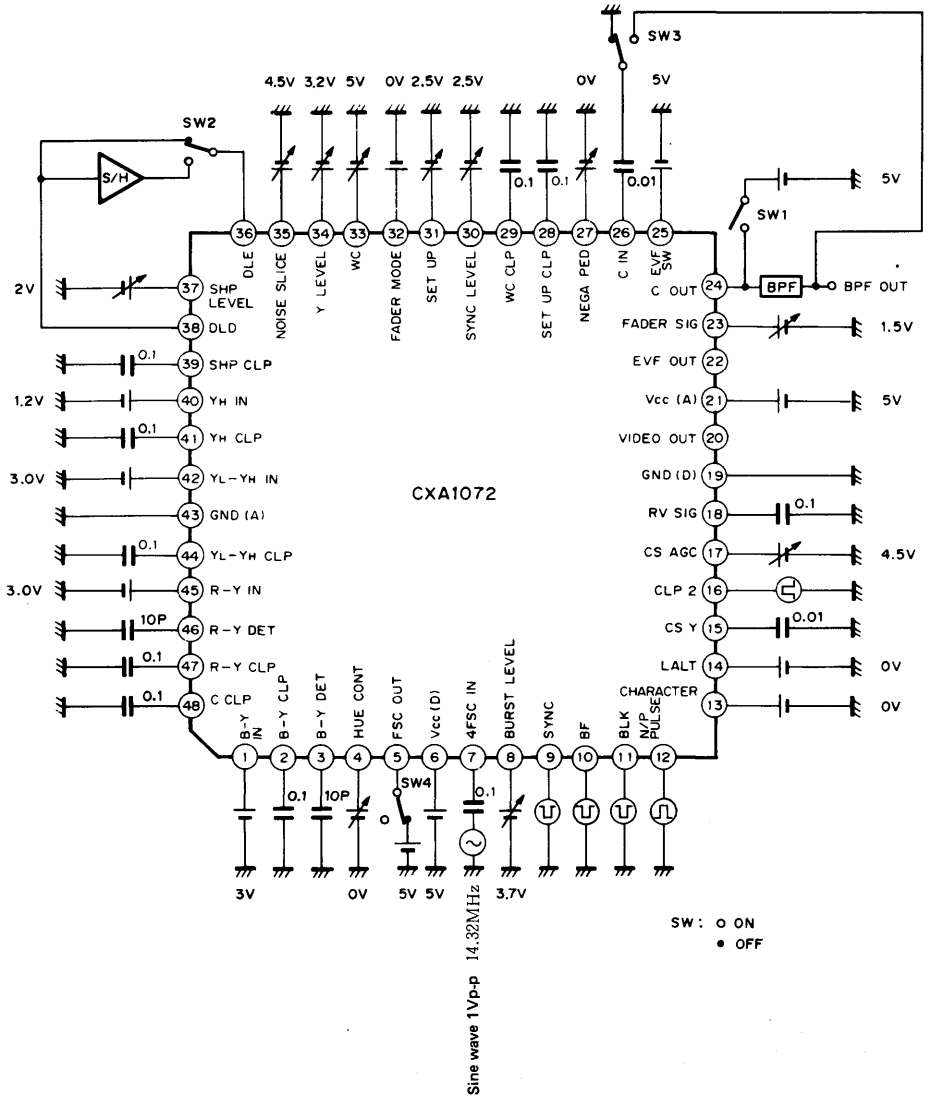


*2)



Test Circuit

(Typical Setting)



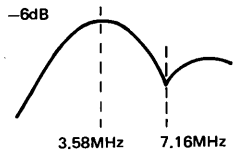
Note) Above conditions are given as the typical setting. The individual conditions of each item are indicated in the chart.

Test Conditions

1. BPF

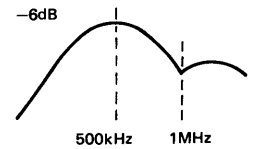
(1) 3.58 MHz BPF

The BPF where with an input of a 3.58 MHz sine wave the output becomes 1/2.



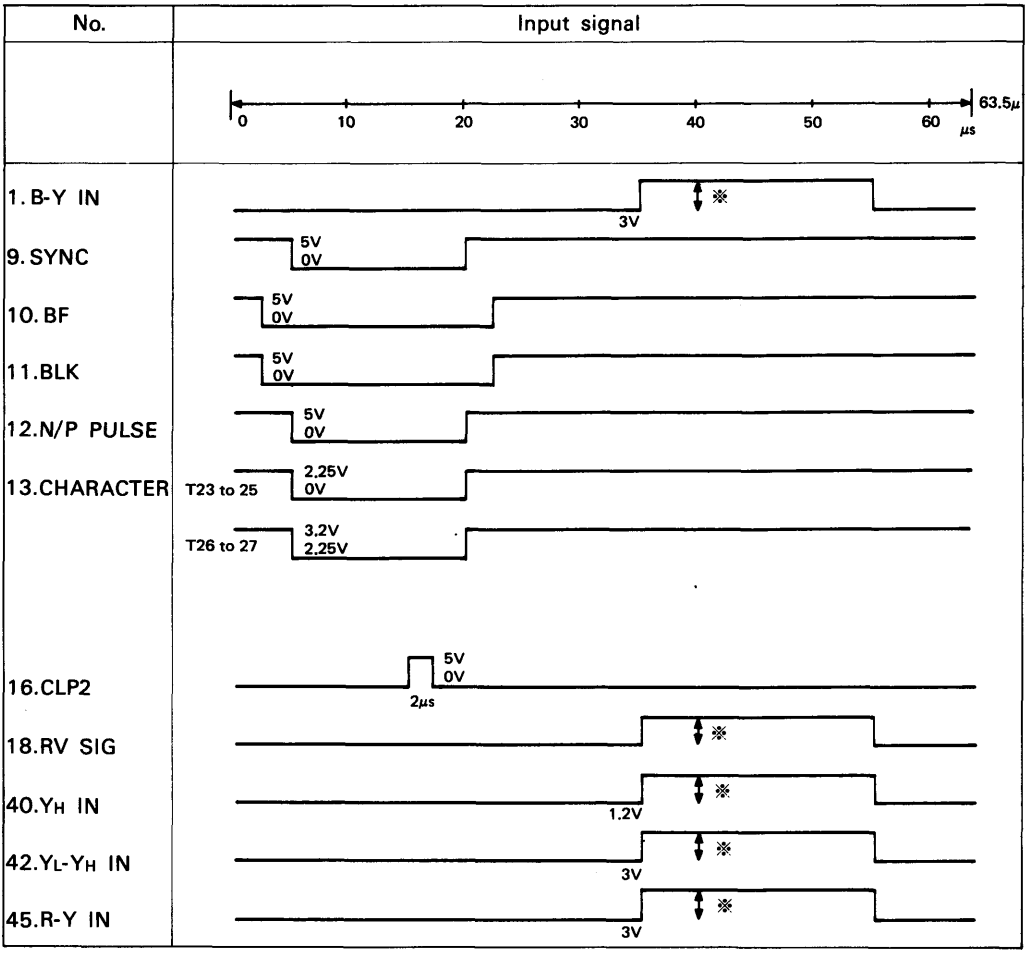
(2) 500 kHz BPF

The BPF where with an input of a 500 kHz sine wave the output becomes 1/2.



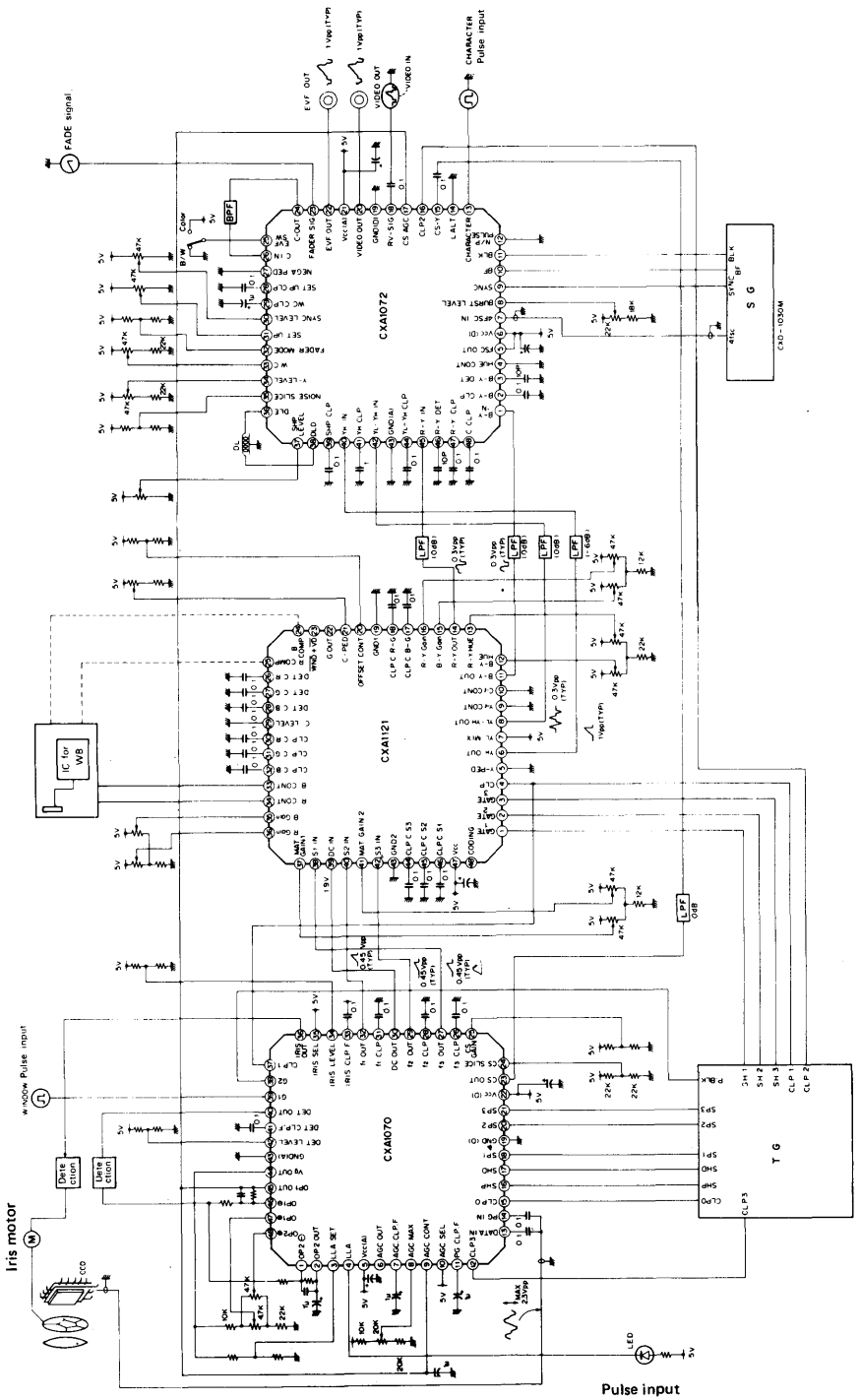
2. Pins shown with an input signal timing chart are indicated in the test circuit as ⊣⊢. However there is also a test where the signal is input.

Input Signal Timing Chart



Note) Level is indicated in the conditions shown in the chart.

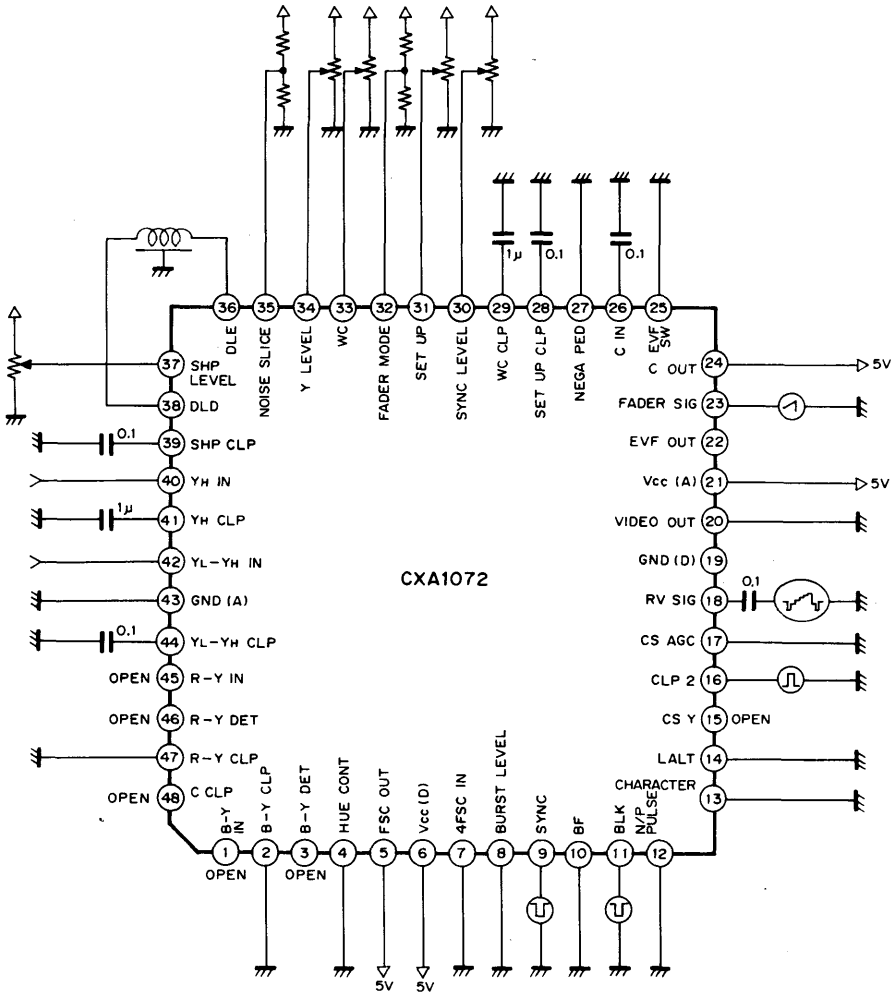
768H Color Compensation Stripe CCD Camera System Diagram



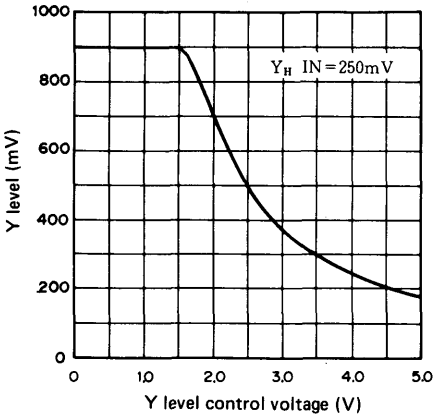
Note) 1. Resistances without value should better be set below 50 kΩ between V_{CC} and GND.
2. The unit of unspecified capacitance should be μF.

Application Circuit

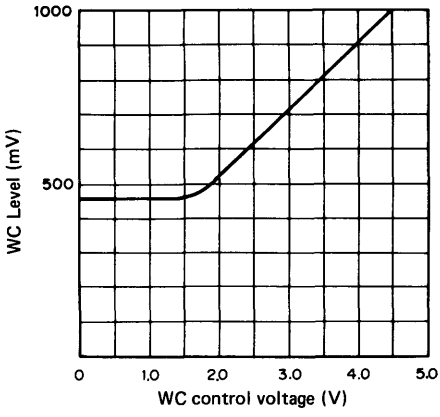
(During Black and White Mode)



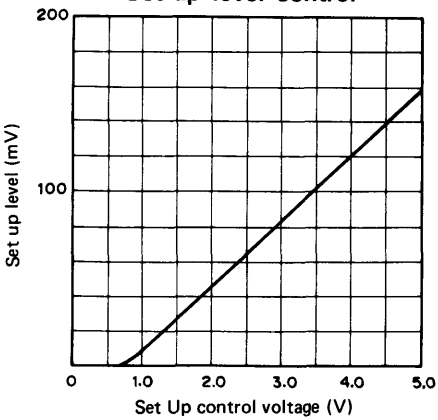
Y-levle control



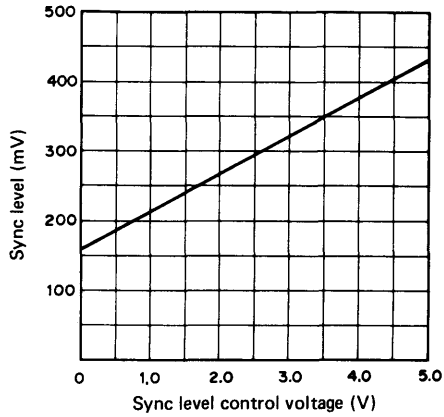
White clip level control



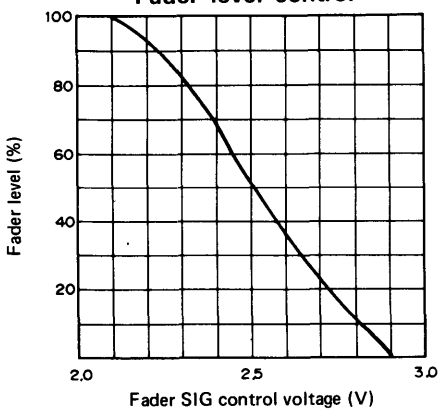
Set-up level control



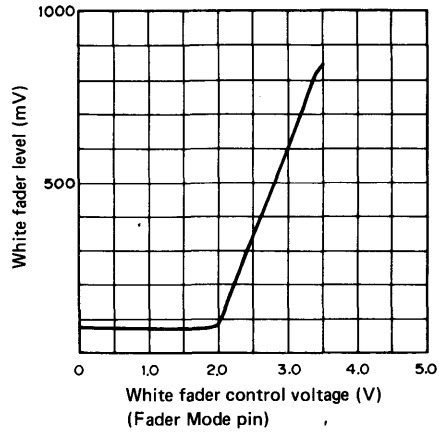
Sync level control



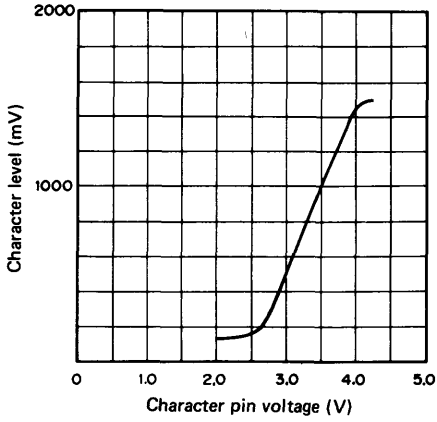
Fader level control



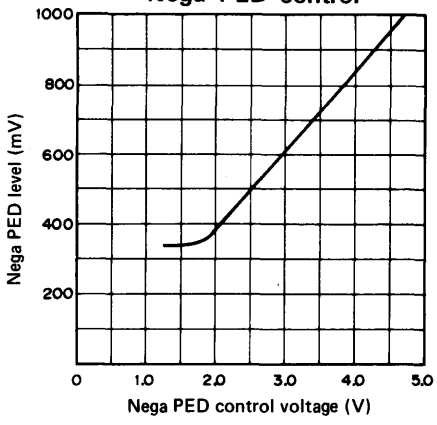
White fader level control



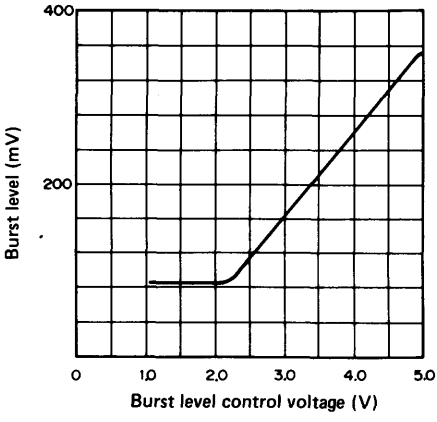
Character level control



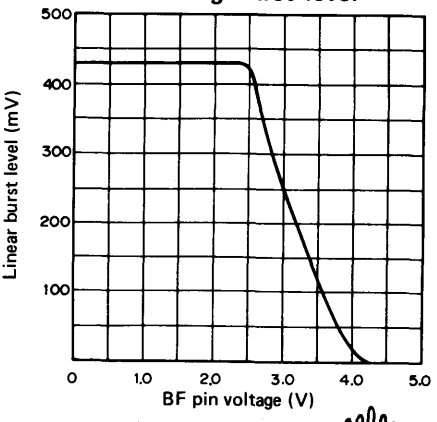
Nega PED control

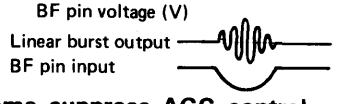


Burst level control

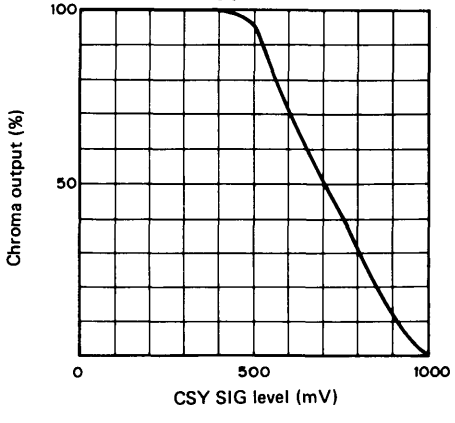


Analog burst level

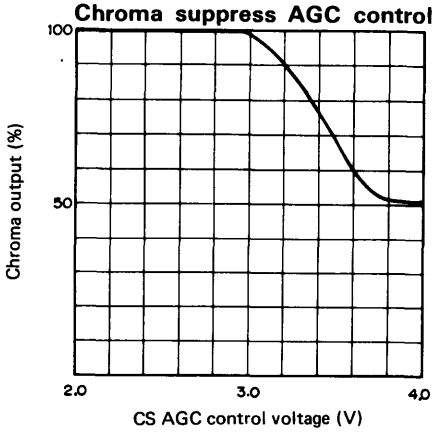




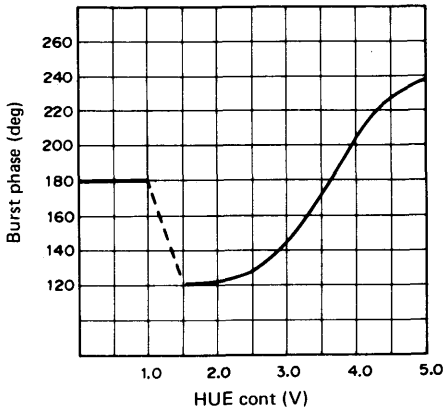
Chroma suppress Y control



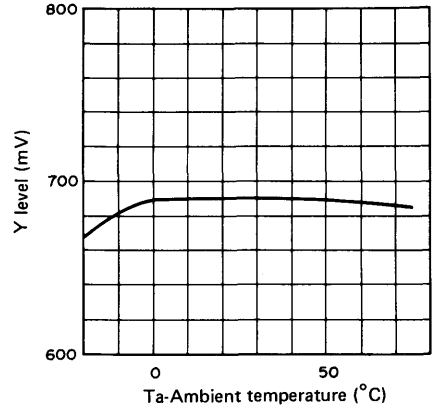
Chroma suppress AGC control



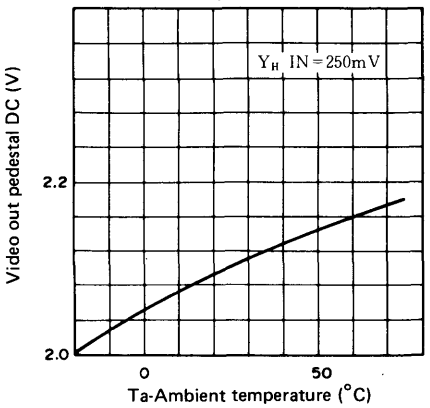
HUE control



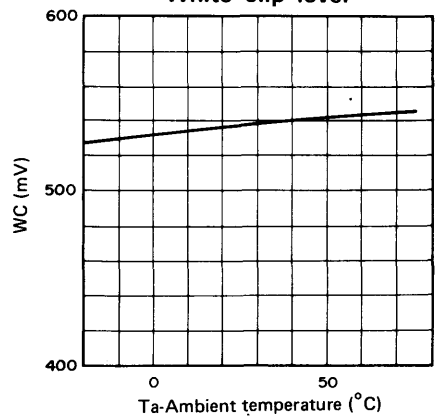
Y level



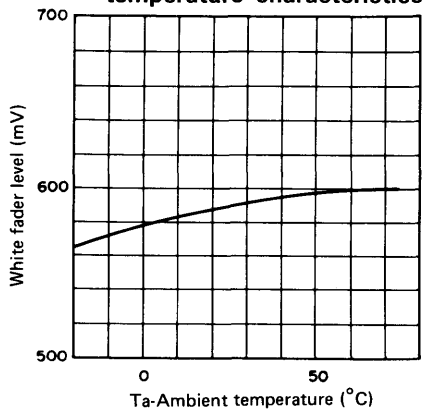
Video out pin pedestal DC



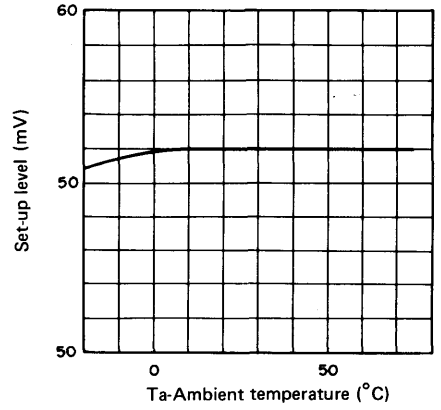
White clip level



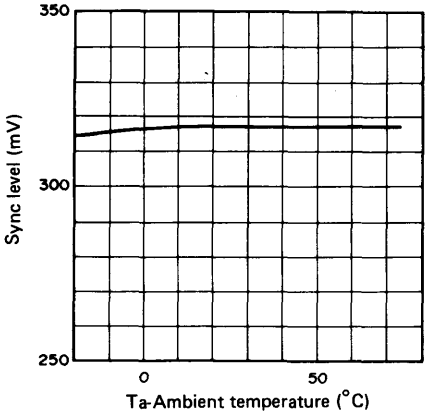
White fader level temperature characteristics



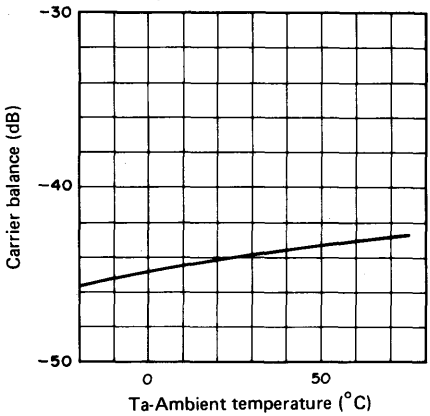
Set-up level temperature characteristics



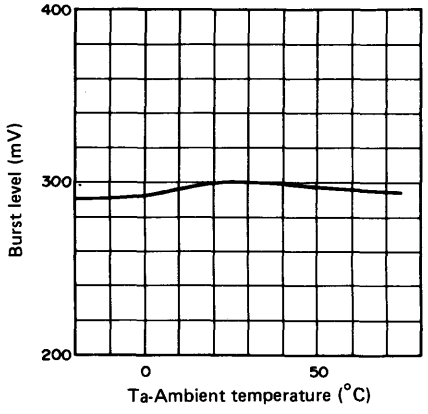
Sync level temperature characteristics



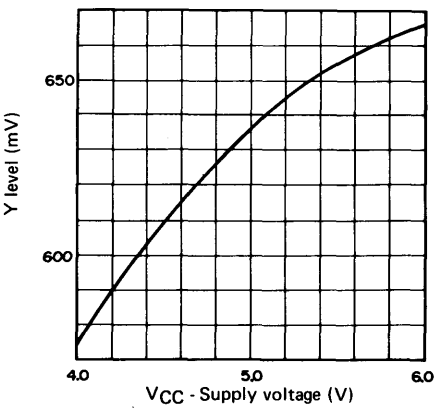
Carrier balance 3.58 MHz temperature characteristics



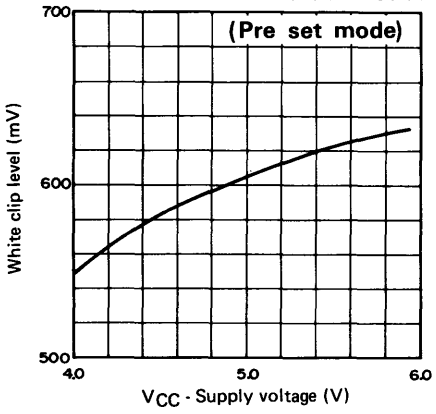
Burst level temperature characteristics



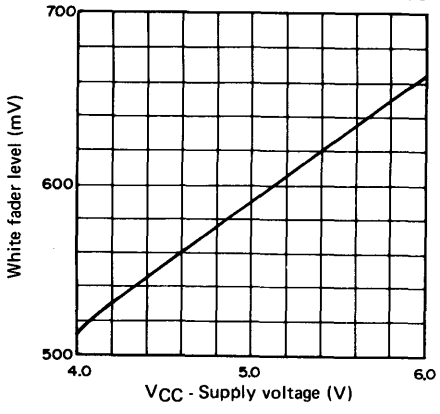
Y level supply fluctuations characteristics



White clip level supply fluctuations characteristics



White fader supply fluctuations characteristics



SONY CXL1503M/1505M

CMOS-CCD Signal Processor

Description

CXL1503M and CXL1505M are CMOS-CCD signal processors developed for CCD camera complementary color filter array processing system.

CXL1503M 1H×4 301.5 bit CCD delay line
CXL1505M 1H×4 453.5 bit CCD delay line

Features

- Single power supply 5V
- Low power consumption
  CXL1503M 100mW (Typ.)
  CXL1505M 150mW (Typ.)
- Built-in peripheral circuits
- Built-in CDS(Correlated Double Sampling) circuit

Function

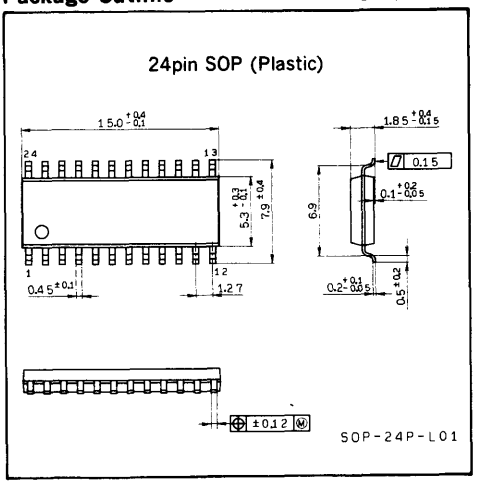
- Clock driver
- Autobias circuit (center and black)
- Pedestal clamp circuit
- CDS circuit

Structure

CMOS-CCD

Package Outline

Unit : mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	T_{opr}	−10 to +60	°C
• Storage temperature	T_{stg}	−55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Recommended Operating Conditions (Ta=25°C)

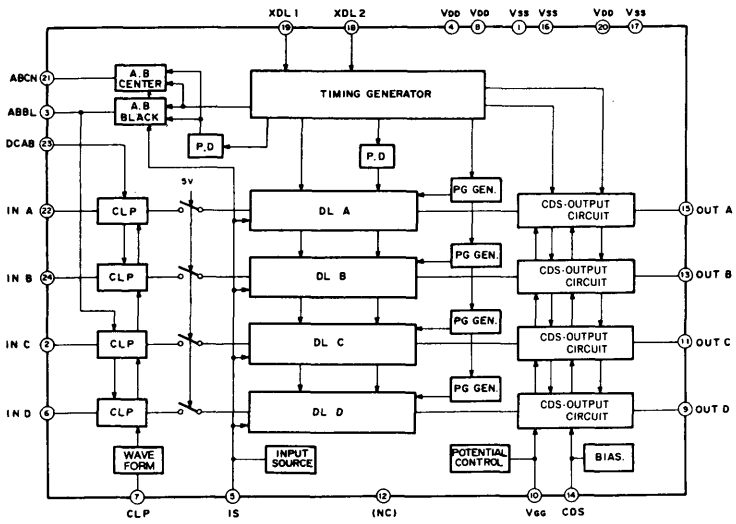
• Supply voltage	V_{DD}	5 ±5%	V

Recommended Clock Conditions (Ta=25°C)

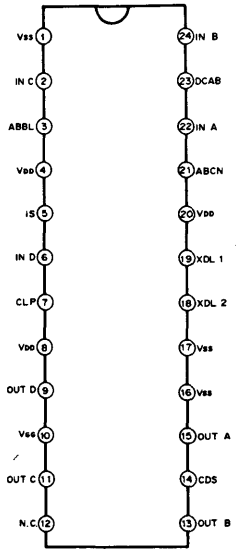
Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock voltage Low		V_L	0		1.0	V	
Clock voltage High		V_H	V_{DD}−1.0		V_{DD}	V	
Clock frequency	CXL1503M	f_{CL}		4.77		MHz	NTSC: 910f_H/3 CCIR: 908f_H/3
	CXL1505M	f_{CL}		7.16		MHz	NTSC: 455f_H CCIR: 454f_H

E89174-HP

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description	Impedance(Ω)
1, 16, 17	V_{SS}	—	GND	
2	IN C	I	Signal input C channel	>100k (at no clamp)
3	ABBL	O	Autobias DC output for Y signal	2k to 20k
4, 8, 20	V_{DD}	—	5V power supply	
5	IS	O	Input source DC output	5k
6	IN D	I	Signal input D channel	>100k (at no clamp)
7	CLP	I	Clamp pulse input	>100k
9	OUT D	O	Signal output D channel	50 to 500
10	V_{GG}	O	Gate bias DC output	2k to 10k
11	OUT C	O	Signal output C channel	50 to 500
12	N.C.	—	—	
13	OUT B	O	Signal output B channel	50 to 500
14	CDS	O	DC output for CDS	500 to 5k
15	OUT A	O	Signal output A channel	50 to 500
18	XDL2	I	Clock pulse input 2	>100k
19	XDL1	I	Clock pulse input 1	>100k
21	ABCN	O	Autobias DC output for C signal	2k to 20k
22	IN A	I	Signal input A channel	>100k (at no clamp)
23	DCAB	I	DC bias input for A and B channel	>100k
24	IN B	I	Signal input B channel	>100k (at no clamp)

Electrical Characteristics (Ta = 25°C, V_{DD}=5.0V, V_{SS}=0V) f_{CL}=4.77MHz (CXL1503M) f_{CL}=7.16MHz (CXL1505M)

Item		Symbol	Test point	SW position SW1	SW2	SW3	SW4 to 7	Bias condition E1	Conditions	Min.	Typ.	Max.	Unit
Autobias Center level		ABCN	V_1	a	b	a	a			1.0	2.0	4.0	V
Autobias Black level		ABBL	V_2	a	b	a	a			1.2	2.2	4.2	V
Input source level		IS	V_3	a	a	a	a			0.3	0.6	3.0	V
CDS source level		CDS	V_4	a	a	a	a			1.2	2.3	3.5	V
Output circuit bias level		V_{GG}	V_5	a	a	a	a			0.3	0.8	3.0	V
*Supply current	CXL1503M	I_{DD}	A_1	b	a	a	a	V_1		—	20	35	mA
	CXL1505M									—	30	40	
Insertion gain		IG	V_6	b	b	a to d	a	A, Bch → V_1 C, Dch → V_2 −0.2V	$20\log\frac{\text{Output amplitude (mVp-p)}}{\text{Input amplitude (SIN100kHz, 100mVp-p)}}$	−4.5	−3.5	—	dB
*Frequency response	CXL1503M	f_G	V_6	c	b	a to d	a	↓	$20\log\frac{\text{Output amplitude (SIN1MHz, 100mVp-p)}}{\text{Output amplitude (SIN100kHz, 100mVp-p)}}$	−1.8	−0.8	—	dB
	CXL1505M									−1.5	−0.4	—	
Linearity		Lin.	V_6	b	b	a to d	a	↓	(Note 1)	0	5	12	%
Insertion gain difference between channels		ΔG							(Note 2)	0	5	15	%
Linearity difference between channels	Ach ↔ Bch	ΔL_{AB}							(Note 3)	0	1	5	%
	Cch ↔ Dch	ΔL_{CD}							(Note 3)	0	1	5	%
Cross talk between channels		CRT	V_6	a	b	a to d	a ↔ b	A, Bch → V_1 C, Dch → V_2−0.2V	(Note 4)	0	1	3	%

* **Note)** Standard values are different between CXL1503M and CXL1505M.

Note

1. Linearity testing

For A channel and B channel, set input bias E_1 to ABCN +0.2(V) first, and then set it to ABCN(V) and ABCN −0.2(V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes.

For C channel and D channel, set input bias E_1 to ABBL −0.4(V) first, and then set it to ABBL −0.2(V) and ABBL(V). Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes.

The maximum output amplitude for the respective A, B, C and D channels is taken as Sout max. and the minimum output amplitude as Sout min. The linearity of the respective channels is defined as

$$\text{Lin.} = \frac{\text{Sout max} - \text{Sout min}}{\text{Sout max} + \text{Sout min}} \times 200\ (\%)$$

2. Calculation of insertion gain difference

As the max. insertion gain among A, B, C and D channels' is taken as Gmax and the min. as Gmin., the insertion gain difference between channels becomes:

$$\Delta G = \text{ABS}\left(1 - 10^{\left(\frac{Gmax - Gmin}{20}\right)}\right) \times 100\ (\%)$$

3. Calculation of linearity difference

Define Ach linearity as L_A, and Bch linearity as L_B we obtain the difference ΔL_{AB} as

$$\Delta L_{AB} = |\, L_A - L_B \,|\ (\%)$$

Similarly we obtain the linearity difference ΔL_{CD} of Cch and Dch as

$$\Delta L_{CD} = |\, L_C - L_D \,|\ (\%)$$

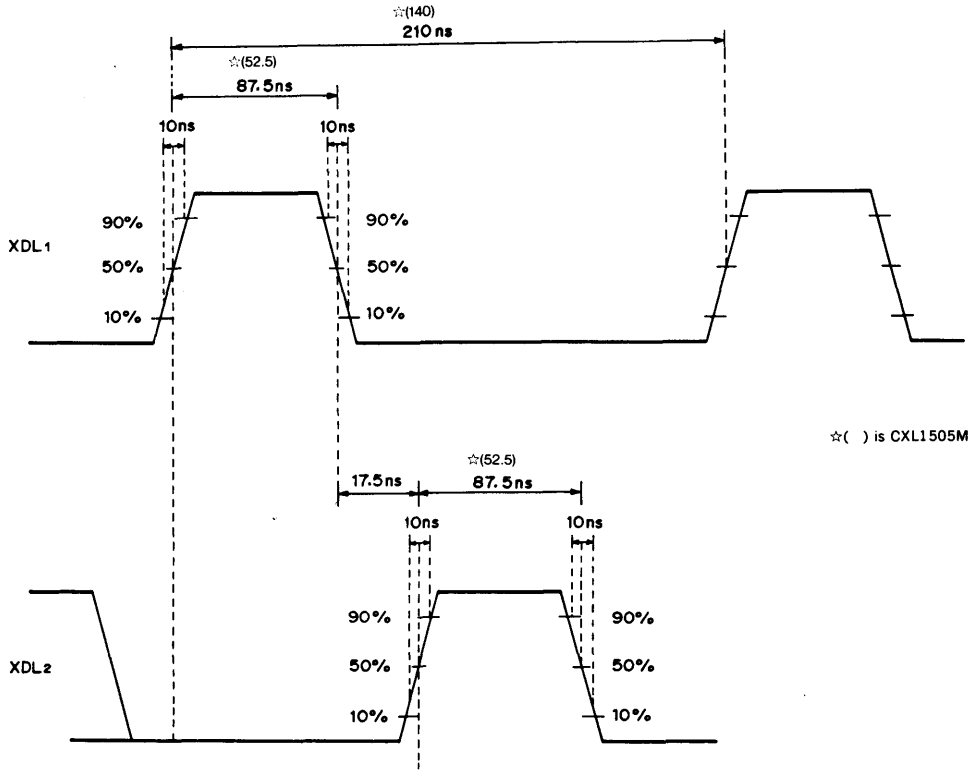
4. Crosstalk calculation

We take CRT_a as: Ach crosstalk value only during Bch input
CRT_b as: Bch crosstalk value only during Ach input
CRT_c as: Cch crosstalk value only during Dch input
CRT_d as: Dch crosstalk value only during Cch input

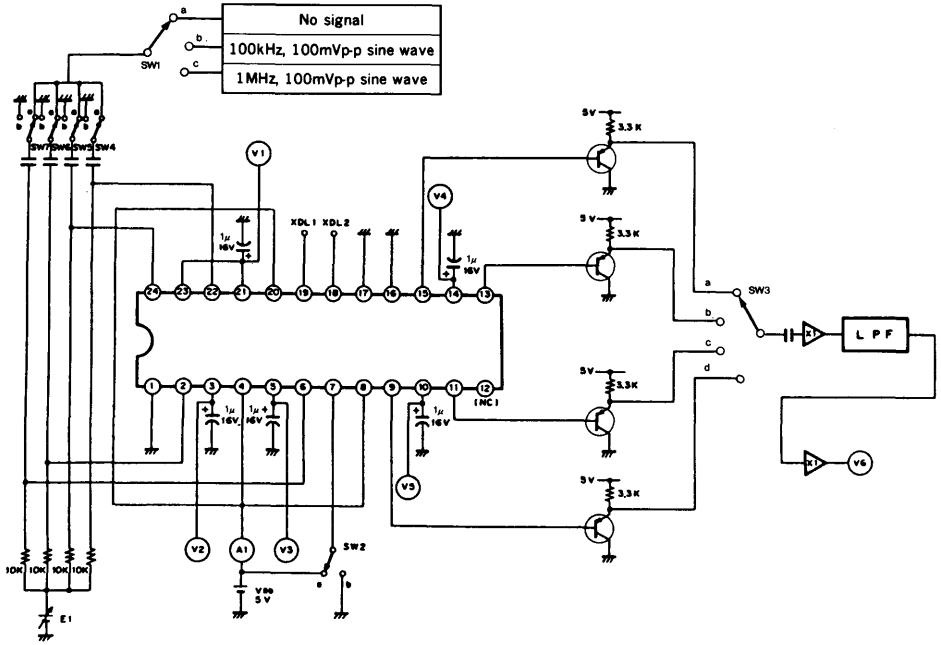
The crosstalk value of respective channels becomes:

$$CRT_{a\ to\ d} = \frac{\text{Crosstalk component}}{\text{Each channel output value}} \times 100\ (\%)$$

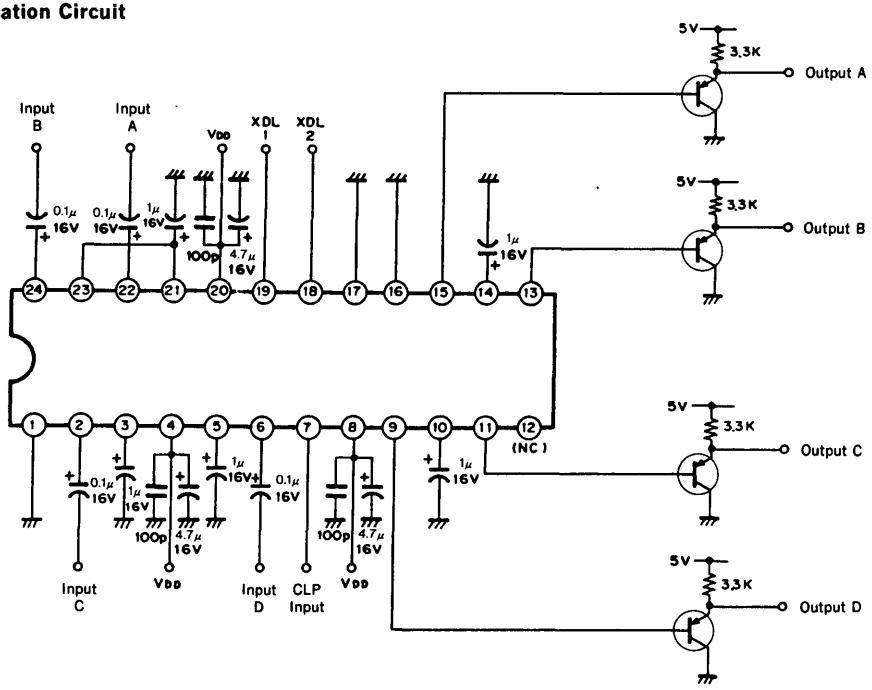
Clock Waveform Timing



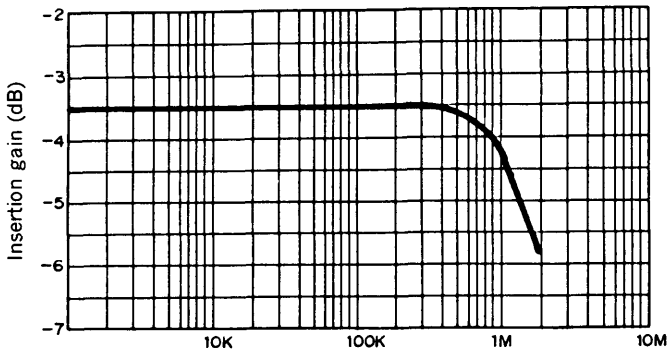
Electrical Characteristics Test Circuit



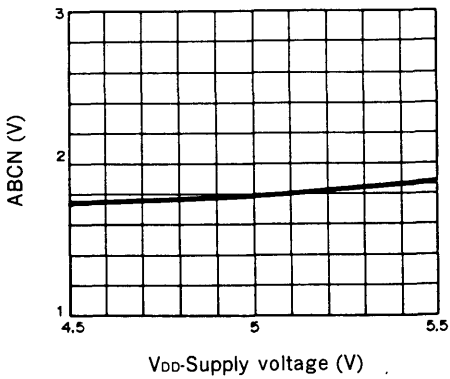
Application Circuit



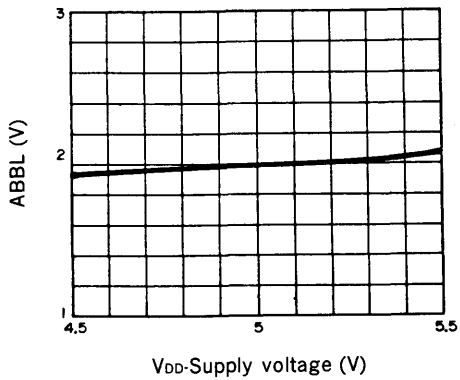
Frequency response



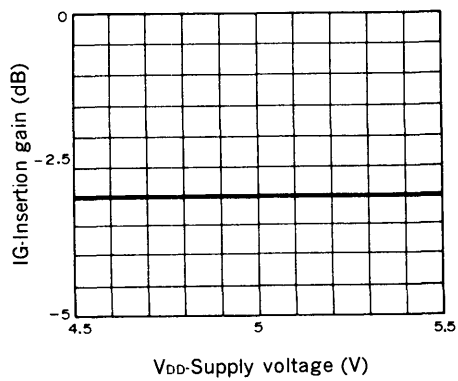
ABCN vs. Supply voltage



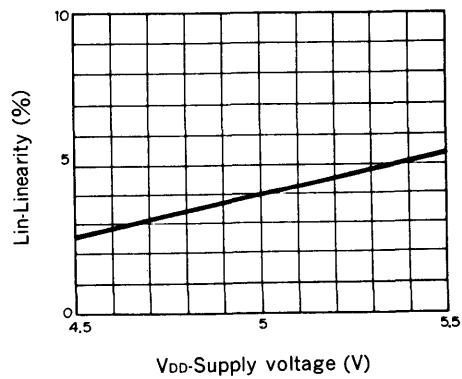
ABBL vs. Supply voltage



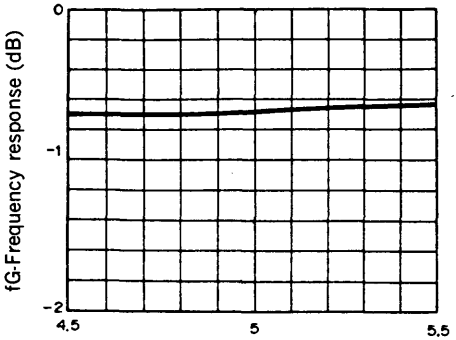
Insertion gain vs. Supply voltage



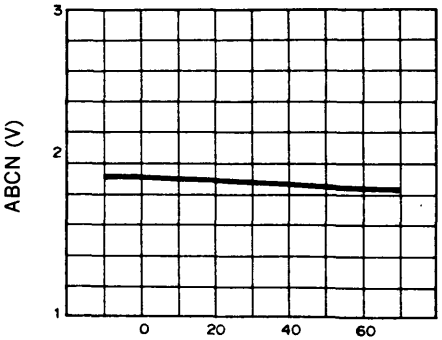
Linearity vs. Supply voltage



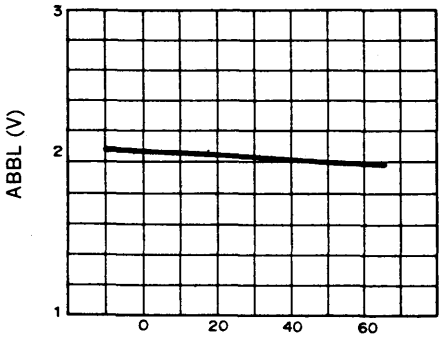
Frequency response vs. Supply voltage



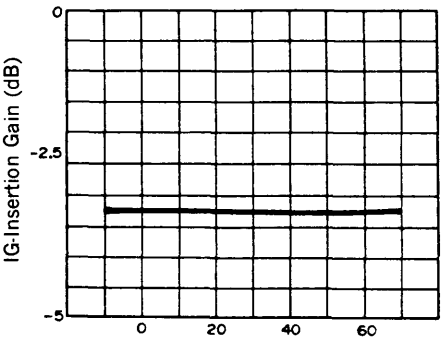
ABCN vs. Ambient temperature



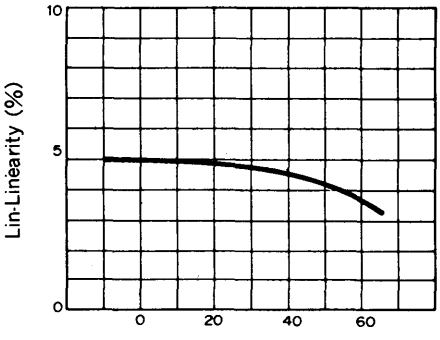
ABBL vs. Ambient temperature



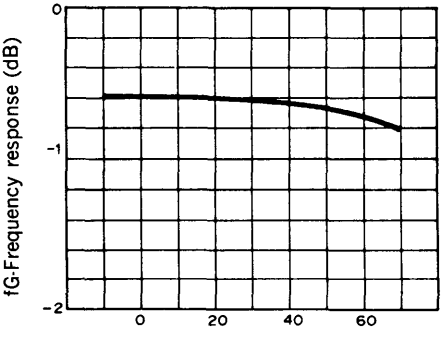
Insertion gain vs. Ambient temperature



Linearity vs. Ambient temperature



Frequency response vs. Ambient temperature



SONY CXL1504M

CMOS-CCD 1H Delay line for NTSC

Description

CXL1504M is a delay line used in conjunction with an external low pass filter. Through negative phase input and positive phase output 1H delay time is obtained for NTSC signals.

Features

- 5V single supply
- 14.3 MHz driver
- Low consumption at 160 mW (Typ.)
- Built-in peripheral circuits
- Completely adjustment free

Functions

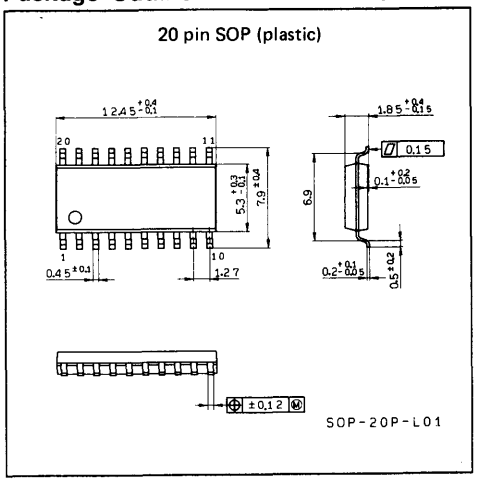
- 905.5bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage ambient temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Operating Voltage Range (Ta=25°C)

V_{DD} 5V±5%

Recommended Clock Conditions (Ta=25°C)

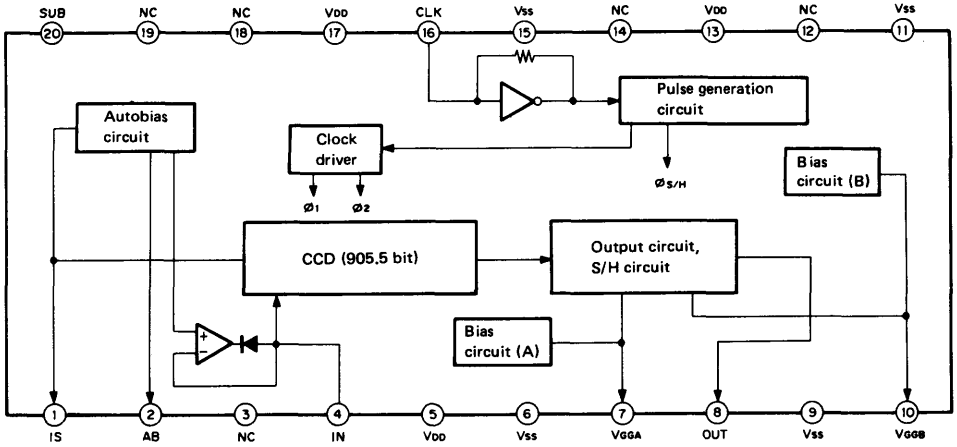
• Input clock amplitude	V_{CLK}	0.3 to 1.0	Vp-p (0.5 Vp-p Typ.)
• Clock frequency	f_{CLK}	14.318182	MHz
• Input clock waveform		sinewave	

Input Signal Amplitude

V_{SIG} 560(Max.) mVp-p

80128-ST

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description	Impedance [Ω]
1	IS	O	CCD bias DC output	600 to 2k
2	AB	O	Autobias DC output	2k to 20k
3	(NC)	–		
4	IN	I	Signal input (Negative phase signal)	>100k (at no clamp)
5	VDD	–	5V supply (For clock driver)	
6	Vss	–	GND	
7	VGGA	O	Gate bias (A) DC output	2k to 10k
8	OUT	O	Signal output (positive phase signal)	40 to 500
9	Vss	–	GND	
10	VGGB	O	Gate bias (B) DC output	2k to 10k
11	Vss	–	GND	
12	(NC)	–		
13	VDD	–	5V supply (for analog system)	
14	(NC)	–		
15	Vss	–	GND	
16	CLK	I	Clock input	4k to 50k
17	VDD	–	5V supply (for digital system)	
18	(NC)	–		
19	(NC)	–		
20	SUB	–	GND	

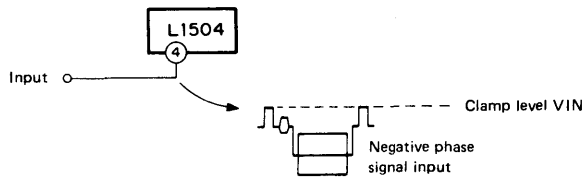
Electrical Characteristics

See the Electrical Characteristics Test Circuits

Ta=25°C, V_{DD}=5V, f_{CLK}=14.318182 MHz, V_{CLK}=500 mVp-p sinewave

Item	Symbol	Test conditions	SW conditions				*Note) Bias conditions V_{BIAS1} (V)	Min.	Typ.	Max.	Unit	Note
			1	2	3	4						
Supply current	I_{DD}	–	a	a	a	–	–	20	32	42	mA	1
Insertion gain	IG	200 kHz 500 mVp-p Sinewave	a	a	a	b	–	−5.0	−3.0	−1.0	dB	2
Frequency response	fr	200 kHz ↔3.58 MHz 150 mVp-p Sinewave	b↔c	a	b	b	VIN−0.2	−2.5	−1.3	0	dB	3
Differential gain	DG	5-staircase wave (See Note 4)	d	a	a	c	–	0	3	7	%	4
Differential phase	DP	5-staircase wave (See Note 4)	d	a	a	c	–	0	3	7	deg	4
S/H pulse coupling	CP	No-signal input	–	b	b	a	VIN	–	200	350	mVp-p	5
S/N ratio	S/N	50% white video signal (See Note 7)	e	a	a	d	–	54	56	–	dB	6

***Note)** VIN is defined as follows.
VIN is the input signal clamp level, it clamps the Video signal sync tip level.



VIN is the pin voltage for pin 4 at no-input signal. Testing is executed with a voltmeter under the following SW conditions.

Item	SW Conditions				Test point
	1	2	3	4	
VIN	–	b	a	–	V1

As VIN varies with each IC, they are all subject to testing.

1) I_{DD} is the IC supply current value during clock and signal input.

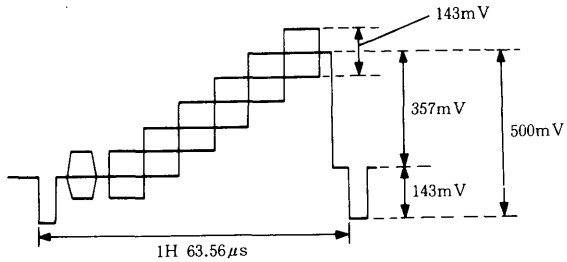
2) IG is the OUT pin output gain when a 500 mVp-p, 200 kHz sinewave is input to IN pin.

$$IG = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500\ \text{[mVp-p]}}\ \text{[dB]}$$

3) Indicates the dissipation at 3.58 MHz in relation to 200 kHz.
From the OUT output voltage when a 150 mVp-p, 200kHz sinewave is fed to IN pin and from the OUT pin output voltage when a 150 mVp-p, 3.58 MHz sinewave is fed to same, calculation is made according to the below formula. The input part bias is tested at VIN—0.2V.

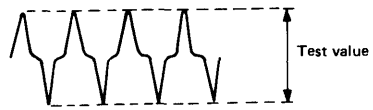
$$fr = 20 \log \frac{\text{OUT pin output voltage (3.58 MHz) [mVp-p]}}{\text{OUT pin output voltage (200 kHz) [mVp-p]}} [dB]$$

4) The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the fig. below is input are tested at the vector scope.

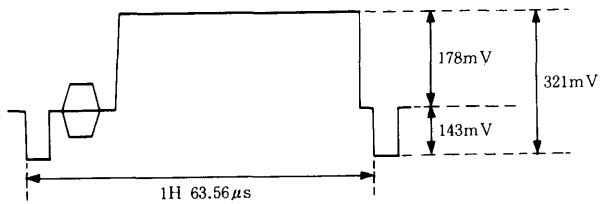


IN pin input waveform is the inverted waveform in the above Fig.

5) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input part bias is tested at VINV.



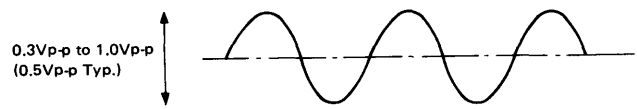
6) S/N ratio during 50% white video signal input shown in Fig. below is tested at video noise meter, in BPF 100 kHz to 4 MHz, Sub Carrier Trap mode.



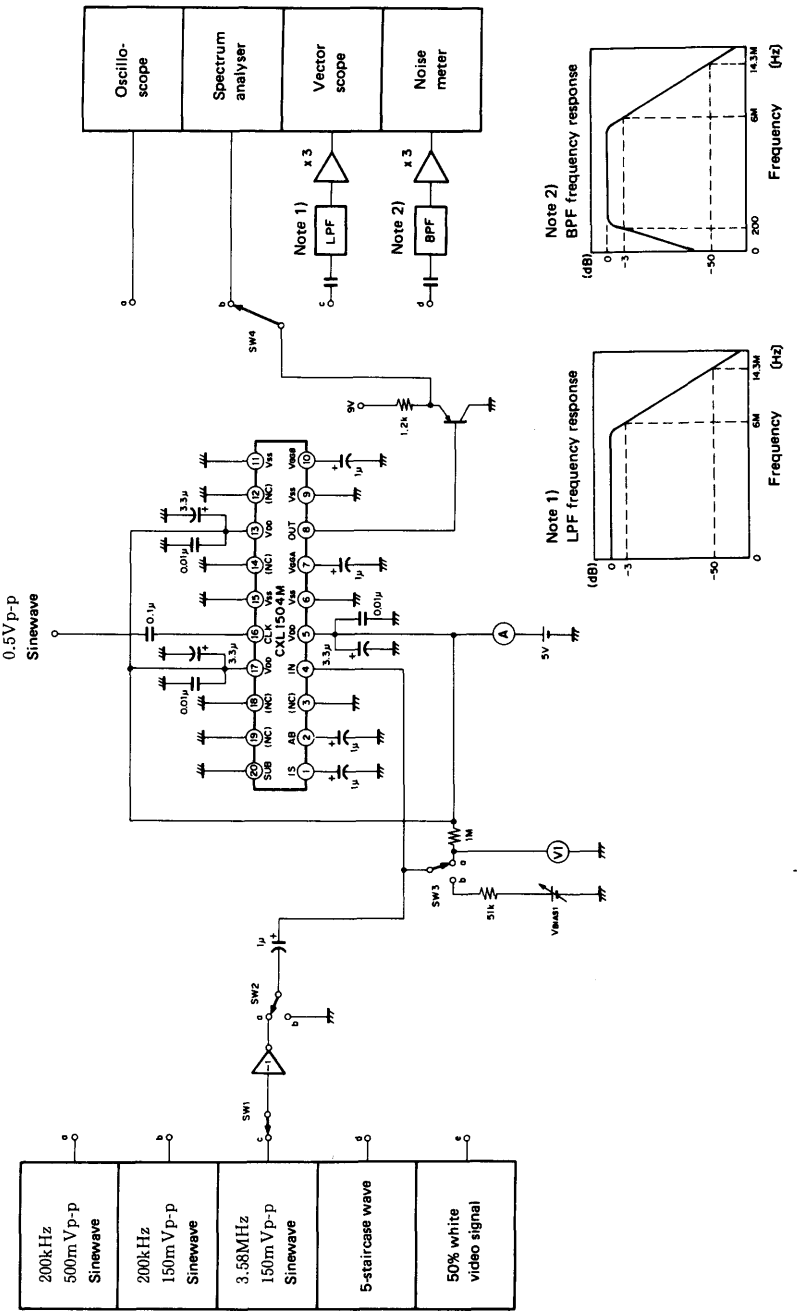
IN pin input waveform is the inverted waveform in the above Fig.

CLOCK

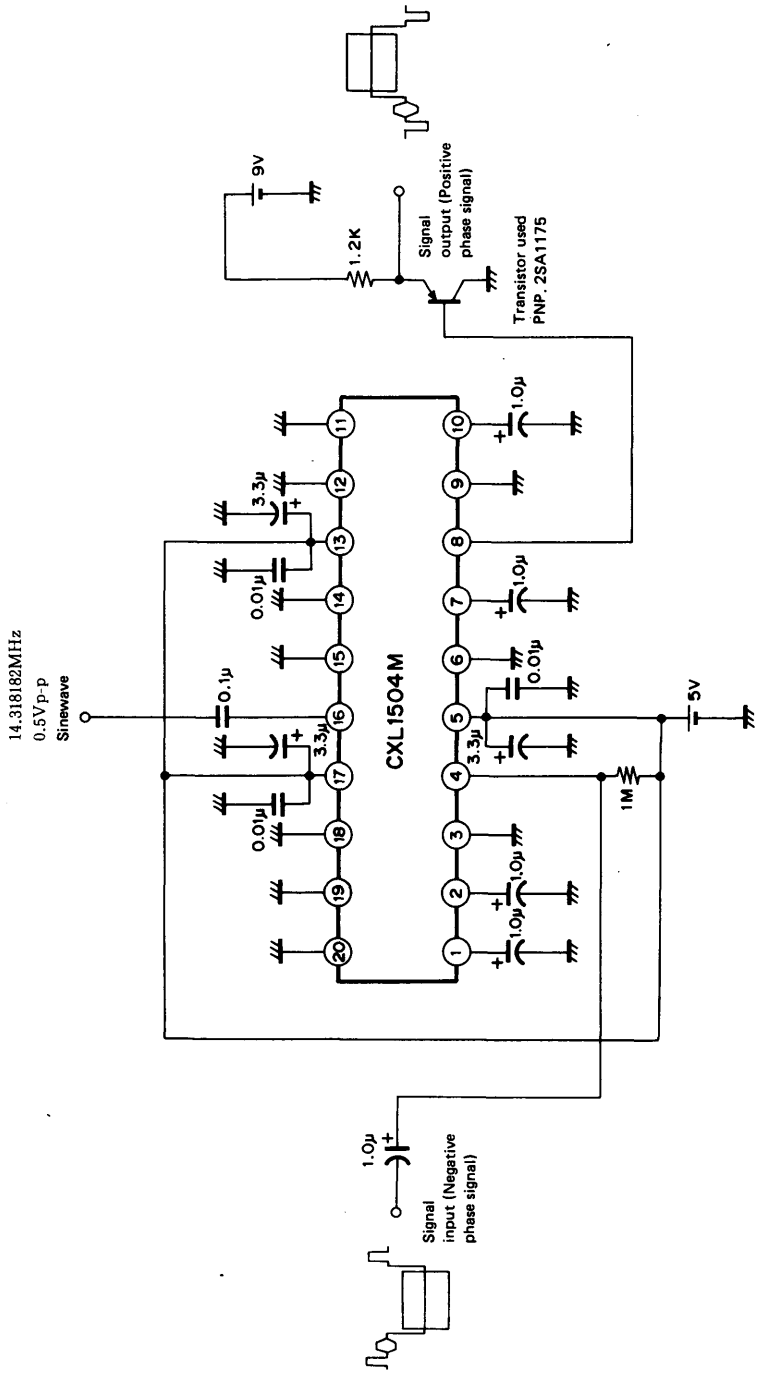
4fsc (14.318182MHz) sinewave



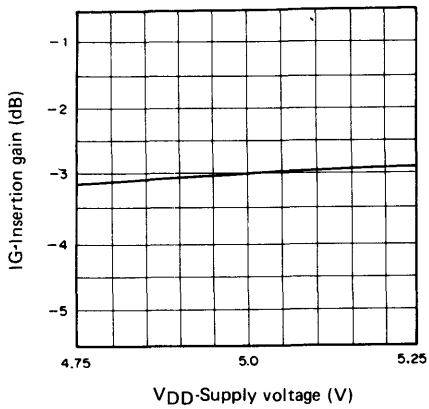
Electrical Characteristics Test Circuits



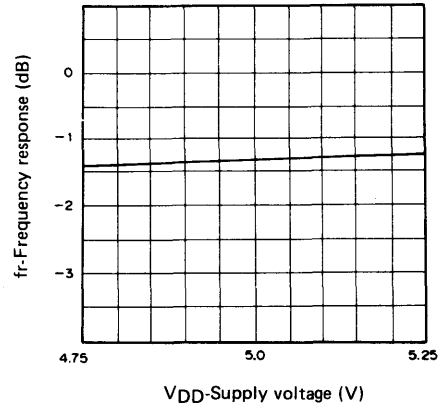
Application Circuit



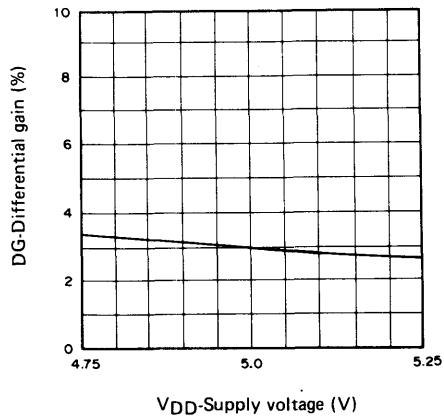
Supply voltage vs. Insertion gain



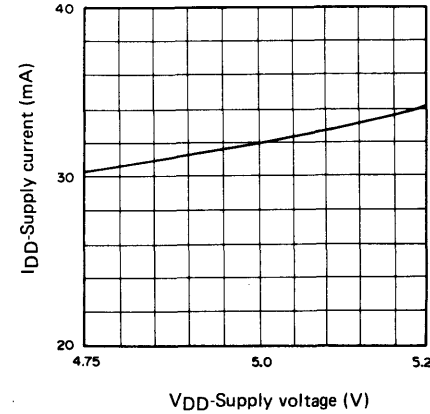
Supply voltage vs. Frequency response



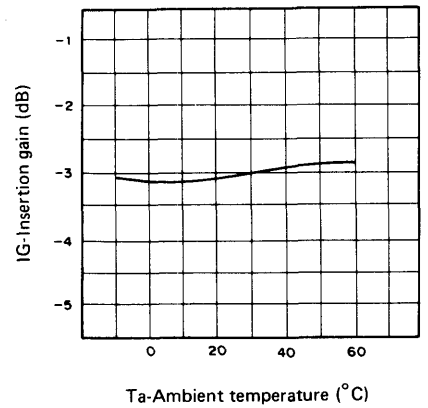
Supply voltage vs. Differential gain



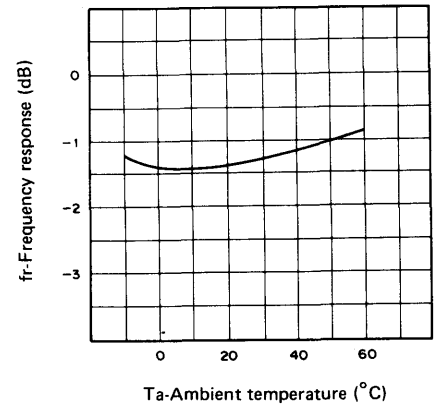
Supply voltage vs. Supply current



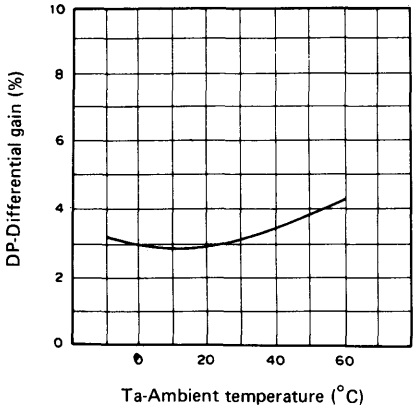
Ambient temperature vs. Insertion gain



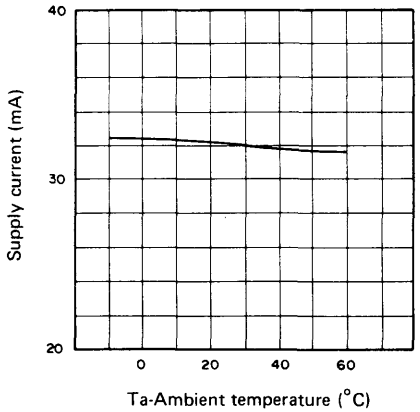
Ambient temperature vs. Frequency response



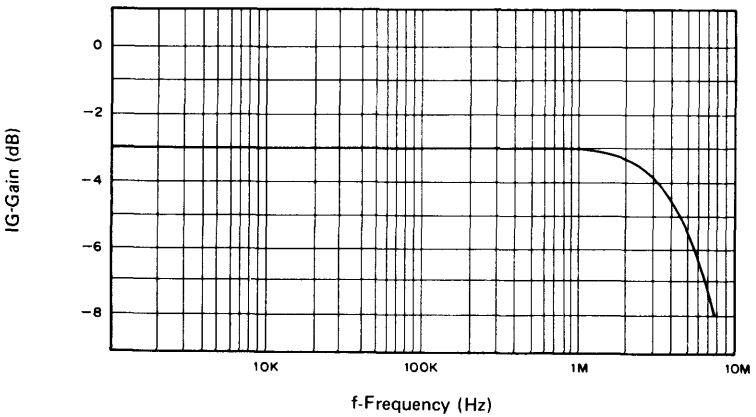
Ambient temperature vs. Differentical gain



Ambient temperature vs. Supply current



Frequency response



IC for Vertical Direction Outline Compensation

Description

CXA1270N is a bipolar IC developed for vertical outline compensation of video camera. It contains all the required functions for vertical outline compensation in a single chip. Also, being a small package, this IC is most suitable for the use in video camera.

20pin VSOP (Plastic)

Features

- Low power consumption
- Usable both in 2H type and 1H type.
- Executes low level noise clip.
- Controlable output level.

Structure

Bipolar silicon monolithic IC

Applications

Video camera

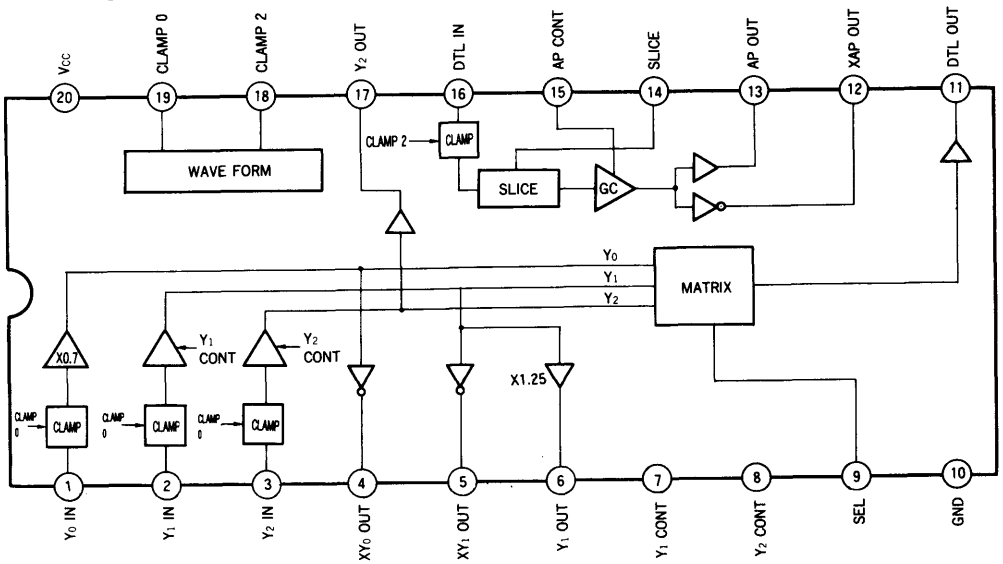
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	10	V
• Storage temperature	T_{stg}	−55 to +150	°C
• Operating temperature	T_{opr}	−20 to +75	°C
• Allowable power dissipation	P_D	375	mW

Recommended Operating Condition

• Supply voltage	V_{CC}	4.75 to 5.25	V

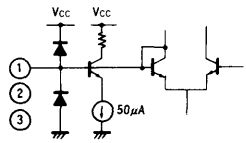
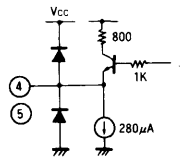
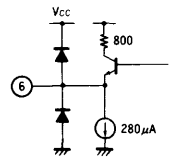
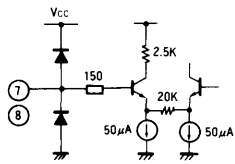
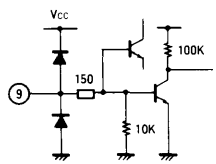
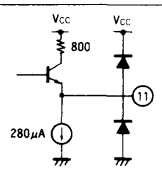
Block Diagram and Pin Configuration

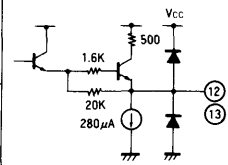
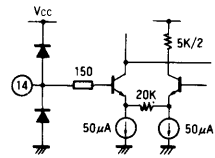
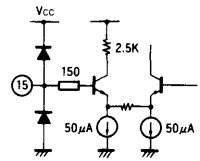
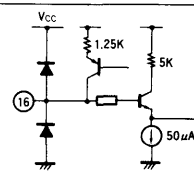
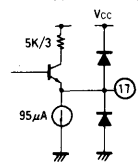
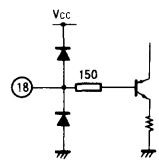
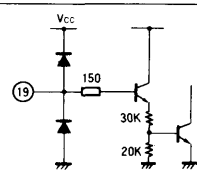


E89631-HP

Pin Description and Equivalent Circuit

V_{CC}=5V

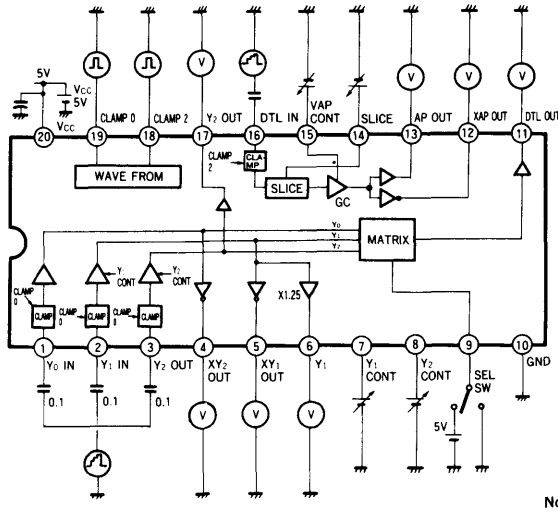
Pin No.	Symbol	Pin voltage	Equivalent Circuit	Description
1	V_0 IN	2.8V (Black level)		Y signal input pin (500Vp-p [Typ.])
2	Y_1 IN	2.8V (Black level)		Y signal input pin (1H delay) (150mVp-p [Typ.])
3	Y_2 IN	2.8V (Black level)		Y signal input pin (2H delay) (150mVp-p [Typ.])
4	XY_0 OUT	2.1V (Black level)		Y_0 A_{mp} inverse output pin
5	XY_1 OUT	2.0V (Black level)		Y_1 A_{mp} inverse output pin
6	Y_1 OUT	2.4V (Black level)		Y_1 A_{mp} output pin
7	Y_1 CONT	1.5V to 3.5V (Outside)		Y_1 A_{mp} gain control pin
8	Y_2 CONT	1.5V to 3.5V (Outside)		Y_2 A_{mp} gain control pin
9	SEL	Low 0V High 5V		Switching pin of 2H mode and 1H mode High (5V)=2H DL mode Low (0V)=1H DL mode
10	GND			GND pin
11	DTL OUT	2.9V		DETAIL signal output

Pin No.	Symbol	Pin voltage	Equivalent Circuit	Description
12	XAP OUT	2.8V		V aperture signal inverse output pin
13	AP OUT	2.8V		V aperture signal output pin
14	SLICE	2V to 4.0V (Outside)		Control pin at SLICE level
15	AP CONT	2V to 4.0V (Outside)		Aperture amplifier (AP AMP) gain control pin
16	DTL IN	3.1V (Black level)		Pin which inputs luminance difference signal (Pin 11) output {Input DTL (DETAIL) OUT signal through external low pass filter.}
17	Y_2 OUT	2.1V		Y_2 A_{mp} output pin
18	CLP2	Pulse		Clamp pulse input pin
19	CLP0	Pulse		Clamp pulse input pin
20	V_{CC}			Supply pin (5V)

Electrical Characteristics Ta=25°C, V_{CC}=5V

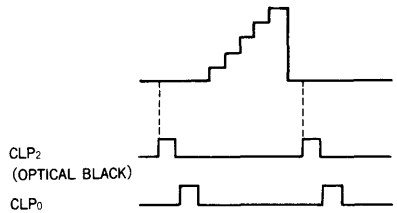
No.	Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
1	Consumption current	ID		6	8	10	mA
2	XY_0 OUT GAIN	XY_0	20 log $\frac{\text{Pin 4 output level}}{\text{Pin 1 input level}}$	−4.6	−3.3	−2.0	dB
3	XY_1 OUT GAIN	XY_1 L	20 log $\frac{\text{Pin 5 output level}}{\text{Pin 2 input level}}$ Y_1 CONT=1.5V			7	dB
		XY_1 H	Y_1 CONT=3.8V	11			dB
4	Y_1 OUT GAIN	Y_1 L	20 log $\frac{\text{Pin 6 output level}}{\text{Pin 5 output level}}$ Y_1 CONT=1.5V	1	2	3	dB
5	Y_2 OUT GAIN	Y_2 L	20 log $\frac{\text{Pin 17 output level}}{\text{Pin 3 input level}}$ Y_2 CONT=1.5V			7	dB
		Y_2 H	Y_2 CONT=3.8V	11			dB
6	AP OUT GAIN	AP	Gain from Pin 16 input to Pin 13 output Conditions { SLICE=0V, AP CONT=1.5V Input 1 (DTL IN) — $V_{IN}1$ Output 1 (AP OUT) — $V_{OUT}1$ Input 2 (DTL IN) — $V_{IN}2$ Output 2 (AP OUT) — $V_{OUT}1$ AP OUT GAIN=20 log $\frac{V_{OUT}2-V_{OUT}1}{V_{IN}2-V_{IN}1}$	6			dB
7	SLICE	SL	Slice level= DTL IN−(AP OUT×$\frac{V_{OUT}2-V_{OUT}1}{V_{IN}2-V_{IN}1}$) Pin 16 input — Slice level — AP CONT=3V (Pin 16 input conversion slice level) SLICE=3V	60	100	140	mV

Electrical Characteristics Test Circuit

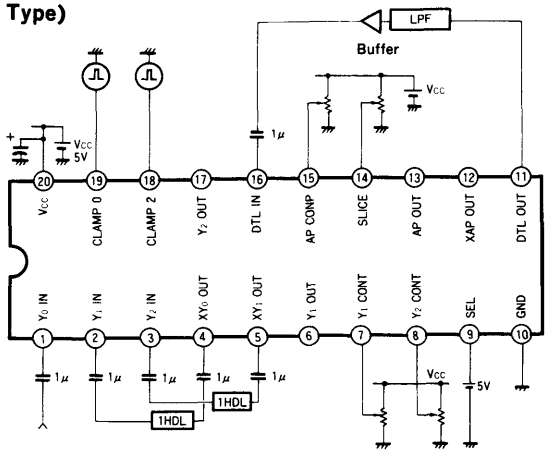


Note) 1. The unit of capacitor is in μF.

2. V indicate Test Pin.



Application circuit (2H Type)

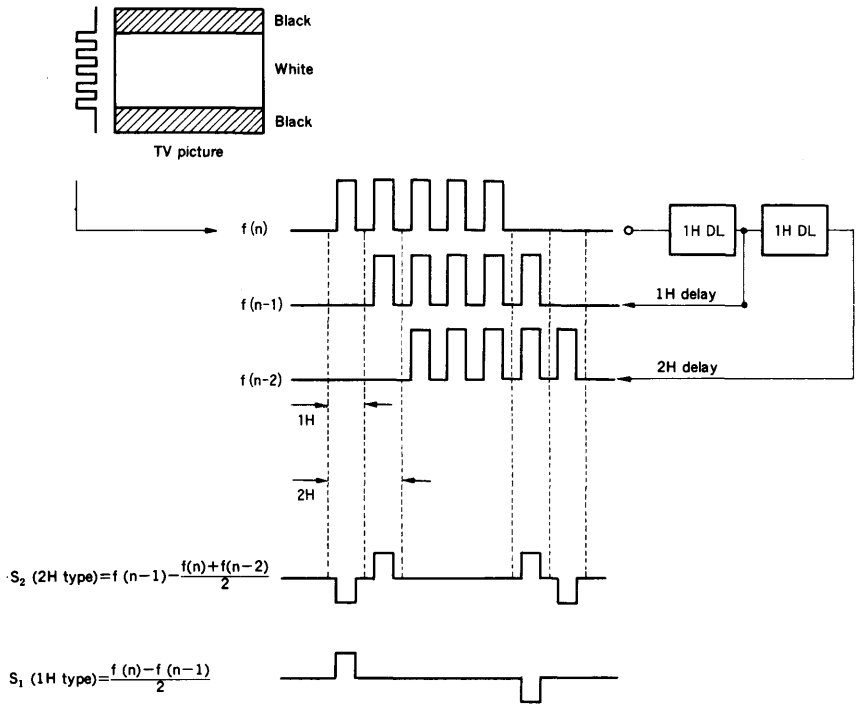


Note) 1. LPF is an abbreviation for Low Pass Filter.

2. DL is an abbreviation for Delay Line

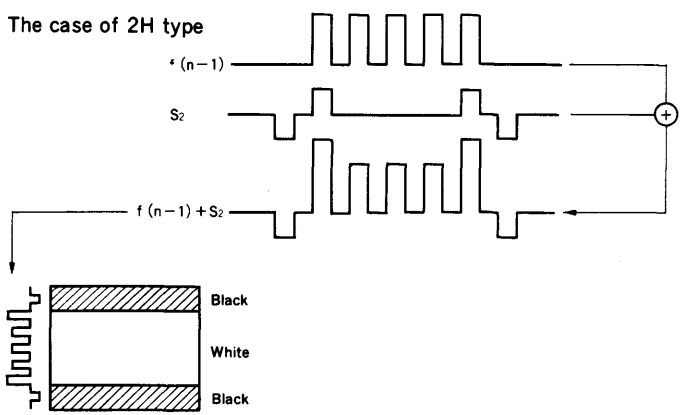
3. DTL is an abbreviation for DETAIL.

Operation

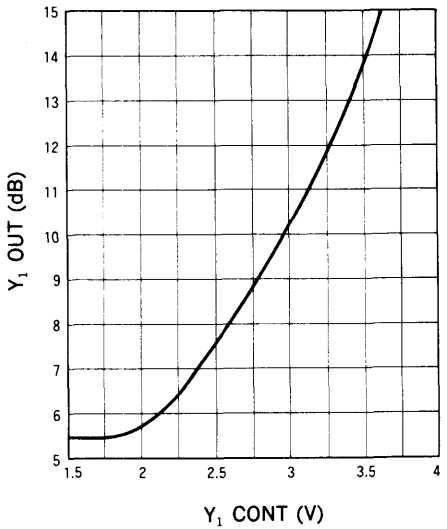


It can execute vertical direction outline emphasis by composing S_1 or S_2 with a Y signal.

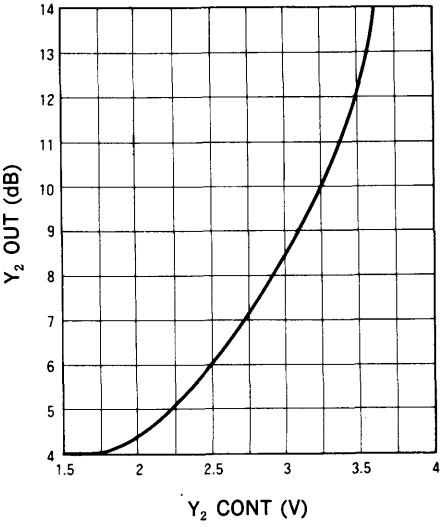
Example) The case of 2H type



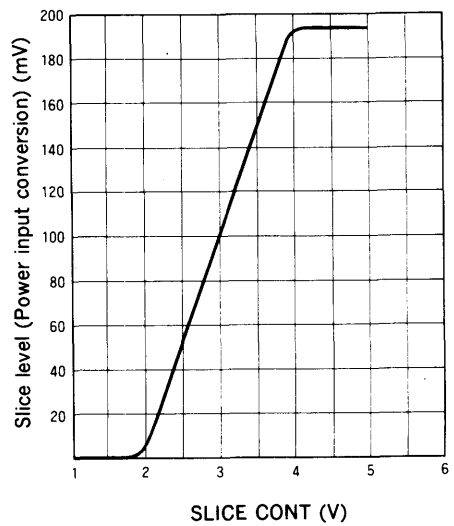
Y_1 Amp control characteristics



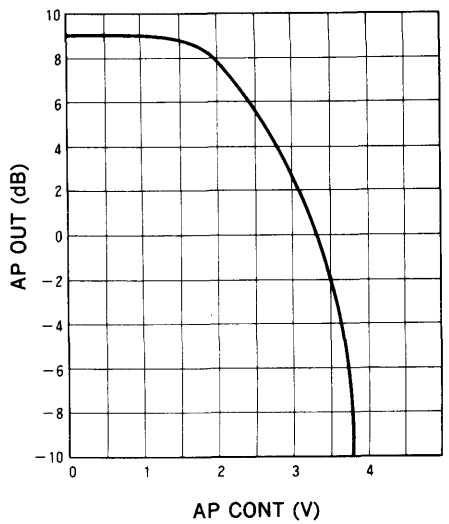
Y_2 Amp control characteristics



Slice level (Power input conversion)



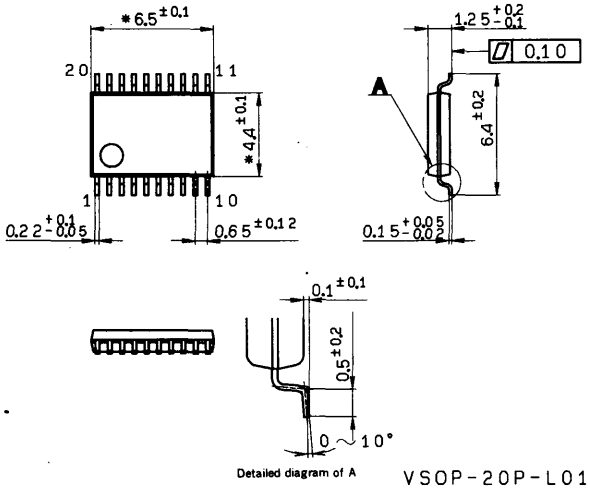
AP Amp control characteristics



Note) See the Electrical Characteristics P.4, No.7

Package Outline **Unit : mm**

20pin VSOP (Plastic) 250mil



Detailed diagram of A

VSOP-20P-L01

Note) Dimensions marked with * do not include residual resin.

Video Output

Description

The CX20095A/CX20186 is a bipolar IC designed as a driver of 75 Ω line (transmission and receiving line) used in the video signal system. It is comprised of a 75 Ω line drive, receiving amplifier and 6dB amplifier for multi-purpose applications.

Features

- Low power supply voltage operation, Vcc = 5V (Standard).
- Transmission/Receiving amplifier has a built-in sync chip clamp.
- Bilateral communication configuration is possible with one line.
- Driver amp and 6dB amp are provided with power-saving function.
- Simple superimpose is possible with the trans amp.

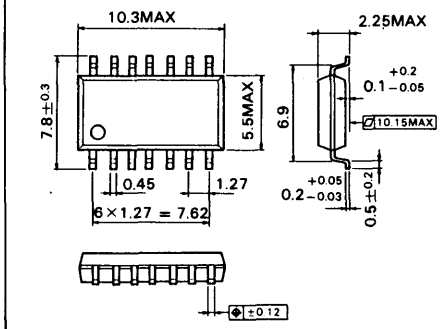
Structure

Bipolar silicon monolithic IC

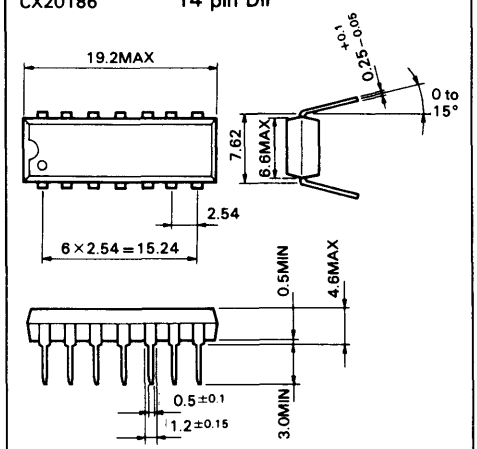
Package Outline

Unit: mm

CX20095A 14 pin SOP



CX20186 14 pin DIP



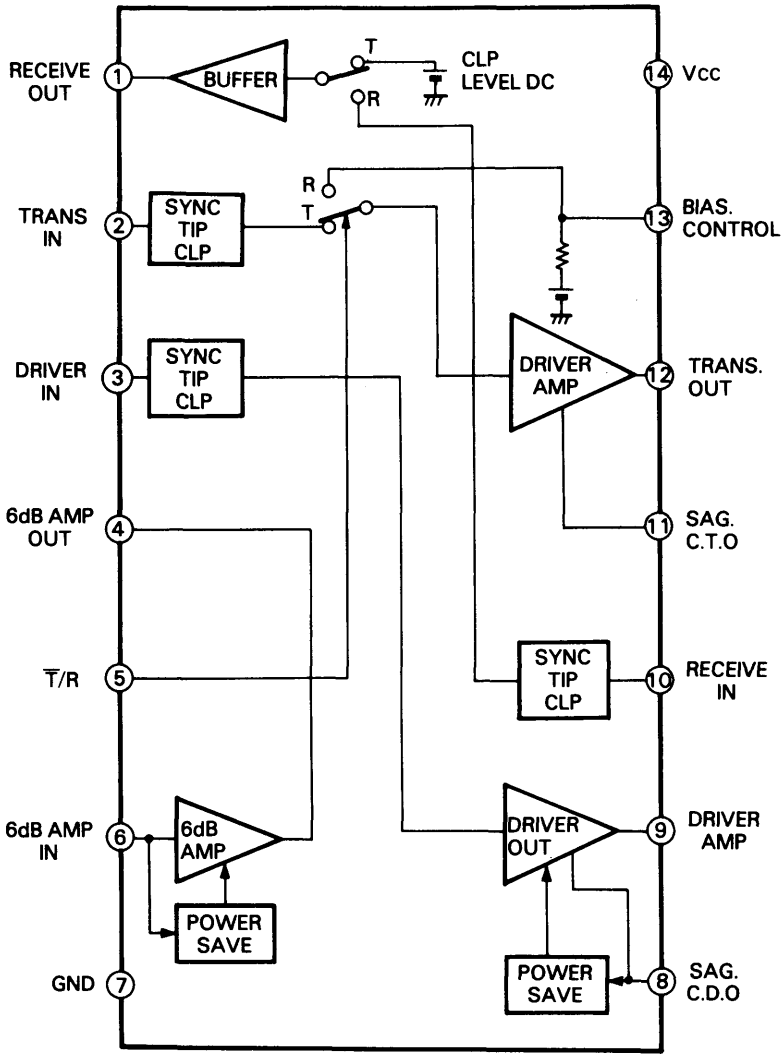
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc		17	V
• Operating temperature	Topr		−10 to +65	°C
• Storage temperature	Tstg		−55 to +150	°C
• Allowable power dissipation	PD	CX20095A	500	mW
		CX20186	650	mW

Recommended Operating Condition

• Supply voltage	Vcc	4.8 to 5.2	V

Block Diagram and Pin Configuration (Top view)



Pin Description

Standard terminal voltage (DC voltage when no signal is input, Ta = 25°C. See Electrical Characteristics Measuring Circuit Diagram) Unit: V

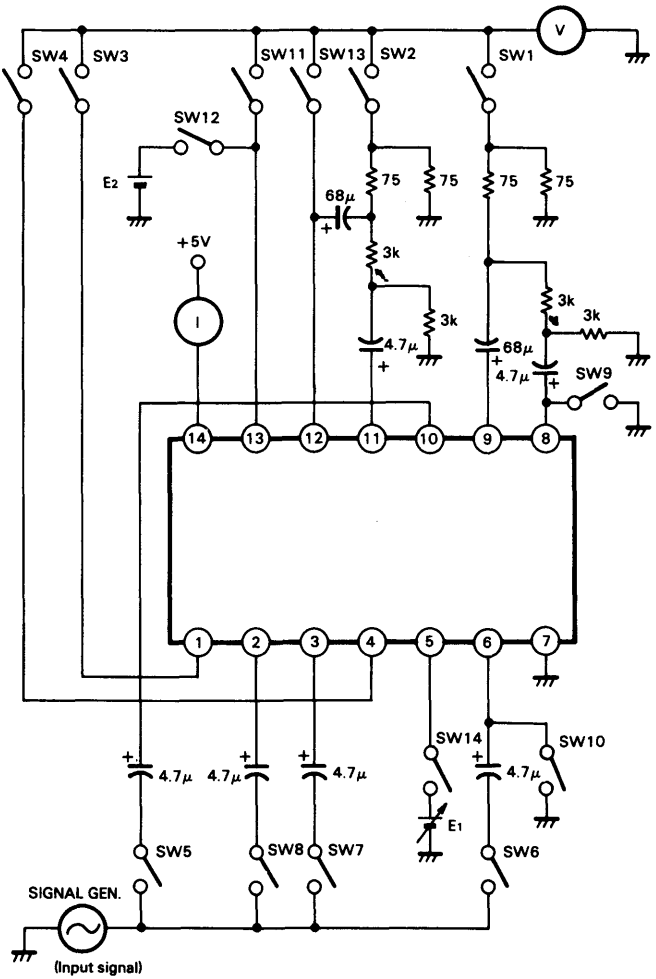
No.	Name	Voltage (V) standard value	Description
1	RECEIVE OUT	1.65	When Pin 5 is at "H", the signal input from Pin 10 is output with gain 0 dB. DC is output when Pin 5 is at "L".
2	TRANS IN	1.28	Trans amp input: As sync chip clamp may result, a low impedance input is required.
3	DRIVER IN	1.28	Drive amp input: As sync chip clamp may result, a low impedance input is required.
4	6 dB AMP OUT	2.35	The signal input from Pin 6 is output with gain 6 dB.
5	T/R	0	Mode switching terminal Trans/Receive: Receive mode at "H" (over 4V) and Trans mode at "L" (less than 1V).
6	6 dB AMP IN	2.45	6 dB amp input: Input impedance more than approx. 10 kΩ, DC 2.4V
7	GND	0	
8	SAG.C.D.O.	1.29	The Pin 9 sag is corrected by adding the sag component in the Pin 9 output. Refer to Electrical Characteristics Measuring Circuit Diagram.
9	DRIVER OUT	1.08	Driver amp output: 75 Ω line drive is output. The signal input from Pin 3 is output with gain 6 dB.
10	RECEIVE IN	1.74	Receiving amp input: As sync chip clamp may result, a low impedance input is required.
11	SAG.C.T.O.	1.30	The Pin 12 sag is corrected by adding the sag component in the Pin 12 output. Refer to Electrical Characteristics Measuring Circuit Diagram.
12	TRANS. OUT	1.10	Trans amp output: The signal input from Pin 2 when Pin 5 is at "L" is output to the 75 Ω line with a gain of 6 dB. A DC voltage determined at Pin 13 is output when Pin 5 is at "H".
13	BIAS. CONTROL	2.13	When Pin 5 is at "H", its voltage is varied to vary the Pin 12 output (DC) in turn. By linking with Pin 5, simple superimpose can be possible in the Pin 12 output. (In this case, the Pin 1 output is affected).
14	Vcc	5.0	+5.0V.

Electrical Characteristics

(Ta = 25°C, Vcc = 5.0V, See Electrical Characteristic Measuring Circuit Diagram)

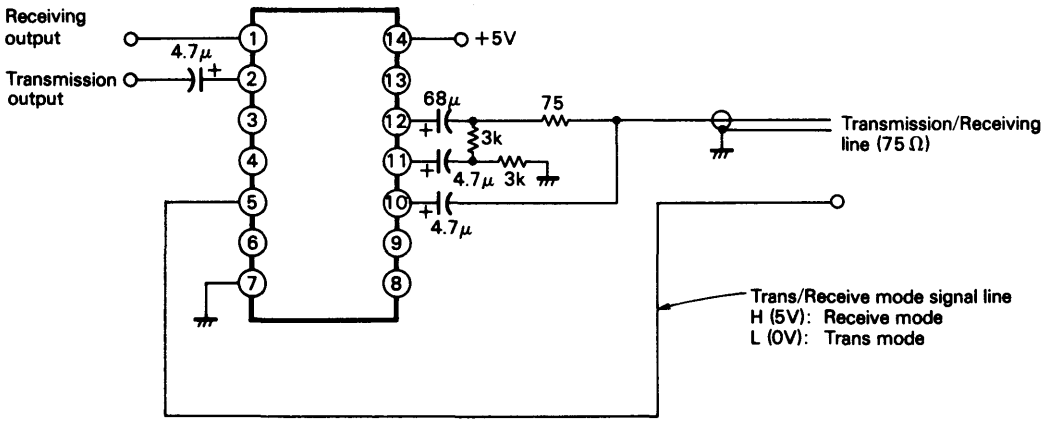
Test No.	Measuring item	Measuring point	Input condition	Measuring condition 1	2	3	4	5	6	7	8	9	10	11	12	13	14	Remark	Measuring symbol	Standard Min.	Typ.	Max.	Unit
1	Consumption current	I																	I_D	7.5	10.5	14	mA
2	Power saving	I										ON	ON						I_{DPS}	4.5	6.5	8.5	mA
3	Trans amp gain	V	500kHz, 1Vp-p		ON						ON						ON	E_1: Less than 1V (for 1Vp-p input)	G_T	−0.5	0	−0.5	dB
4	Trans dynamic range	V	16kHz, Square wave		ON						ON						ON	E_1: Less than 1V (input equivalent)	D_T	1.4			Vp-p
5-a	Trans bias control	V												ON			ON	E_1: Measured value over 4V = A	V_{13}	2.0	2.1	2.2	V
5-b	Trans bias control	V														ON	ON	E_1: Measured value over 4V = B	V_{12}	2.65	2.75	2.85	V
5-c	Trans bias control	V	E_2 = 2.3V												ON	ON	ON	$20 \log = \frac{\text{(Measuring value)} - B}{E_2 - A}$ (E_2 = 2.3V)	G_{BC}	5.3	5.8	6.3	dB
6	Receiver amp gain	V	500kHz, 1Vp-p			ON		ON									ON	E_1: Over 4V (for 1Vp-p input)	G_R	−0.5	0	−0.5	dB
7	Receiver dynamic range	V	16kHz, Square wave			ON		ON									ON	E_1: Over 4V (input equivalent)	D_R	1.7			Vp-p
8	Driver amp gain	V	500kHz, 1Vp-p	ON						ON								For input 1Vp-p	G_D	−0.5	0	−0.5	dB
9	Driver dynamic range	V	16kHz, Square wave	ON						ON								Input equivalent	D_D	1.4			Vp-p
10	6dB amp gain	V	500kHz, 1Vp-p				ON		ON									For input 1Vp-p	G_A	5.5	6.0	6.5	dB
11	6dB dynamic range	V	16kHz, 1.4Vp-p Square wave				ON		ON									1.4Vp-p	D_A	2.6	2.8	3.0	Vp-p
12	Trans receiving leakage	V	4MHz 0.7Vp-p			ON					ON						ON	E_1: Over 4V (for 0.7Vp-p) (4MHz component)	L_{TR}			−40	dB

Electrical Characteristics Test Circuit

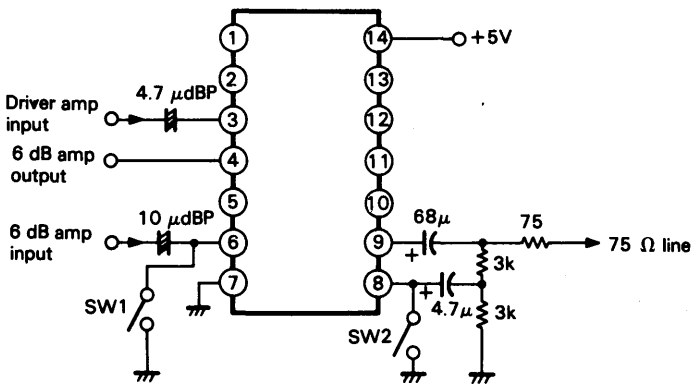


Application Circuit

Transmission and receiving reference circuit diagram (Trans amp, Receive amp)

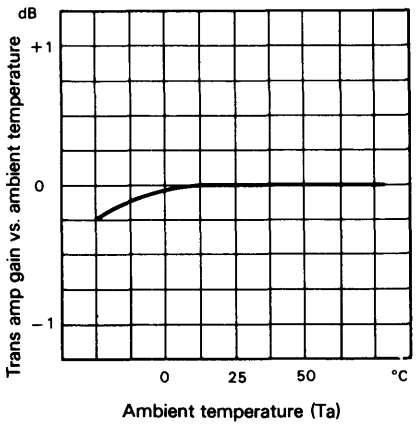


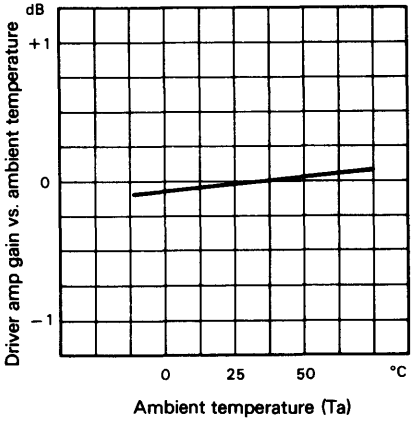
Driver amp, 6 dB amp external reference circuit diagram

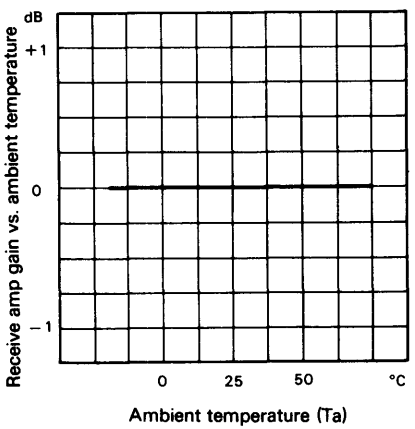


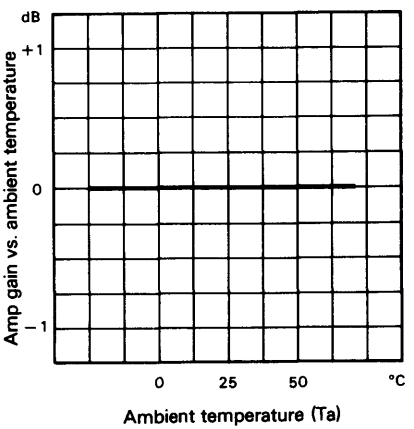
SW1: 6 dB amp power saving mode when switched on.
SW2: Driver amp power saving mode when switched on.

Temperature Characteristics









*Note) Gain at 25°C is assumed to be 0 dB.

CCD Delay Line

6) CCD Delay Line

Type	Application	Function	Page
CXL1009P	Video disk	CMOS-CCD delay line for time base corrector, 300mil shirink-DIP	673
CXL1008P/M	VCR	NTSC skew compensate	682
CXL5001P/M	General purpose	NTSC 1H CMOS-CCD delay line	694
CXL5002P/M	General purpose	NTSC 1/2H CMOS-CCD delay line	701
CXL5003P/M	General purpose	PAL 1H CMOS-CCD delay line	707
CXL5005P/M	General purpose	NTSC 1H CMOS-CCD delay line, with PLL	714

SONY

CXL1009P

CMOS-CCD Signal Processor for TBC

Description

CXL1009P is a CMOS-CCD signal processor developed for Time Base Corrector (TBC).

Features

- Low power consumption 160 mW (Typ.)
- Wide variable frequency range (15.2 to 27.2 MHz)
- Built-in peripheral circuits

Functions

- 680 bit CCD register x 2
- Clock drivers
- Autobias circuit (For Audio/Video)
- Sync tip clamp circuit
- T-type flip-flop circuit
- Timing generator circuit
- Output feedback circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}		11	V
• Supply voltage	V_{CL}		6	V
• Operating temperature	Topr	−10 to	+60	°C
• Storage temperature	Tstg	−55 to	+150	°C
• Allowable power dissipation	P_D		1	W

Recommended Operating Conditions

• Supply voltage	V_{DD}	9	V ±5%
• Supply voltage	V_{CL}	9	V ±5%

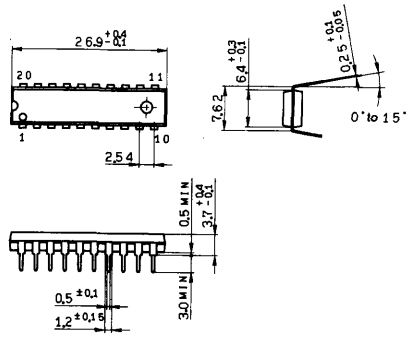
Recommended Input Signal Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_{INP-P}	–	1.0	1.28	Vp-p

Package Outline

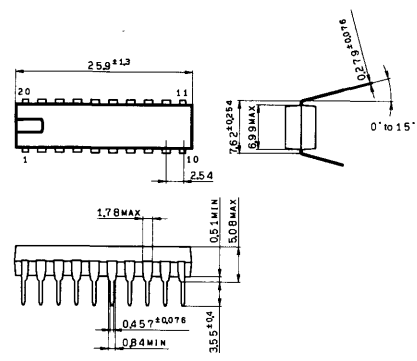
Unit: mm

20 pin DIP (Plastic)



DIP-20P-02

20 pin DIP (Plastic)



DIP-20P-121

Recommended Clock Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	f_{CK}	15.2	21.4	27.2	MHz	Pulse or Sinewave*
Clock amplitude	V_{CKP-P}	1.0	2.0	4.0	Vp-p	
Duty (during pulse)	Dy	40	50	60	%	

***Note)** During pulse the clock requires a pulse as shown in Fig. 1.

E88Z37-YA

Recommended Clock Waveform (Pulse)

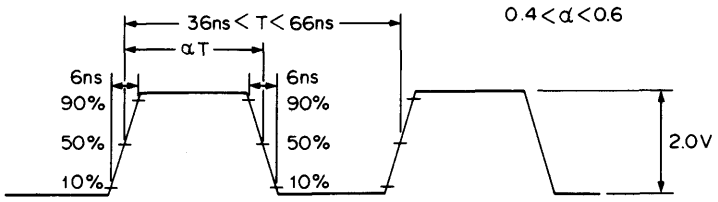
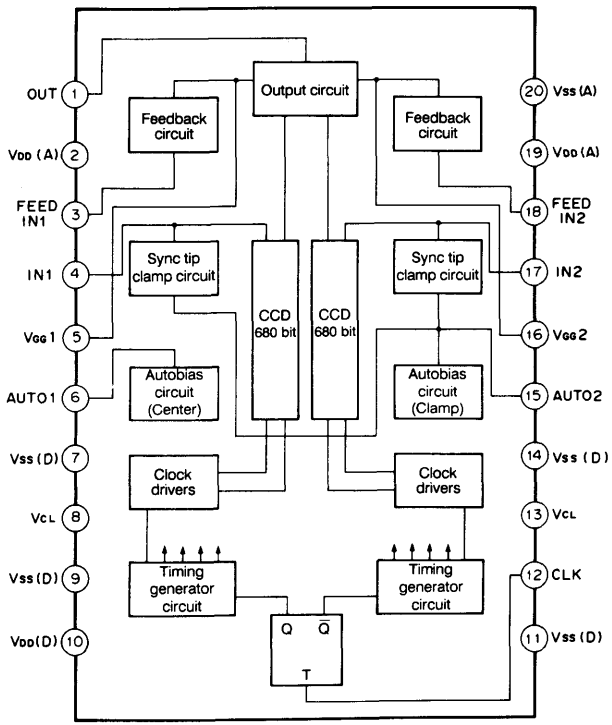


Fig. 1

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	OUT	O	Output
2	V_{DD} (A)		Power supply 1 (Analog)
3	FEED IN1	I	Feedback input 1
4	IN1	I	Input 1
5	V_{GG} 1	I	Gate1
6	AUTO1	O	Autobias 1
7	Vss (D)		GND (Digital)
8	V_{CL}		Power supply 2 (Digital)
9	Vss (D)		GND (Digital)
10	V_{DD} (D)		Power supply 1 (Digital)
11	Vss (D)		GND (Digital)
12	CLK	I	Clock input
13	V_{CL}		Power supply 2 (Digital)
14	Vss (D)		GND (Digital)
15	AUTO2	O	Autobias 2
16	V_{GG} 2	I	Gate 2
17	IN2	I	Input 2
18	FEED IN2	I	Feedback input 2
19	V_{DD} (A)		Power supply 1 (Analog)
20	Vss (A)		GND (Analog)

Electrical Characteristics 1

Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, See the Electrical Characteristics Test Circuit.

Item	Symbol	Test conditions	SW condition				Test point	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4					
Pin voltage	$V_{AUTO1-DC}$	Pin 6 voltage	b	a	a	a	V6	4.0	5.5	7.0	V
	$V_{AUTO2-DC}$	Pin 15 voltage	b	a	a	a	V5	3.5	5.0	6.5	V
	V_{IN-DC}	Pins 4 and 17 voltage	b	b	a	a	V7	3.5	5.0	6.5	V
	V_{GG-DC}	Pins 5 and 16 voltage	a	a	a	a	V8	1.0	2.0	3.0	V
			b								
			c								

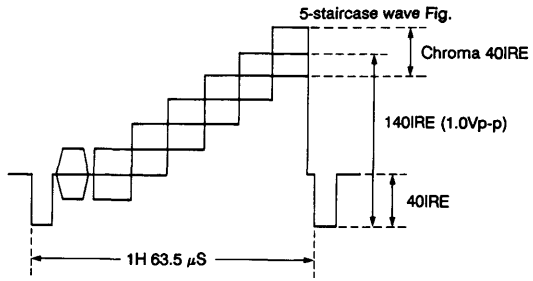
Electrical Characteristics 2

Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, See the Electrical Characteristics Test Circuit.
Test conditions: Set the voltage of pins E1 and E2 as follows:
E1 = $V_{GG\text{-}DC}$, E2 = $V_{AUTO2\text{-}DC}$ + 0.65V or $V_{AUTO1\text{-}DC}$

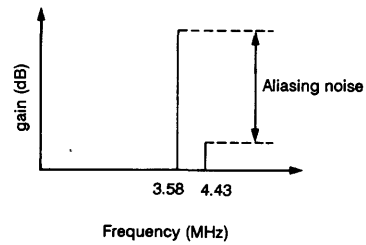
Item	Symbol	Test conditions	SW condition				Test point	Min.	Typ.	Max.	Unit
			SW1	SW2	SW3	SW4					
Supply current	I_{DD}	250 kHz, 1.0Vp-p sine wave input	b	a	a	a	A1	–	7	12	mA
	I_{CL}						A2	–	20	28	mA
Insertion gain	IG	250 kHz, 1.0Vp-p sine wave input $IG = 20\log\left[\frac{\text{Output voltage (Vp-p)}}{1Vp\text{-}p}\right]$	a to c	a	a	b	V2	–3	0	3	dB
Frequency response	f_G	Dissipation at 3.58 MHz vs. 250 kHz $f_G = 20\log(V_{3.58MHz}/V_{250kMz})$ $V_{3.58MHz}$: Output signal voltage during 3.58 MHz input V_{250kMz}: Output signal voltage during 250 kHz input	a to c	a	b	b	V2	–3	–1	0	dB
Differential gain	DG	5-staircase wave (See Fig.) input Y = 140IRE (= 1.0Vp-p) Measuring with vectorscope.*1	a to c	a	c	b	S	–	3	5	%
Differential phase	DP							–	3	5	Deg
Noise	S/N1	S: Input = 250 kHz, 1.0Vp-p sine wave	b	a	a	c	V3	50	55	–	dB
		N: Input = Alternating grounding point (rms)	b	a	d	c					
Aliasing noise	S/N2	Input = 3.58 MHz, 1.0Vp-p sine wave *2	d	a	b	d	SA	35	50	–	dB
Insertion gain difference	ΔIG	250 kHz, 1.0Vp-p sine wave *3	a to c	a	a	b	V2	–	1	2.4	%
DC output voltage difference	$\Delta V_{O\text{-}DC}$	250 kHz, 1.0Vp-p sine wave *4	a to c	a	a	a	V1	–	–	0.3	V

Note)

*1. Differential gain and differential phase conditions.



*2. Aliasing noise
Measure with a spectrum analyzer the 4.43 MHz output signal voltage at 3.58 MHz input (clock frequency 16.02 MHz).



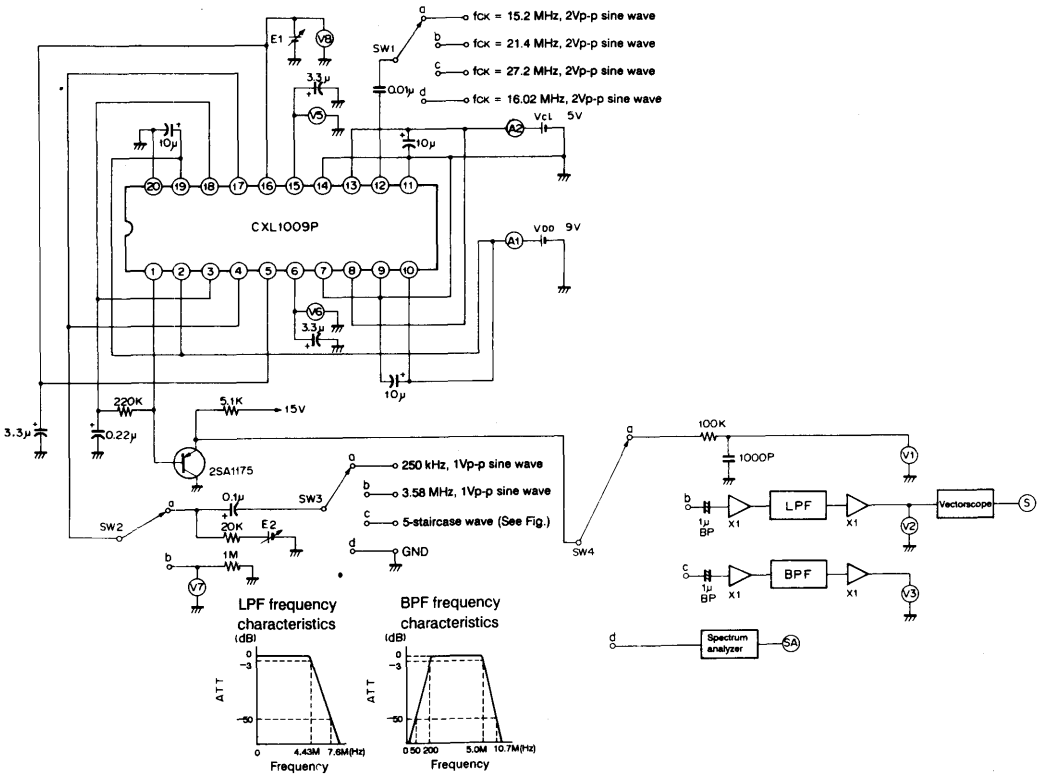
*3. Insertion gain difference
With the insertion gain of clock frequencies of 15.2 MHz, 21.4 MHz and 27.2 MHz, determine maximum value as IGmax [dB] and minimum value as IGmin [dB]. Insertion gain difference ΔIG is defined as follows.

$$\Delta IG = \frac{10^{(IGmax/20)} - 10^{(IGmin/20)}}{10^{(IGmax/20)} + 10^{(IGmin/20)}} \times 200\ [\%]$$

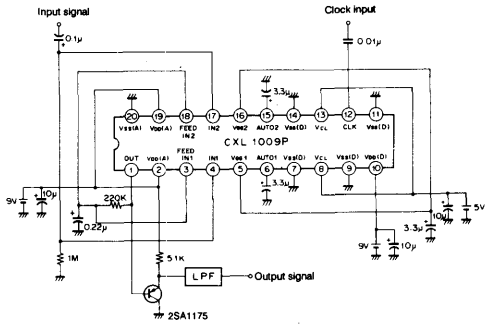
*4. DC output voltage difference
With the DC output voltage of clock frequencies of 15.2 MHz, 21.4MHz and 27.2 MHz, determine maximum value as $V_{O\text{-}DC\,max}$ and minimum value as $V_{O\text{-}DC\,min}$. DC output voltage difference $\Delta V_{O\text{-}DC}$ is defined as follows.

$$\Delta V_{O\text{-}DC} = V_{O\text{-}DC\,max} - V_{O\text{-}DC\,min}\ [V]$$

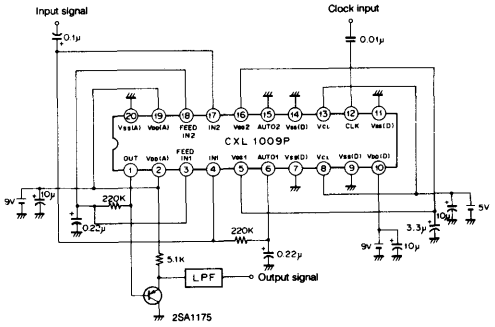
Electrical Characteristics Test Circuit



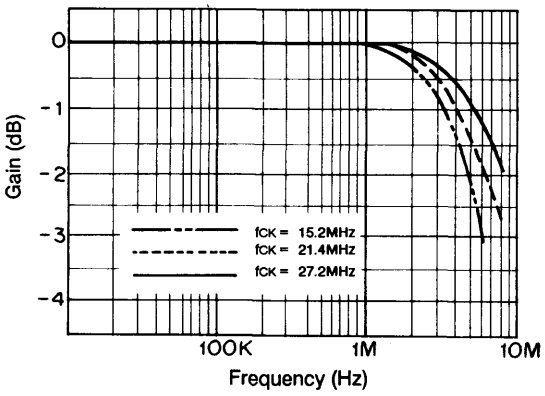
Application Circuit (Video)



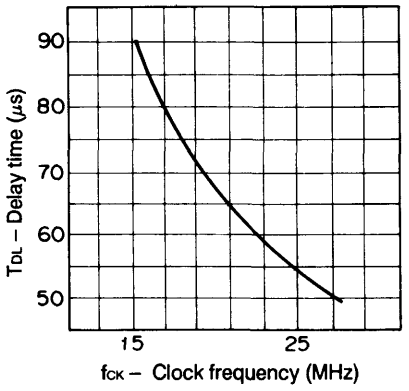
Application Circuit (Audio)



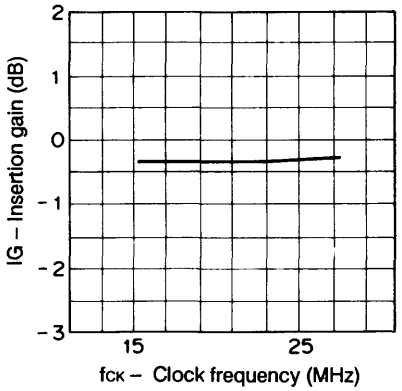
Frequency characteristics



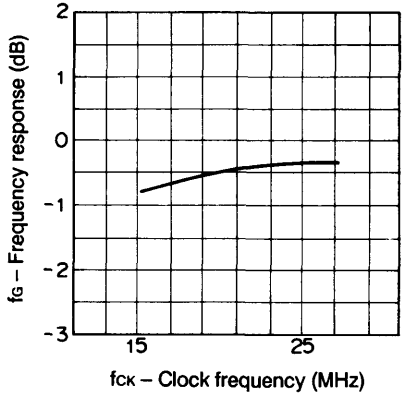
Delay time vs. Clock frequency



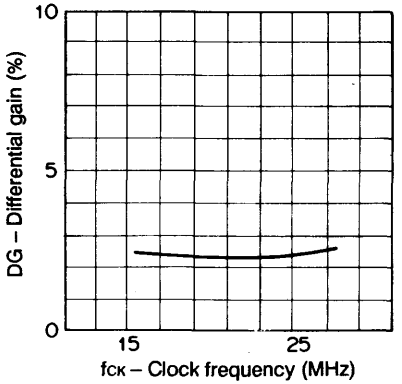
Insertion gain vs. Clock frequency



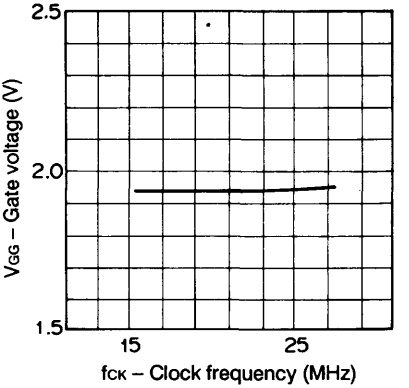
Frequency response vs. Clock frequency



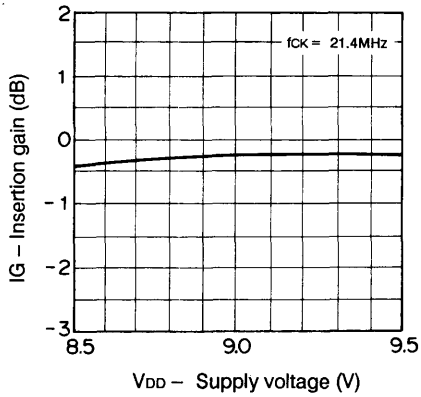
Differential gain vs. Clock frequency



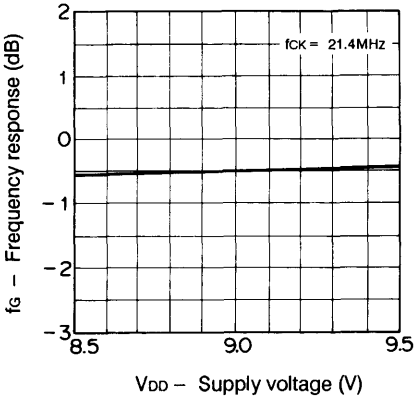
Gate voltage vs. Clock frequency



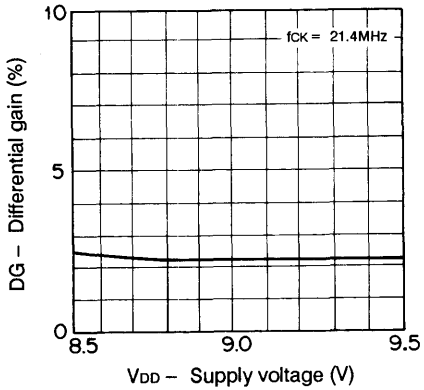
Insertion gain vs. Supply voltage



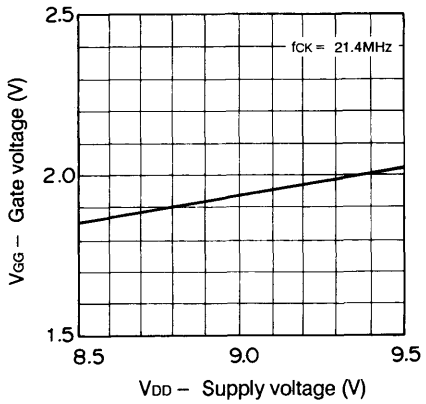
Frequency response vs. Supply voltage



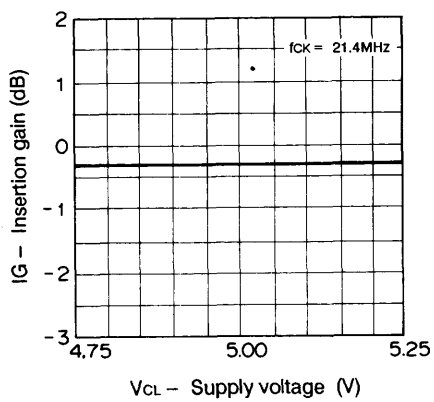
Differential gain vs. Supply voltage



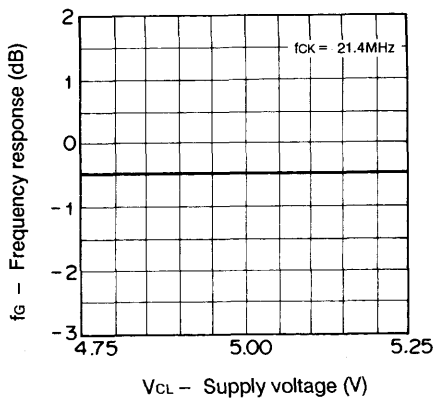
Gate voltage vs. Supply voltage



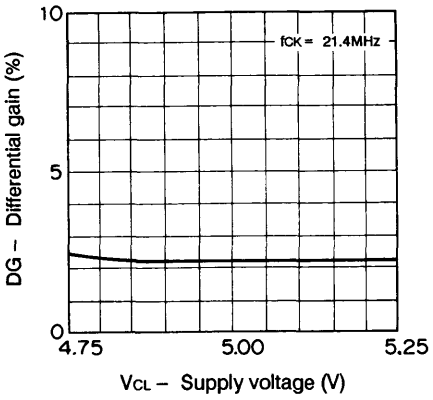
Insertion gain vs. Supply voltage



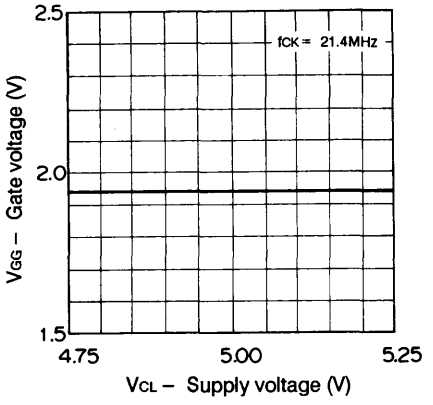
Frequency response vs. Supply voltage



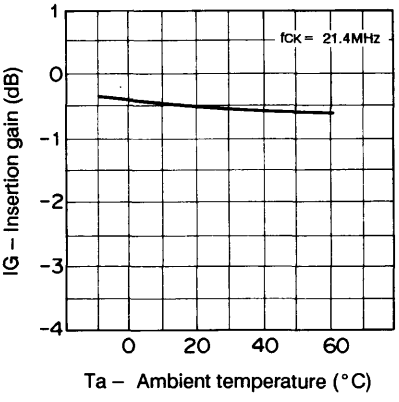
Differential gain vs. Supply voltage



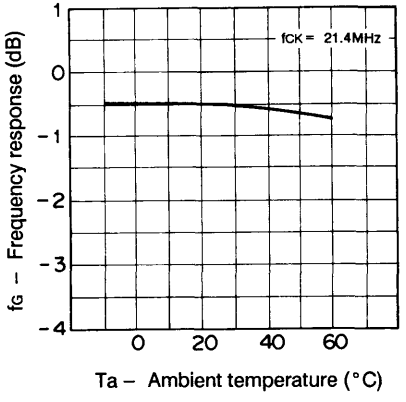
Gate voltage vs. Supply voltage



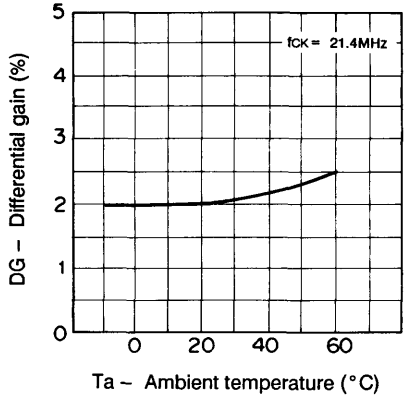
Insert gain vs. Ambient temperature



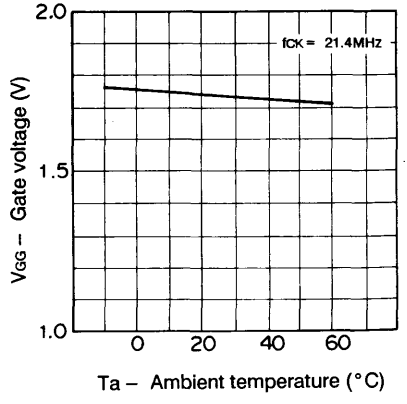
Frequency response vs. Ambient temperature



Differential gain vs. Ambient temperature



Gate voltage vs. Ambient temperature



SONY

CXL1008P/M

CMOS-CCD Signal Processor for Skew Compensation

Description

CXL1008P/M are CMOS-CCD signal processors developed for the varying-speed video signal for home-use 8 mm VTRs.

Features

- Low power consumption 105 mW (Typ.)
- Built-in peripheral circuit
- Adjustment is necessary for one part.

Functions

- 1/2H 359-bit, direct 20-bit CCD register
- Clock driver
- Timing oscillation circuit
- Automatic bias circuit
- Sink chip clamp circuit
- Dummy VD insert circuit
- Sample hold circuit

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	11	V
	V_{CL}	6	V
• Operating temperature	T_{opr}	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	CXL1008P 1000	mW
		CXL1008M 500	mW

Recommended Operating Conditions

• Supply voltage	V_{DD}	9V±5	%
	V_{CL}	5V±5	%

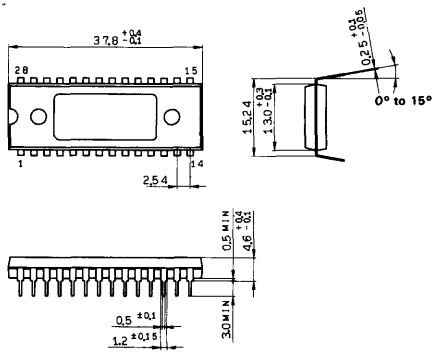
Recommended Clock Conditions

• Clock input amplitude	V_{CLK}	0.15 to 1.0 (0.3 Typ.)	Vp-p
• Clock frequency	f_{CLK}	10.738635	MHz

Package Outline

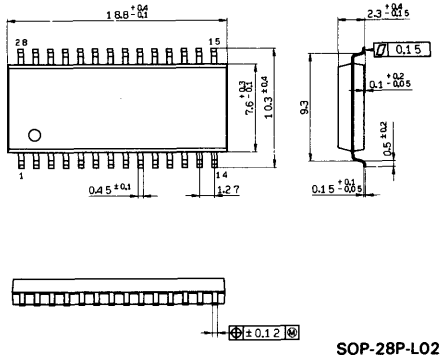
Unit: mm

CXL1008P 28 pin DIP (Plastic)



DIP-28P-03

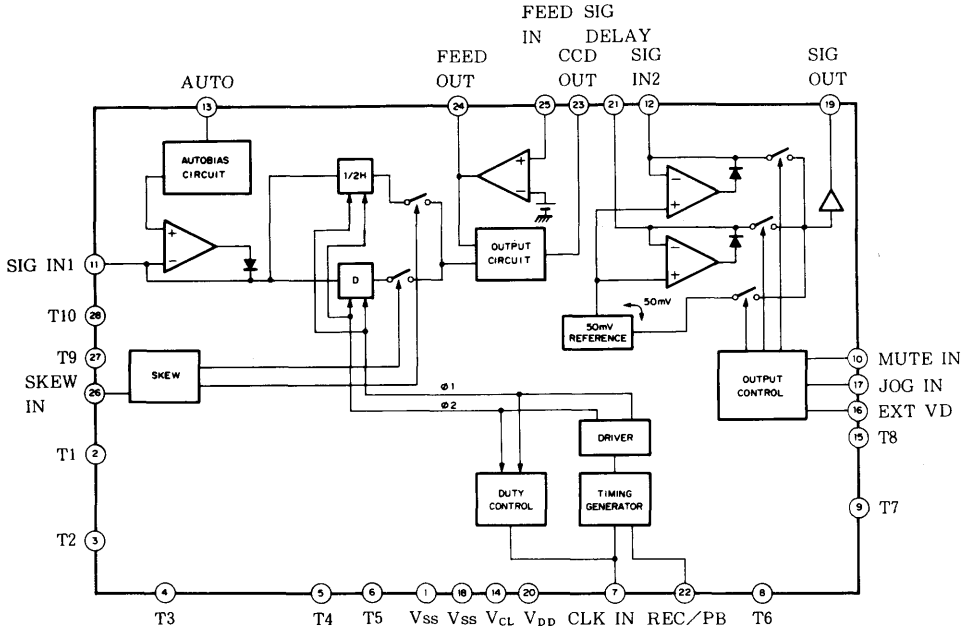
CXL1008M 28 pin SOP (Plastic)



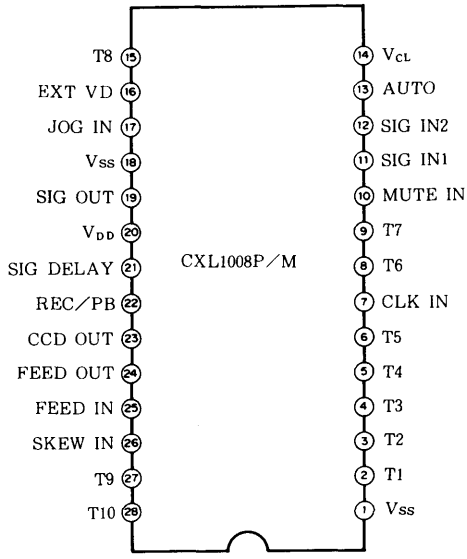
SOP-28P-L02

* 60924 – ST

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Condition	Description	Impedance (Ω)
1	Vss			GND	
7	CLK IN	I	0.3Vp-p	Input the sinewave of 3 fsc (10.738635 MHz)	>50k
10	MUTE IN	I	5V when muting, normally 0V	The video signal mute is generated at High level. See the Logic Table of Signal Output Selection State (Table 1).	>100k
11	SIG IN1	I	1.1 Vp-p or less	Signal input pin of CCD DL Enter composite video signal.	>100k
12	SIG IN2	I	2.2 Vp-p or less	Signal input pin of the through side Enter composite video signal.	>100k
13	AUTO	O		The DC level of automatic bias is output.	10k
14	V_{CL}		+5V	Power supply 1	
16	EXT VD	I	When VD is inserted, 5V	Use this pin when VD is inserted to the video signal in the external dummy VD signal input.	>100k
17	JOG IN	I	JOG mode 5V PB/REC mode 0V	JOG/NORMAL PB selection pin See the Logic Table of Signal Output Selection State (Table 1).	>100k
18	Vss			GND	
19	SIG OUT	O		Final output	0.6 to 1.5k
20	V_{DD}		+9V	Power supply 2	
21	SIG DELAY	I		After the output from pin 23 CCD OUT passes through LPF, input it to the same pin and insert clamp and VD.	>100k
22	REC/PB	I	5V when PB 0V when REC	Operate the clock at High when PB. Stop the clock at Low when REC.	>100k
23	CCD OUT	O		Direct output from CCD DL	0.6 to 1.5k
24	FEED OUT	O		Feedback DC output	10k
25	FEED IN	I		Smoothing capacitor connection pin of the bias commutation loop on the output circuit	>100k
26	SKEW IN	I		Select Direct DL and 1/2H DL signals when High and Low, respectively. See the CCD/DL mode selection logic table (Table 2).	>100k

Note) T1 through T10 test pins must be connected as shown in the example of the application circuit because of the IC internal circuit.

Precautions

Countermeasures for electrostatics are necessary because some pins have low electrostatic strength (particularly Pin 26: SKEW IN).

Electrical Characteristics

(See the Electrical Characteristics Test Circuit)

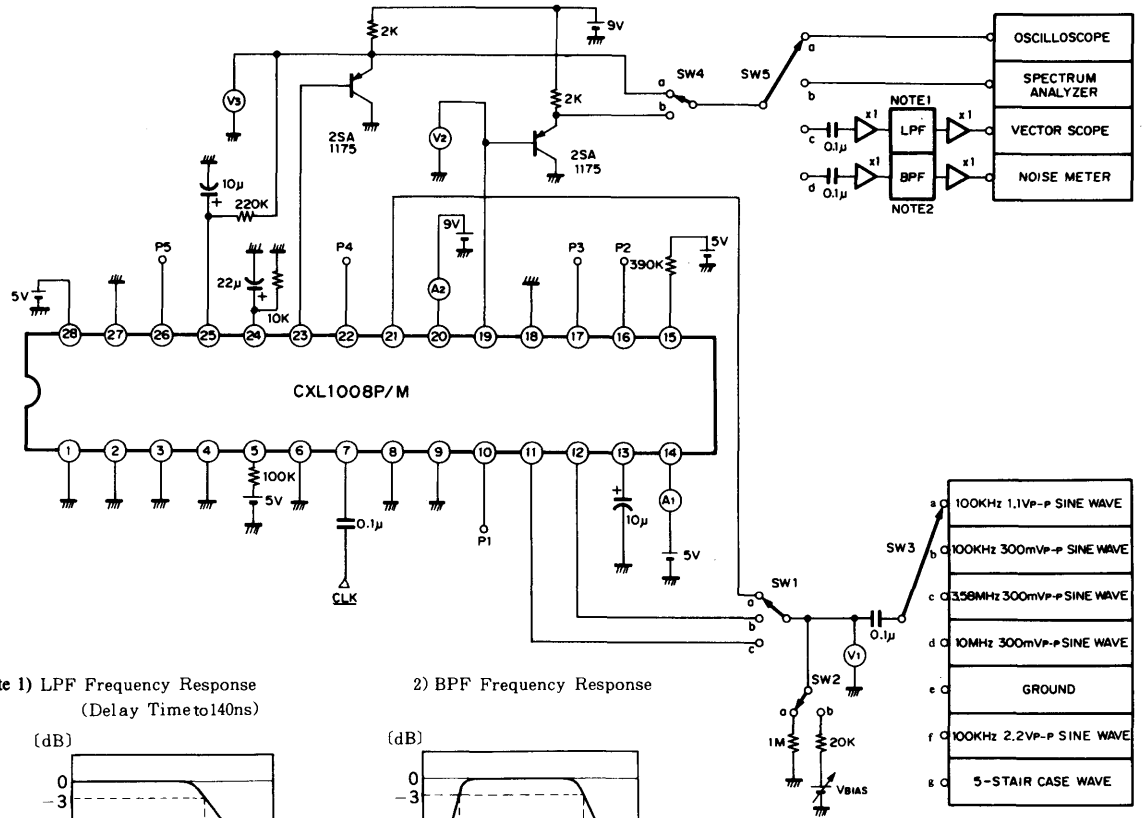
Ta = 25℃, V_{DD} = 9.0V, V_{CL} = 5.0V, f_{CLK} = 10.7MHz, V_{CLK} = 0.3Vp-p Sinewave

Items	Symbol	Test Conditions	Switch Conditions					Control Pin Conditions *1, *2					Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	P1	P2	P3	P4	P5					
Power current	I_{DD}	PB. JOG	c	a	a						H			7	12	mA	1
	I_{CL}		c	a	a						H			8	10	mA	1
Clock input level	CLK										H		0.15	0.3	1.0	V	
Signal input pin voltage	Vdi1		c	a	e						H		4.0	5.0	6.0	V	2
	Vdi2		b	a	e								4.0	4.2	4.4	V	2
	Vdi3		a	a	e								4.0	4.2	4.4	V	2
Signal output pin voltage	Vdo1		c	a	e						H		1.7	2.0	2.4	V	3
	Vdo2		b	a	e			L	L	L			1.5	2.0	2.5	V	3
CCD signal output voltage difference	Δ Dab	Direct↔1/2H	c	a	e	a	a				H	H↔L	−55	0	55	mV	4
Signal insert gain	IG_{CCD}		c	b	a	a	a				H		− 3.0	0	3.0	dB	5
	IG_{In2}		b	b	f	b	a	L	L	L			− 1.2	− 0.8	0	dB	5
	IG_{DL}		a	b	f	b	a	L	L	H			− 1.2	− 0.8	0	dB	5
CCD output signal gain difference	Δ Gab	Direct↔1/2H	c	b	a	a	a				H	H↔L	− 1.3	0	1.3	%	6
Frequency characteristics	f_{CCD}	3.58MHz/100kHz	c	b	b↔c	a	b				H		−3	−2	0	dB	7
	f_{In2}	10MHz/100kHz	b	b	b↔d	b	b	L	L	L			− 0.5	0	—	dB	8
	f_{DL}	10MHz/100kHz	a	b	b↔d	b	b	L	L	H			− 0.5	0	—	dB	8
Frequency characteristics difference	Δ fab	Direct↔1/2H at 3.58MHz	c	b	b↔c	a	b				H	H↔L	− 0.2	0	0.2	dB	9
Differential gain	DG_{CCD}	1.1 Vp-p input	c	b	g	a	c				H		0	3	10	%	10
	DG_{In2}	2.2 Vp-p input	b	b	g	b	c	L	L	L			0	2	4	%	10
	DG_{DL}	2.2 Vp-p input	a	b	g	b	c	L	L	H			0	2	4	%	10

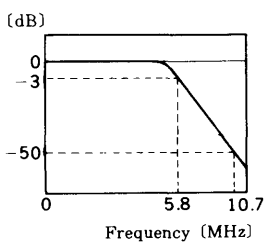
Test Items	Symbol	Test Conditions	Switch Conditions					Control Pin Conditions *1, *2					Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	P1	P2	P3	P4	P5					
Differential phase	DP_{CCD}	1.1 Vp-p input	c	b	g	a	c				H		0	3	5	deg	10
	DP_{In2}	2.2 Vp-p input	b	b	g	b	c	L	L	L			0	3	5	deg	10
	DP_{DL}	2.2 Vp-p input	a	b	g	b	c	L	L	H			0	3	5	deg	10
Allowable input amplitude	V_{IN1-AC}		c		g								—	—	1.1	Vp-p	
	V_{IN2-AC}		a/b		g								—	—	2.2	Vp-p	
SN rate	S/N_{CCD}		c	b	a↔e	a	d				H		50	55	—	dB	11
	S/N_{In2}		b	b	f↔e	b	d	L	L	L			50	65	—	dB	11
	S/N_{DL}		a	b	f↔e	b	d	L	L	H			50	65	—	dB	11
VD insert depth	V_{VD}	2 Vp-p video signal from sink chip	a	a	g	b	a	L	⊓	H			0	50	100	mV	12
Logical input	$V_{IN\ H}$												4.0		—	V	
	$V_{IN\ L}$												—		1.0	V	

Note) •1. Control pins correspond to P1 through P5 of the Electrical Characteristics Test Circuit.
•2. Symbols "H" and "L" in control pin conditions represent "$V_{IN\ H}$" and "$V_{IN\ L}$" of logical input.

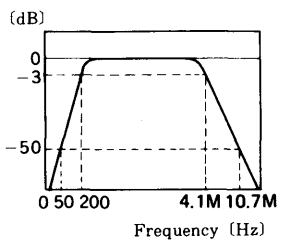
Electrical Characteristics Test Circuit



Note 1) LPF Frequency Response
(Delay Time to 140ns)



2) BPF Frequency Response

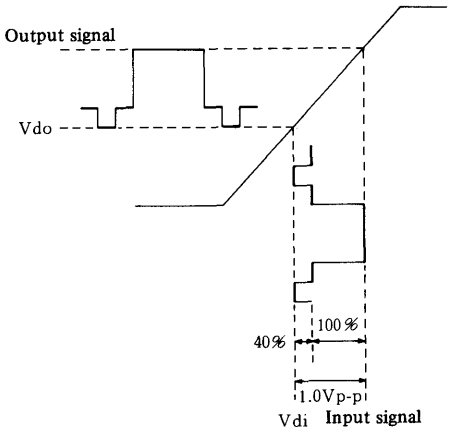


Note)

1. Current value when the clock is in operation in the PB or JOG mode.
   In the REC mode, the clock is stopped (Pin 22 is at low) to save power.

2. With the signal input pin voltage value, the video signal sync tip is clamped.

3. Vdo1 is a CCD OUT output voltage when the SIG IN1 input voltage is Vdi1
   Vdo2 is a SIG OUT output voltage when the SIG IN2 input voltage is Vdi2.
   Vdo1 and Vdo2 represent outputs for the sync tip clamp level when a white level signal is input as shown in the diagram.



4. ΔDab denotes an output voltage difference of CCD OUT when the direct DL and 1/2H DL are switched.

5. IG_{CCD} is a gain when a 1.1 Vp-p 100 kHz sinewave is input to SIG IN1.

$$IG_{CCD} = 20 \log \frac{\text{Output amplitude (Vp-p)}}{1.1 \text{ Vp-p}}$$

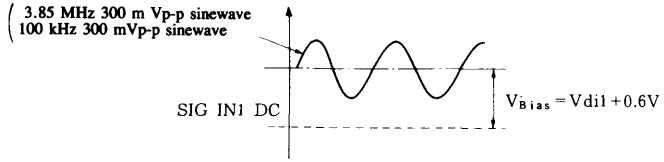
It is measured by giving a Vdi1 + 0.6 bias with V_{Bias}.
IGin2 and IG_{PL} are SIG OUT gains when 2.2 Vp-p 100 kHz sinewave is input to each of SIG IN2 and SIG DELAY pins.

$$IG_{in2} = 20 \log \frac{\text{Output amplitude (Vp-p)}}{2.2 \text{ Vp-p}}$$

It is measured by giving a Vdi2 + 1.1V bias with V_{Bias}.

6. ΔGab is a gain difference between the direct DL and 1/2H DL.

7. It represents a loss at 3.58 MHz compared with 100 kHz.
It is measured by raising the SIG IN1 input pin by 0.6V higher than the sync tip clamp level (Vdi1) with V_{Bias}.

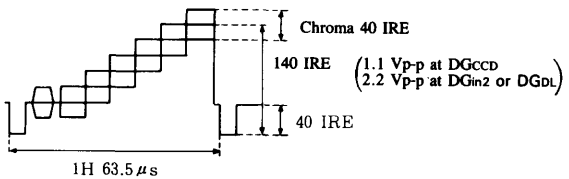


$$F_{CCD} = 20 \log \frac{V3.58\ MHz\ output}{V100\ kHz\ output}$$

8. It represents a loss at 10 MHz compared with 100 kHz.
It is measured by raising the SIG IN2 or SIG DELAY pin by 1.1V higher than the sync tip clamp level (Vdi2 or Vdi3) with V_{Bias}.

9. ΔFab is a frequency response difference between the direct DL and 1/2H DL.

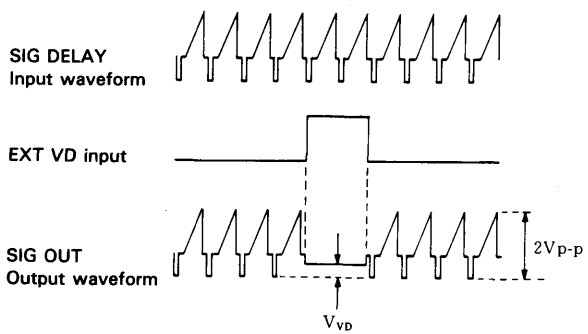
10.



DG is measured with a vectorscope in each mode of the 5-stage waves.

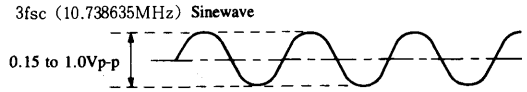
11. Measure S/N of the BPF 100 kHz to 4.2 MHz in the subcarrier trap mode with a video noise meter.

12.



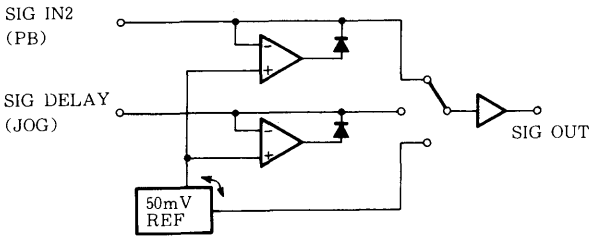
Set a voltage value at V_{VD} when inserting EXT VD to the 2 Vp-p signal output waveform sync tip of SIG OUT.

CLOCK



Function Outline

Output signal selection



The video output signal is selected by selecting the output switch for three signals: Pin 10 (MUTE IN), Pin 17 (JOG IN) and Pin 16 (EXT VD).

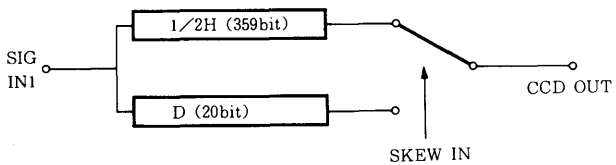
Logic Table of Signal Output Selection State

Input control signal state			Video signal output selection state			
JOG IN	MUTE IN	EXT VD	PB	JOG	VD insert	MUTE
0	0	0	○	×	×	×
0	0	1	○	×	×	×
0	1	0	×	×	×	○
0	1	1	×	×	×	○
1	0	0	×	○	×	×
1	0	1	×	×	○	×
1	1	0	×	×	×	○
1	1	1	×	×	○	○

Table 1

Note) 1. Figures "0" and "1" of the input control signal state are equivalent to "Low" and "High" of logic.
2. Items marked with the symbol "○" in the video signal output selection state are selected.
3. PB = $\overline{\text{JOG IN}} \cdot \overline{\text{MUTE IN}}$
JOG = JOG IN . $\overline{\text{MUTE IN}} \cdot \overline{\text{EXT VD}}$
VD insert = JOG IN . EXT VD
MUTE = MUTE IN

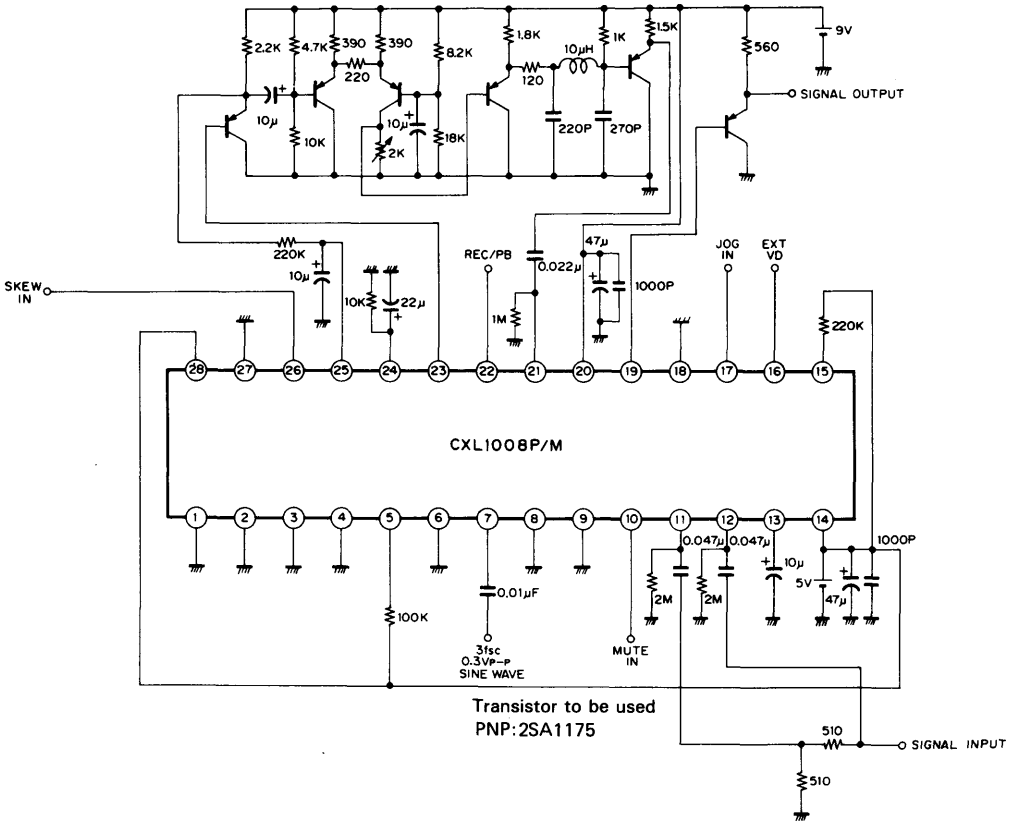
CCD selection



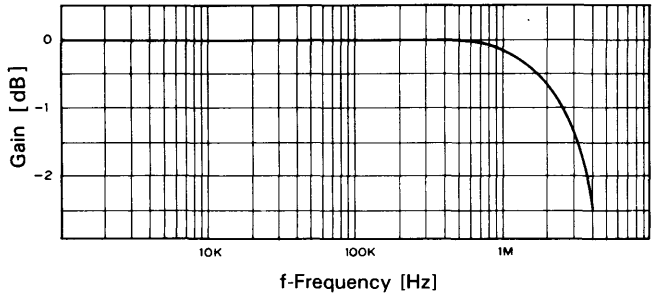
Logic Table of Signal Output Selection State

Control signal	CCD DL mode	
SKEW IN	D	1/2H
0	×	○
1	○	×

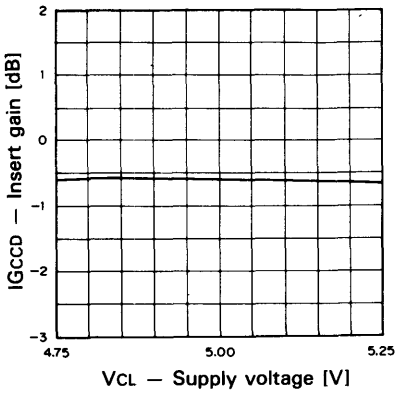
Table 2



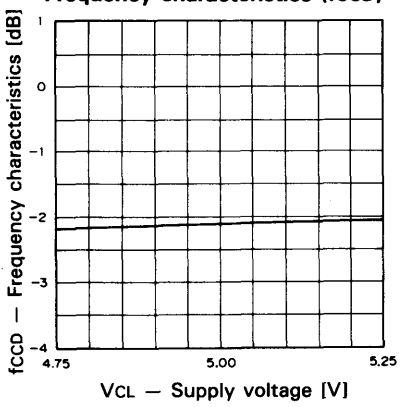
Frequency characteristics (Ta = 25°C)



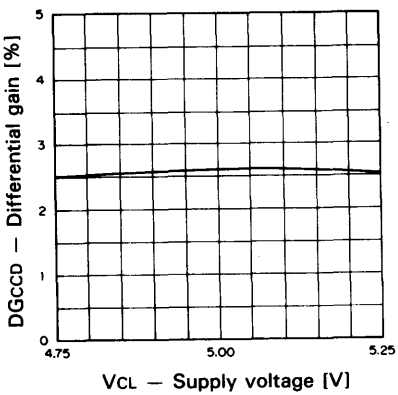
Supply voltage (VCL) vs. Insert gain (IGCCD)



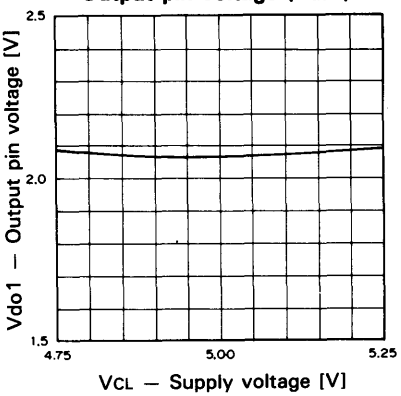
Supply voltage (VCL) vs. Frequency characteristics (fCCD)



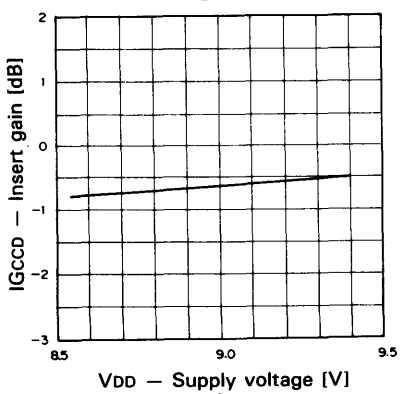
Supply voltage (VCL) vs. Differential gain (DGCCD)



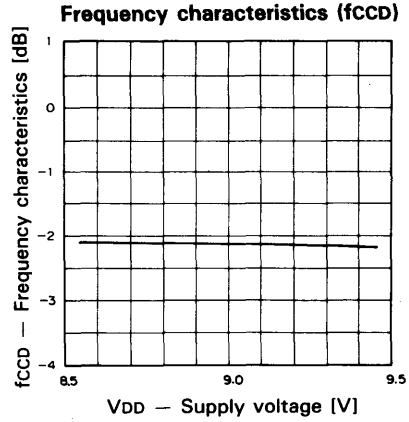
Supply voltage (VCL) vs. Output pin voltage (Vdo1)



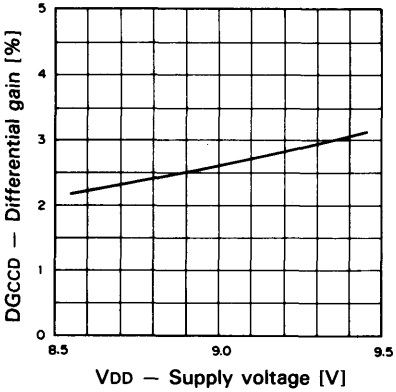
Supply voltage (VDD) vs. Insert gain (IGCCD)



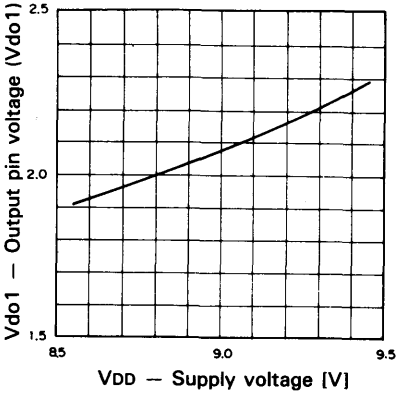
Supply voltage (VDD) vs. Frequency characteristics (fCCD)



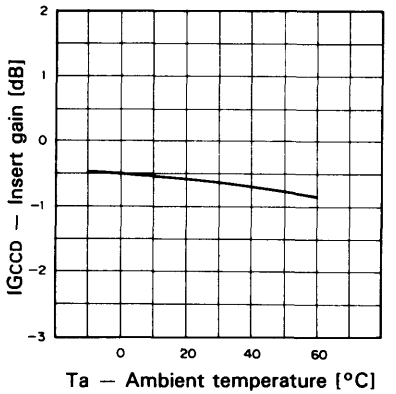
Supply voltage (V_{DD}) vs. Differential gain (DG_{CCD})



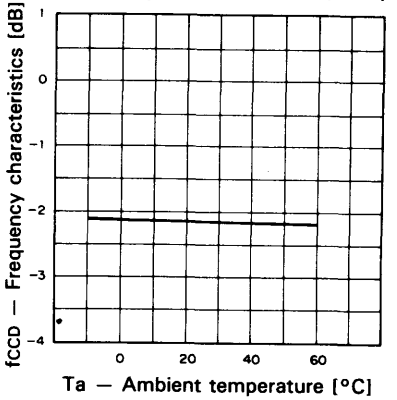
Supply voltage (V_{DD}) vs. Output pin voltage (Vdo1)



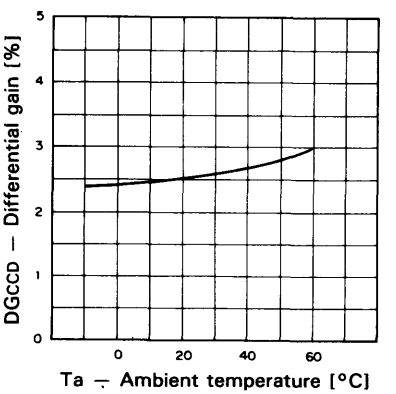
Ambient temperature (Ta) vs. Insert gain (IG_{CCD})



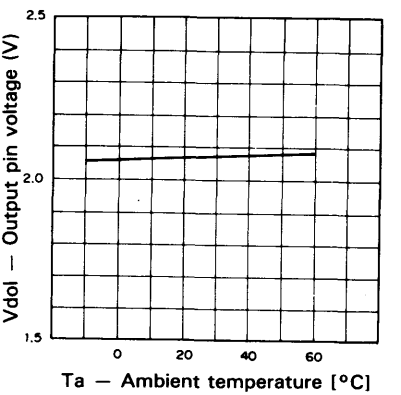
Ambient temperature (Ta) vs. Frequency characteristics (f_{CCD})



Ambient temperature (Ta) vs. Differential gain (DG_{CCD})



Ambient temperature (Ta) vs. Output pin voltage (f_{CCD})(Vdo1)



SONY® CXL5001P/CXL5001M

CMOS-CCD 1H Delay Line for NTSC

Description

The CXL5001P/CXL5001M are general purpose CCD delay line ICs which provide 1H delay time of NTSC.

Features

- Low power dissipation 80 mW (typical)
- Small size package (8-pin DIP, MFP)
- Low differential gain DG=3% (typical)
- Input signal amplitude 180IRE (=1.28Vp-p, max.)
- Low input clock amplitude operation 150 mVp-p (min.)
- On chip peripheral circuits.

Functions

- 680 bit CCD register
- Clock drivers
- Autobias circuit
- Synchronized tip clamp circuit
- Sample and hold circuit

Absolute Maximum Ratings (Ta=25°C)

• Power supply voltage 1	V_{DD}	11	V
• Power supply voltage 2	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	CXL5001P 480	mW
		CXL5001M 350	mW

Recommended Operating Conditions

V_{DD}	9V±5%
V_{CL}	5V±5%

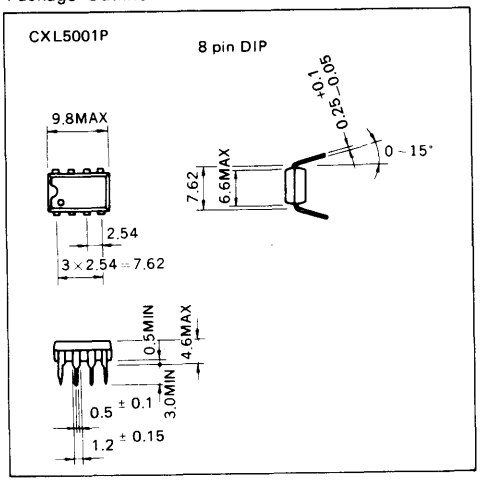
Recommended Clock Conditions

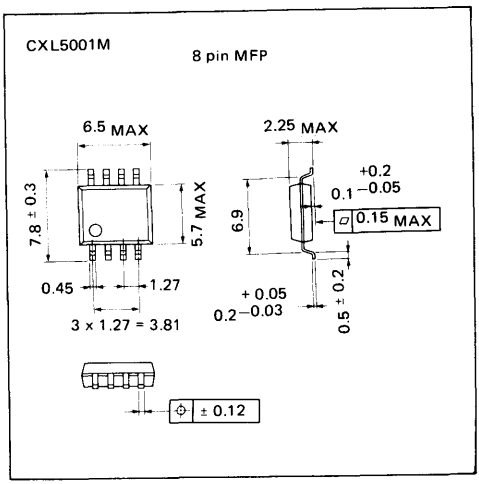
• Input clock amplitude	V_{CK}	150 mVp-p to 1.0 Vp-p (Typical 250 mVp-p)
• Clock frequency	f_{CK}	10.7 MHz

Structure

CMOS-CCD

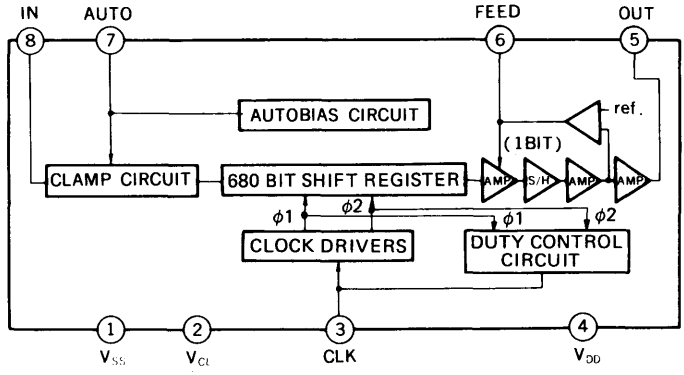
Package Outline Unit: mm





50656-ST

Block Diagram



Pin Description

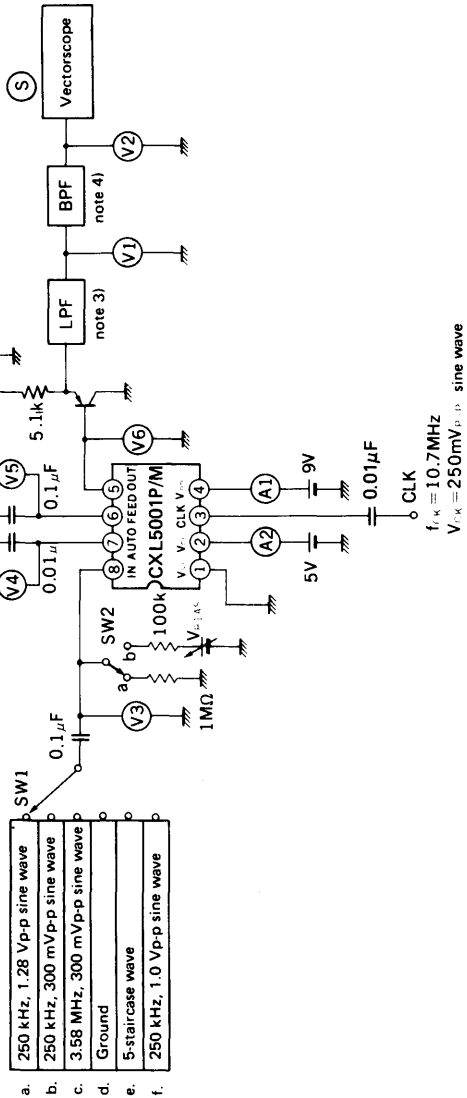
Pin No.	Symbol	Description	Impedance [Ω]	Pin No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		5	OUT	Signal output	600 to 1k
2	V_{CL}	5V power supply		6	FEED	Feedback DC output	>100k
3	CLK	Clock input	>100k	7	AUTO	Autobias DC output	10k
4	V_{DD}	9V power supply		8	IN	Signal input	>100k

Electrical Characteristics

(Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{CK}=10.7 MHz. V_{CK}=250 mVp-p sine wave, See "Electrical characteristics measuring circuit")

Item	Symbol	Measuring condition	SW condition		Measuring point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	9	11	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20log ($V_{3.58\ MHz}$/ $V_{250\ kHz}$) (Note 1)	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope (Note 2)	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	V_{IN-AC}	INPUT=250 kHz, 1.28 Vp-p.	d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$		a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

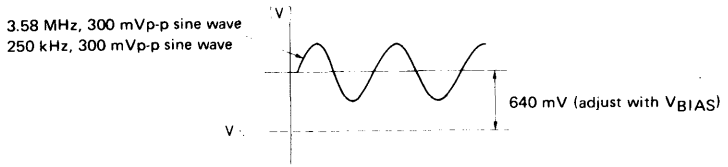
Electrical Characteristics Measuring Circuit



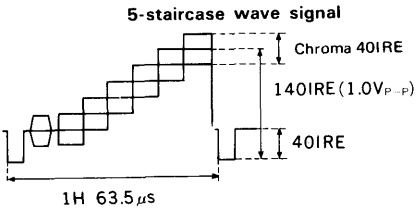
Note 1) Frequency characteristics measuring condition

$V_{3.58\ MHz}$ (Output signal voltage [Vp-p] at 3.58 MHz input)
$V_{250\ kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 8 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.

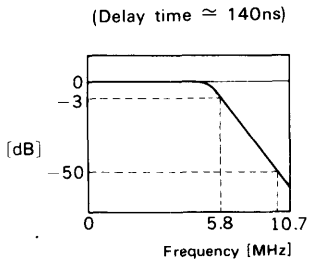


Note 2) Differential gain and differential phase measuring condition

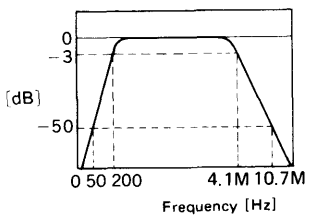


DG and DP are measured at output S point by vectorscope.

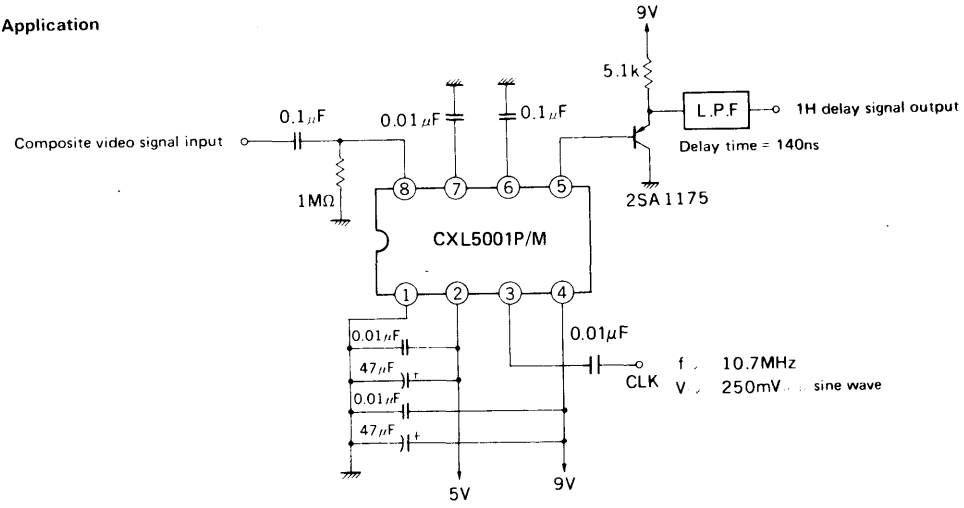
Note 3) LPF frequency characteristics



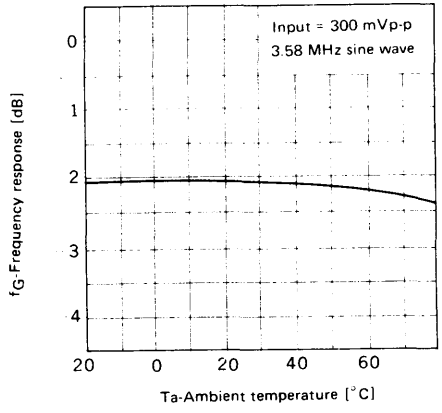
Note 4) BPF frequency characteristics



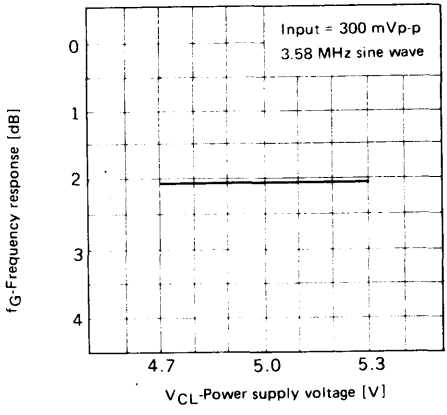
Application



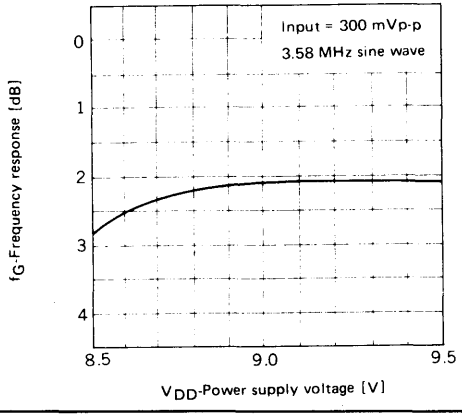
Frequency response vs. Ambient temperature



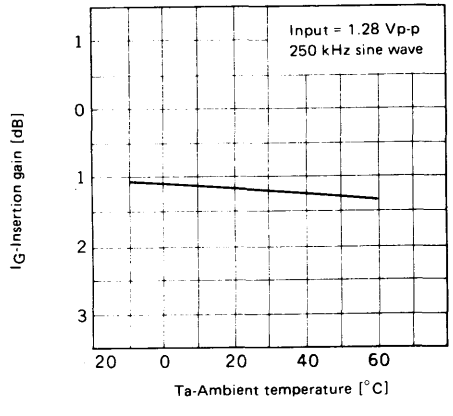
Frequency response vs. Power supply voltage



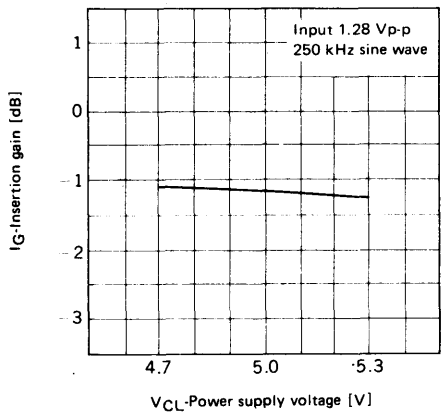
Frequency response vs. Power supply voltage



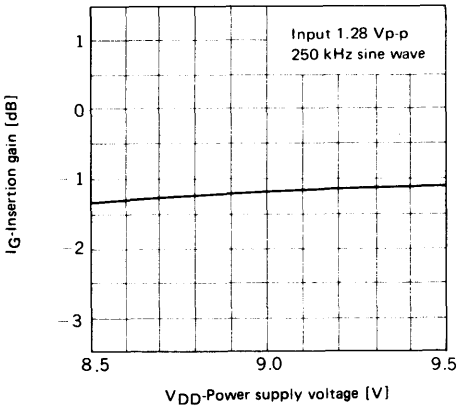
Insertion gain vs. Ambient temperature



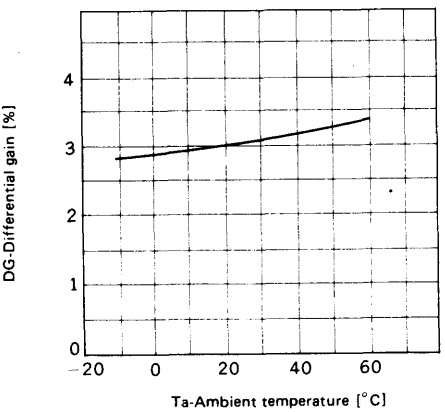
Insertion gain vs. Power supply voltage



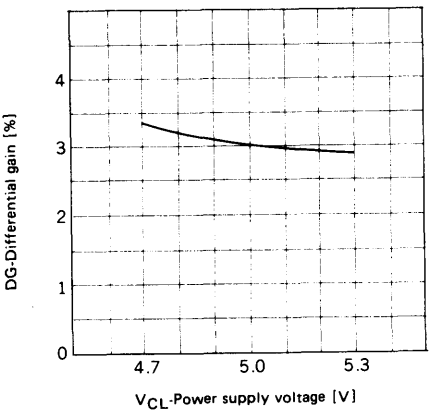
Insertion gain vs. Power supply voltage



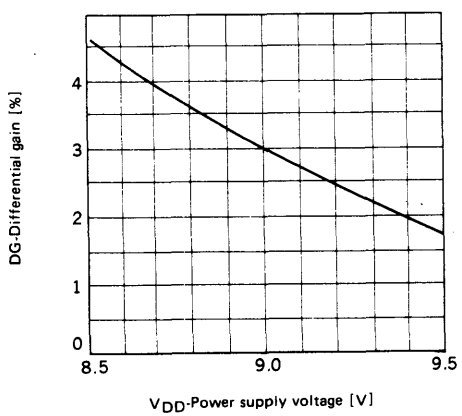
Differential gain vs. Ambient temperature



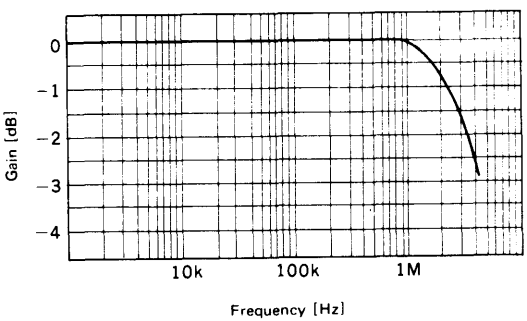
Differential gain vs. Power supply voltage



Differential gain vs. Power supply voltage



Frequency response



SONY

CXL5002P/M

CMOS-CCD 1/2H Delay Line for NTSC

Description

CXL5002P/CXL5002M are general purpose CCD delay line ICs which provide 1/2H delay time of NTSC.

Features

- Low power dissipation 70mW (Typ.)
- Small size package (8 pin DIP, SOP)
- Low differential gain DG = 3% (Typ.)
- Input signal amplitude 180IRE (= 1.28Vp-p, Max.)
- Low input clock amplitude operation 150mVp-p (Min.)
- On chip peripheral circuits.

Structure

CMOS-CCD

Functions

- 340 bit CCD register
- Clock drivers
- Autobias circuit
- Synchronous Signal tip clamp circuit
- Sample and hold circuit

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage 1	V_{DD}	11	V
• Supply voltage 2	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
P_D CXL5002P		480	mW
CXL5002M		350	mW

Recommended Operating Conditions

V_{DD}	9V ± 5%
V_{CL}	5V ± 5%

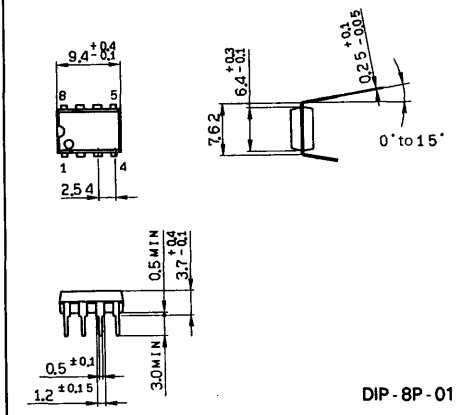
Recommended Clock Conditions

- Input clock amplitude V_{CK} 150mVp-p to 1.0Vp-p (250mVp-p Typ.)
- Clock frequency f_{CK} 10.7 MHz

Package Outline

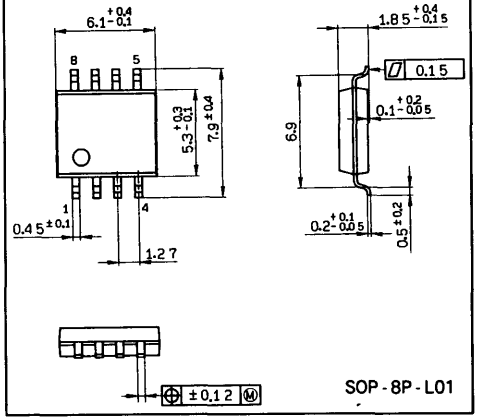
Unit : mm

CXL5002P 8 pin DIP



DIP-8P-01

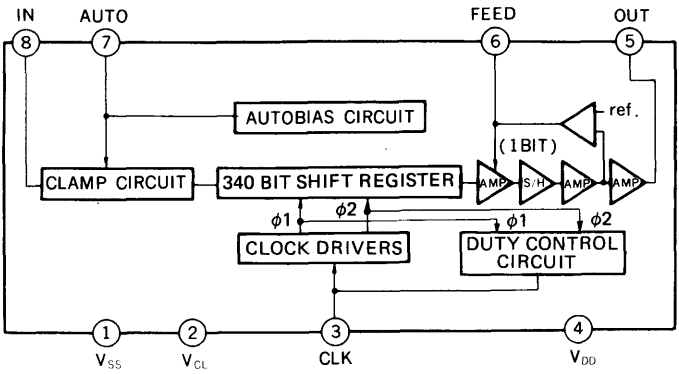
CXL5002M 8 pin SOP



SOP-8P-L01

50657A – ST

Block Diagram



Pin Description

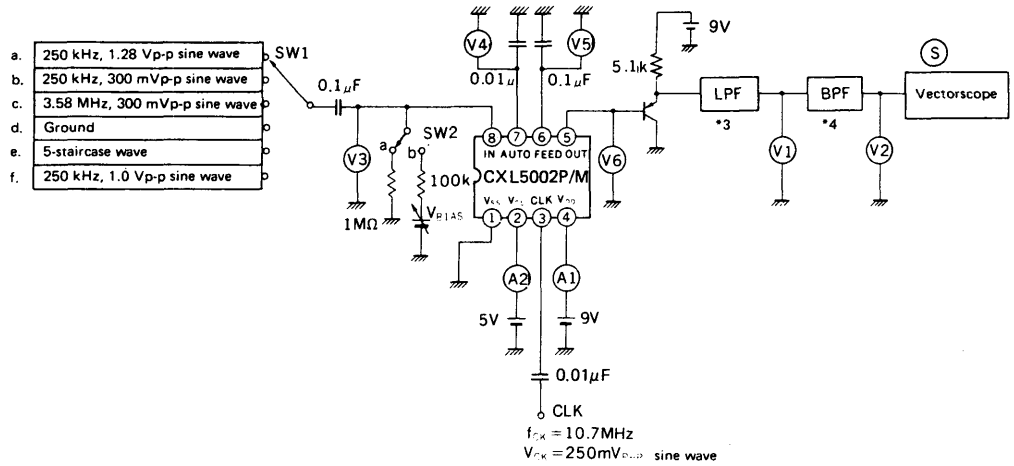
No.	Symbol	Description	Impedance [Ω]	No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		5	OUT	Signal output	600 to 1k
2	V_{CL}	5V power supply		6	FEED	Feedback DC output	>100k
3	CLK	Clock input	>100k	7	AUTO	Autobias DC output	10k
4	V_{DD}	9V power supply		8	IN	Signal input	>100k

(Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{CK}=10.7 MHz. V_{CK}=250 mVp-p sine wave,

Electrical Characteristics See ,, See "Electrical characteristics test circuit")

Item	Symbol	Measuring condition	SW condition		Measuring point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	7	9	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20log ($V_{3.58\ MHz}$/ $V_{250\ kHz}$) *1	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope *2	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	V_{IN-AC}		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$	INPUT=250 kHz, 1.28 Vp-p.	a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

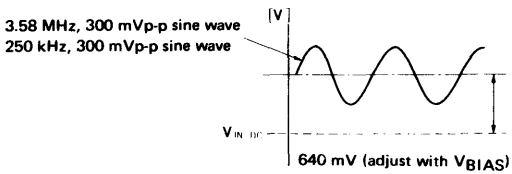
Electrial Characteristics Test Circuit



Note *1. Frequency characteristics measuring condition

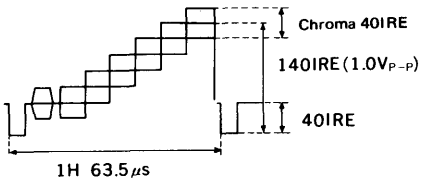
$V_{3.58\ MHz}$ (Output signal voltage [Vp-p] at 3.58 MHz input)
$V_{250\ kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 8 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.



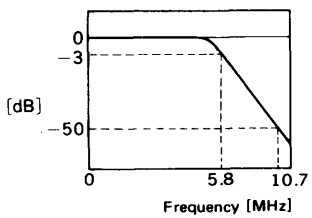
***2. Differential gain and differential measuring phase measuring condition**

5-staircase wave signal

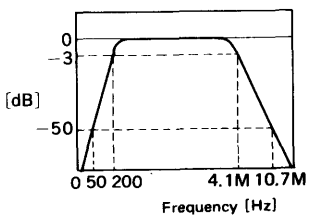


DG and DP are measured at output S point by vectorscope.

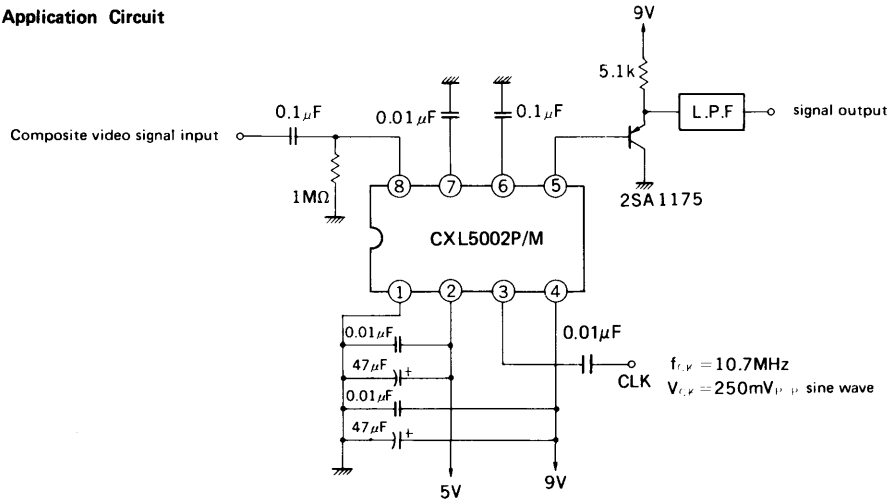
***3. LPF frequency characteristics**



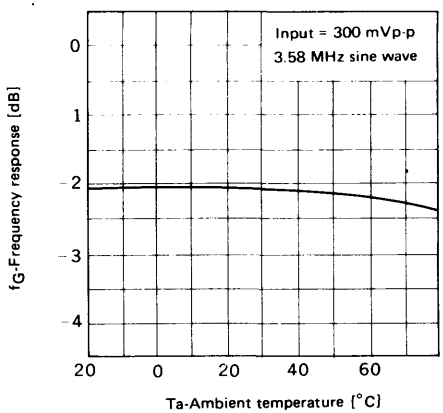
***4. BPF frequency characteristics**



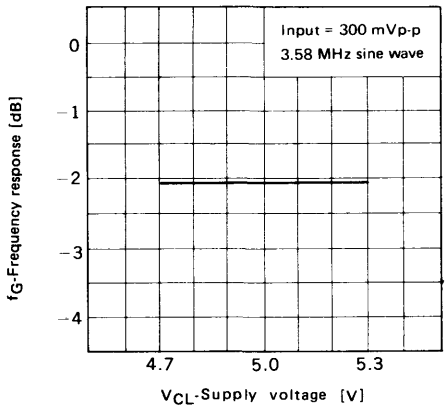
Application Circuit



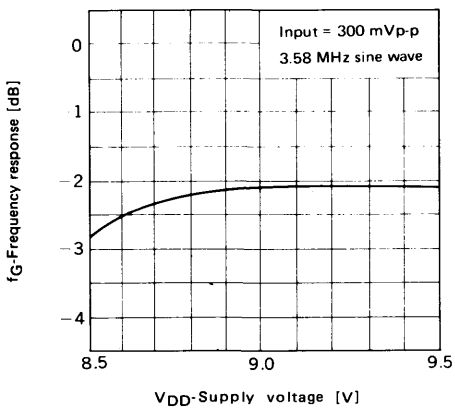
Frequency response vs. Ambient temperature



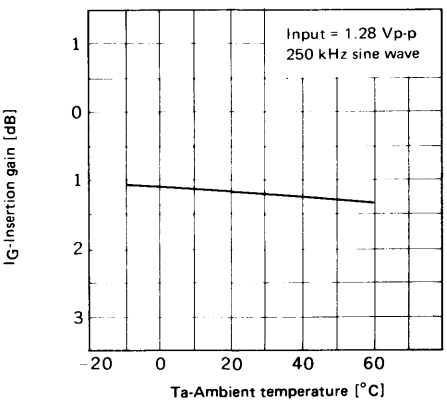
Frequency response vs. Supply voltage



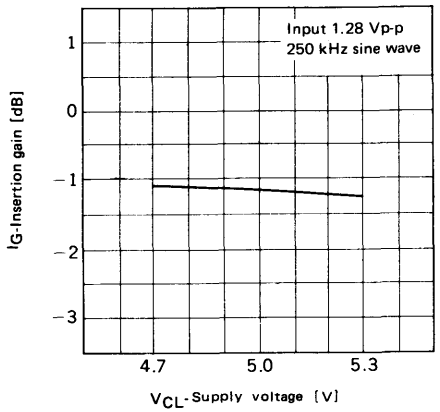
Frequency response vs. Supply voltage



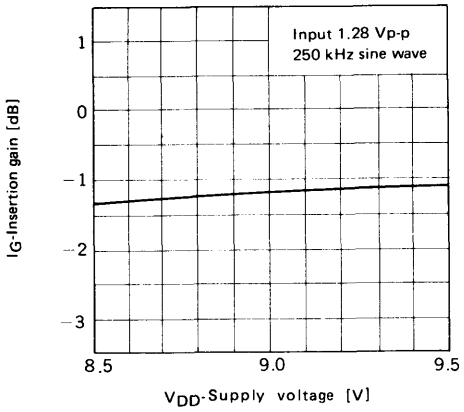
Insertion gain vs. Ambient temperature



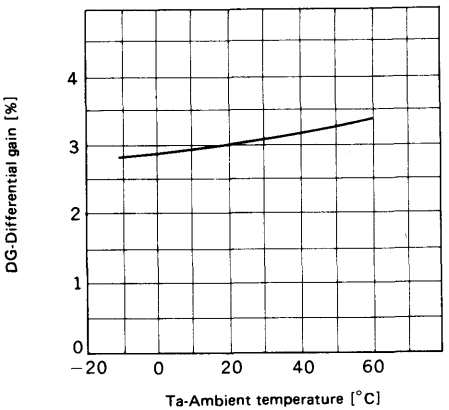
Insertion gain vs. Supply voltage



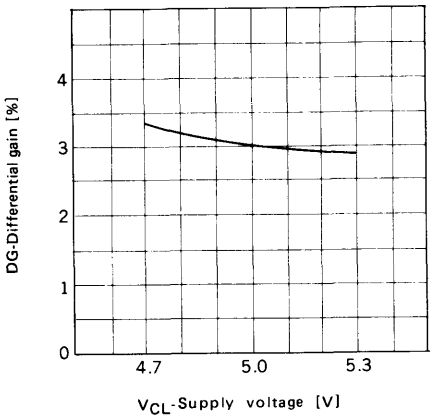
Insertion gain vs. Supply voltage



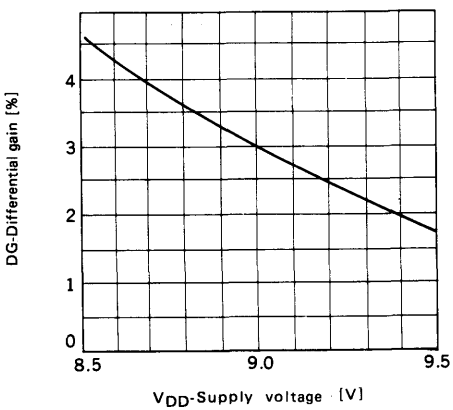
Differential gain vs. Ambient temperature



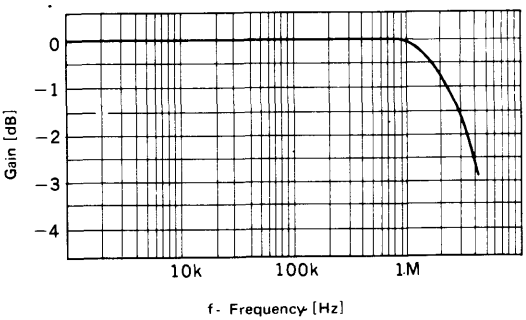
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage



Frequency response



SONY

CXL5003P/M

CMOS-CCD 1H Delay Line for PAL

Description

CXL5003P/CXL5003M are general purpose CCD delay line ICs which provide 1H delay time of PAL.

Features

- Low power dissipation 110 mW (Typ.)
- Small size package (8-pin DIP, SOP)
- Low differential gain DG=3% (Typ.)
- Input signal amplitude 180IRE (=1.28 Vp-p, Max.)
- Low input clock amplitude operation 150 mVp-p (Min.)
- On chip peripheral circuits

Structure

CMOS-CCD

Functions

- 848 bit CCD register
- Clock drivers
- Autobias circuit
- Synchronized tip clamp circuit
- Sample and hold circuit

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	11	V
• Supply voltage	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D CXL5003P	480	mW
	CXL5003M	350	mW

Recommended Operating Conditions

• Supply voltage	V_{DD}	9V±5%
	V_{CL}	5V±5%

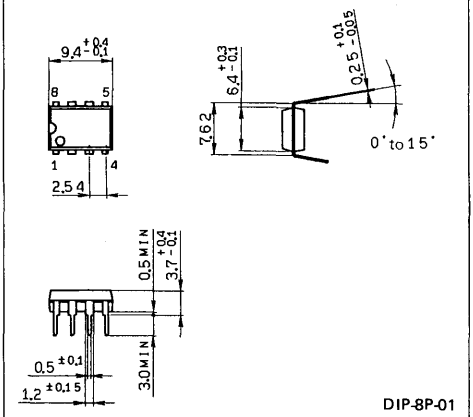
Recommended Clock Conditions

• Input clock amplitude	V_{CK}	150 mVp-p to 1.0 Vp-p (250 mVp-p Typ.)
• Clock frequency	f_{CK}	13.3 MHz

Package Outline

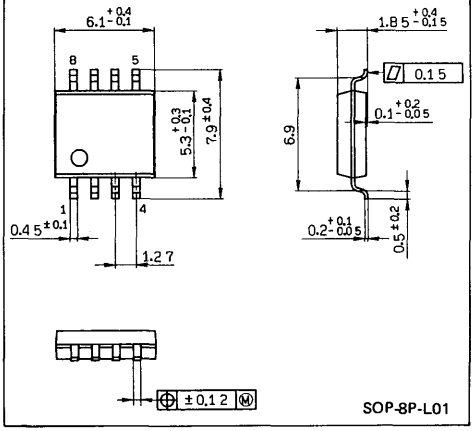
Unit: mm

CXL5003P 8 Pin DIP (Plastic)



DIP-8P-01

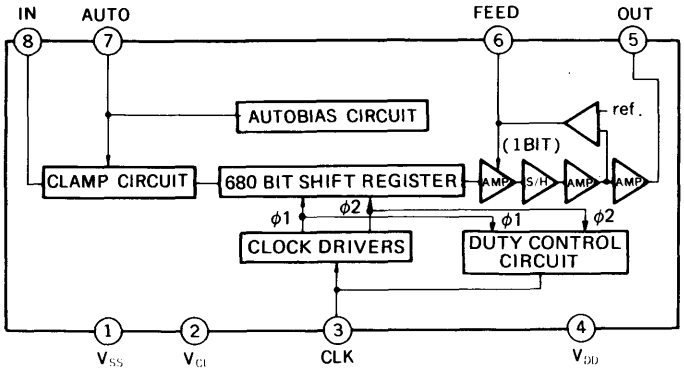
CXL5003M 8 Pin SOP (Plastic)



SOP-8P-L01

51221A-ST

Block Diagram



Pin Description

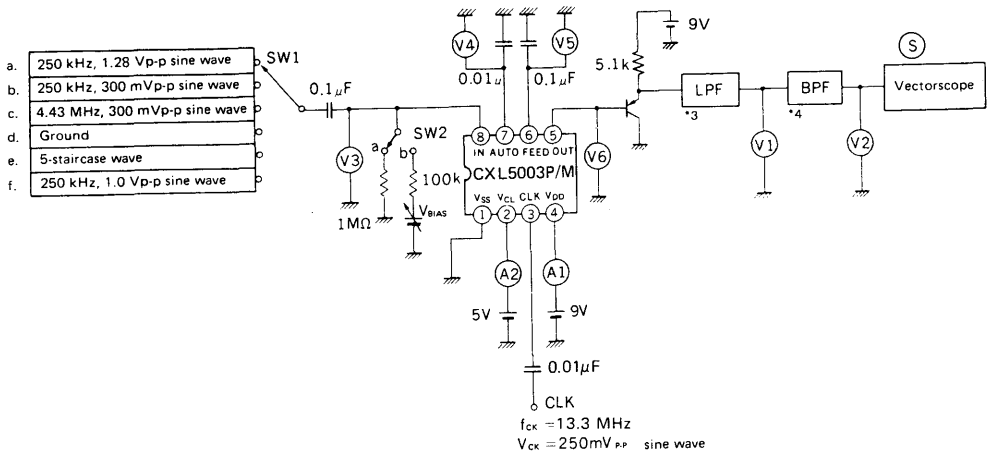
No.	Symbol	Description	Impedance [Ω]	No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		5	OUT	Signal output	600 to 1k
2	V_{CL}	5V power supply		6	FEED	Feedback DC output	>100k
3	CLK	Clock input	>100k	7	AUTO	Autobias DC output	10k
4	V_{DD}	9V power supply		8	IN	Signal input	>100k

Electrical Characteristics

(Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{ck}=13.3 MHz, V_{ck}=250 mVp-p sine wave, See "Electrical characteristics test circuit")

Item	Symbol	Measuring condition	SW condition		Measuring point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	14	16	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20 log ($V_{4.43\ MHz}$/ $V_{250\ kHz}$) *1	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope *2	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	$V_{IN\text{-}AC}$		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	$V_{IN\text{-}AC}$		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO\text{-}DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED\text{-}DC}$	INPUT=250 kHz, 1.28 Vp-p.	a	a	V5	1.3	2.3	3.3	V
	$V_{OUT\text{-}DC}$				V6	1.7	2.7	3.7	V

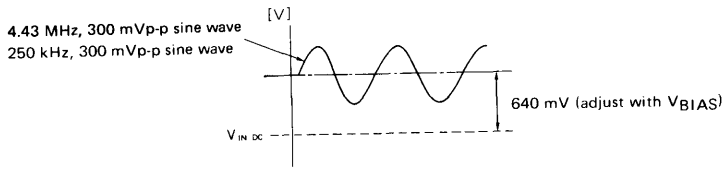
Electrical Characteristics Test Circuit



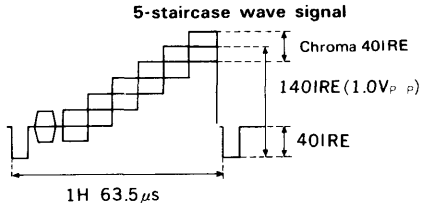
Note *1. Frequency characteristics measuring condition

$V_{4.43\ MHz}$ (Output signal voltage [Vp-p] at 4.43 MHz input)
$V_{250\ kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 8 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.

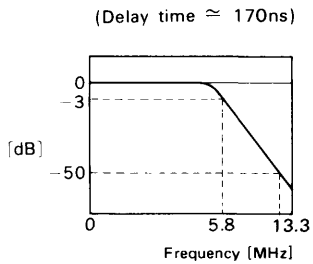


*2. Differential gain and differential phase measuring condition

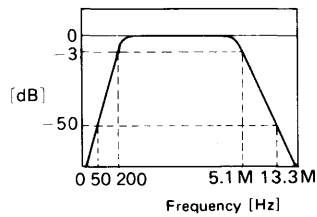


DG and DP are measured at output S point by vectorscope.

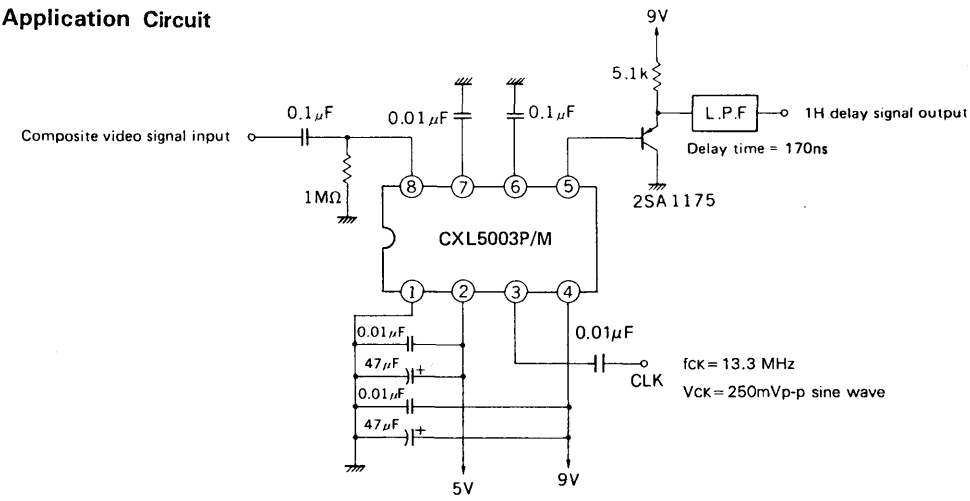
*3. LPF frequency characteristics



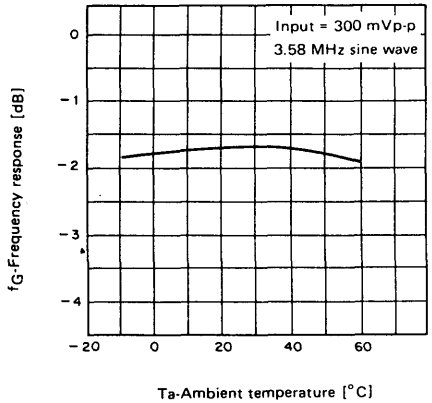
*4. BPF frequency characteristics



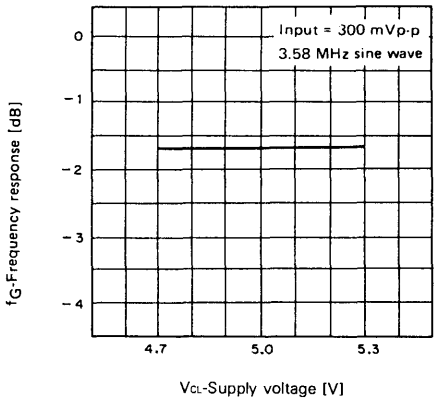
Application Circuit



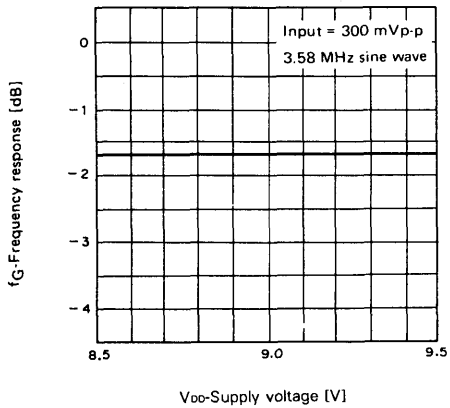
Frequency response vs. Ambient temperature



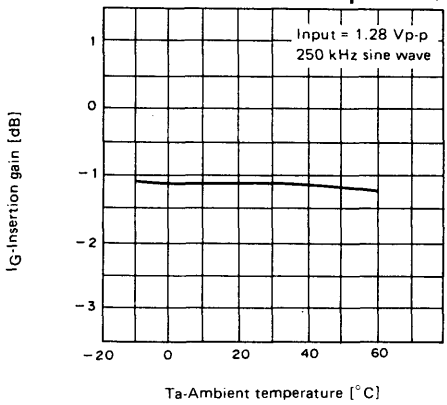
Frequency response vs. Supply voltage



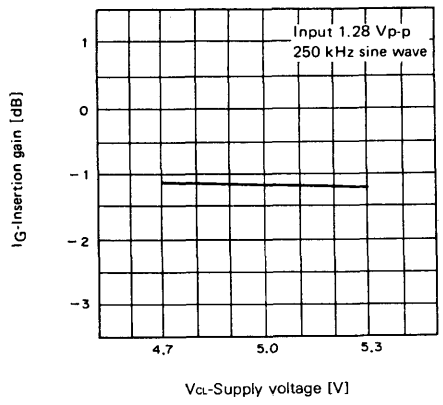
Frequency response vs. Supply voltage



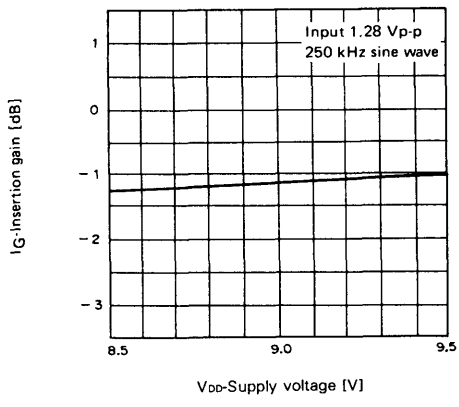
Insertion gain vs. Ambient temperature



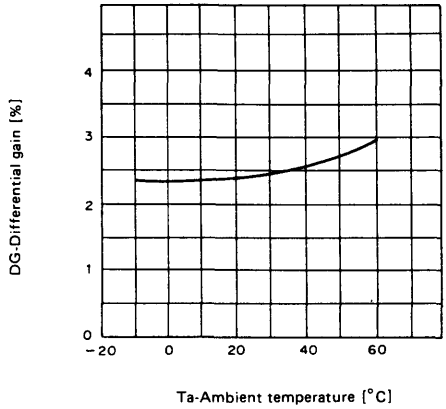
Insertion gain vs. Supply voltage



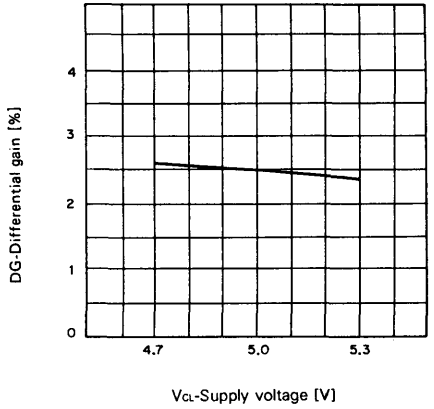
Insertion gain vs. Supply voltage



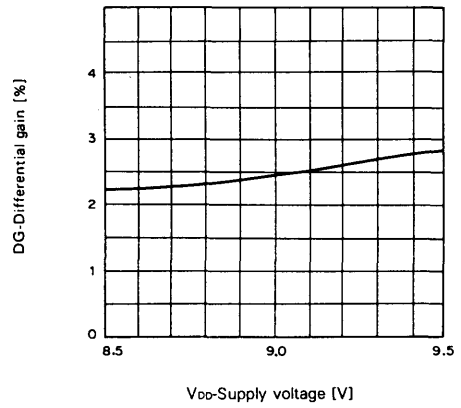
Differential gain vs. Ambient temperature



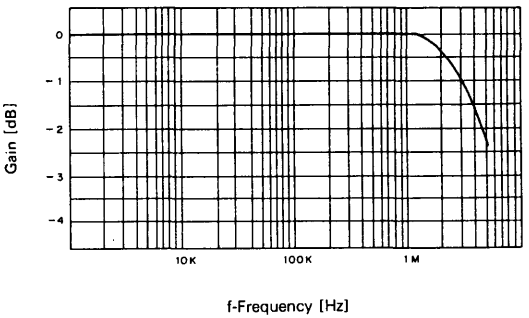
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage



Frequency response



SONY CXL5005P/CXL5005M

CMOS-CCD 1H Delay Line for NTSC with PLL

Description

CXL5005P/CXL5005M are general purpose CCD delay line ICs which provide 1H delay time of NTSC.

The ICs are operative with a color sub-carrier frequency (3.58 MHz), as they contain a PLL.

Features

- Low power consumption 90 mW (Typ.)
- Small size package (14-pin DIP, SOP)
- Low differential gain DG=3% (Typ.)
- Input signal amplitude 180 IRE (=1.28 Vp-p, Max.)
- Low input clock amplitude operation 200 mVp-p (Min.)
- On chip peripheral circuits.
- 3xfsc output pin is provided.

Structure

CMOS-CCD

Functions

- 680 bit CCD resister
- Clock drivers
- Autobias circuit
- Synchronized tip clamp circuit
- Sample and hold circuit
- PLL (Phase Locked Loop)

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	11	V
• Supply voltage	V_{CL}	6	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation			
	P_D	CXL5005P 800	mW
		CXL5005M 400	mW

Recommended Operating Conditions

• Supply voltage	V_{DD}	9	V±5%
	V_{CL}	5	V±5%

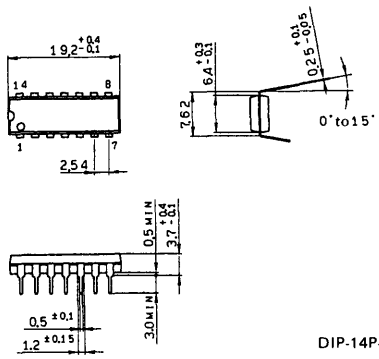
Recommended Clock Conditions

• Input clock amplitude	V_{CLK}	200 mVp-p to 1.0 Vp-p (300mVp-p Typ.)
• Clock frequency	f_{CLK}	3.579545 MHz

Package Outline

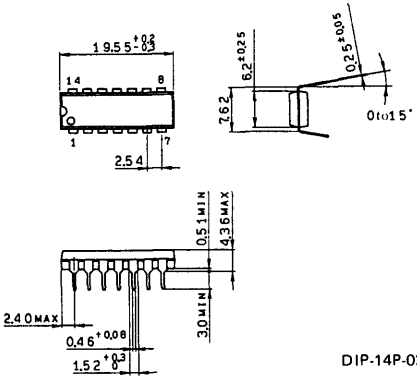
Unit: mm

CXL5005P 14Pin DIP (Plastic)



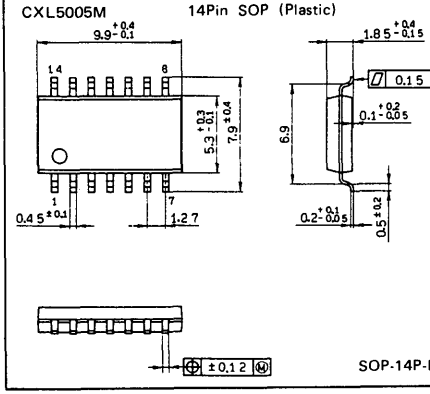
DIP-14P-01

14Pin DIP (Plastic)



DIP-14P-021

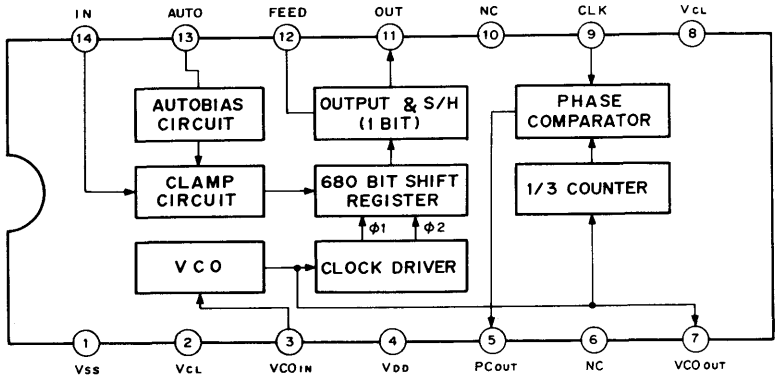
CXL5005M 14Pin SOP (Plastic)



SOP-14P-L01

E88Z40-ST

Block Diagram



Pin Description

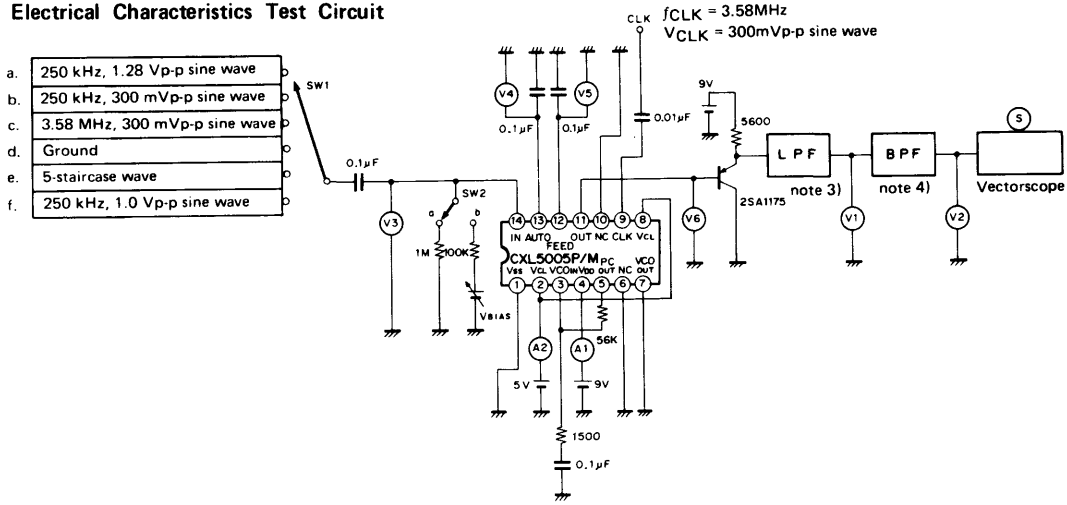
No.	Symbol	Description	Impedance [Ω]	No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND		8	V_{CL}	5V power supply	
2	V_{CL}	5V power supply		9	CLK	Clock input	≈ 5k
3	VCO_{IN}	VCO input	>100k	10	NC		
4	V_{DD}	9V power supply		11	OUT	Signal output	600 to 1k
5	PC_{OUT}	Phase Comparator output	≈ 5k	12	FEED	Feedback DC output	>100k
6	NC			13	AUTO	Autobias DC output	10k
7	VCO_{OUT}	VCO output	≈ 5k	14	IN	Signal input	>100k

Electrical Characteristics

(Ta=25°C, V_{DD}=9.0V, V_{CL}=5.0V, f_{CK}=3.58 MHz, V_{CK}=300 mVp-p sine wave, Test poit See"Electrcal characteristics test circuit")

Item	Symbol	Test condition	SW condition		Test point	Min.	Typ.	Max.	Unit
			SW1	SW2					
Supply current	I_{DD}	INPUT=250 kHz, 1.28 Vp-p.	a	a	A1	—	4	5	mA
	I_{CL}				A2	—	9	12	mA
Insertion gain	IG	INPUT=250 kHz, 1.28 Vp-p IG=20log (Output voltage [Vp-p]/ 1.28[Vp-p])	a	a	V1	−3	0	3	dB
Frequency response	fG	fG=20log ($V_{3.58\ MHz}$/ $V_{250\ kHz}$) (Note 1)	b,c	b	V1	−3.0	−2.1	—	dB
Differential gain	DG	5-staircase wave input Y=140IRE (=1.0 Vp-p) Measure S point with vectorscope (Note 2)	e	a	S	—	3	5	%
Differential phase	DP					—	3	5	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: input=250 kHz 1.0 Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: input=DC output (Vrms)	d	a	V2				
Output DC voltage	V_{IN-AC}		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$	INPUT=250 kHz, 1.28 Vp-p.	a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

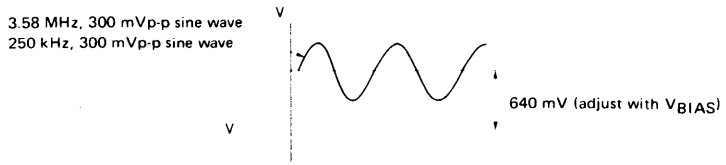
Electrical Characteristics Test Circuit



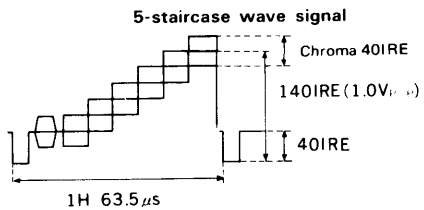
Note 1) Frequency characteristics measuring condition

$V_{3.58\ MHz}$ (Output signal voltage [Vp-p] at 3.58 MHz input)
$V_{250\ kHz}$ (Output signal voltage [Vp-p] at 250 kHz input)

Set pin 14 (IN) voltage [V] = $V_{IN\text{-}DC}$ + 640 mV.



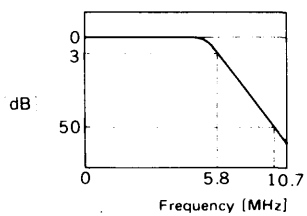
2) Differential gain and differential phase measuring condition



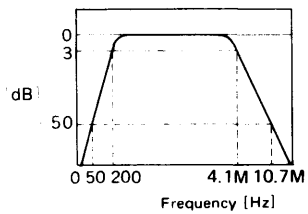
DG and DP are measured at output S point by vectorscope.

3) LPF frequency characteristics

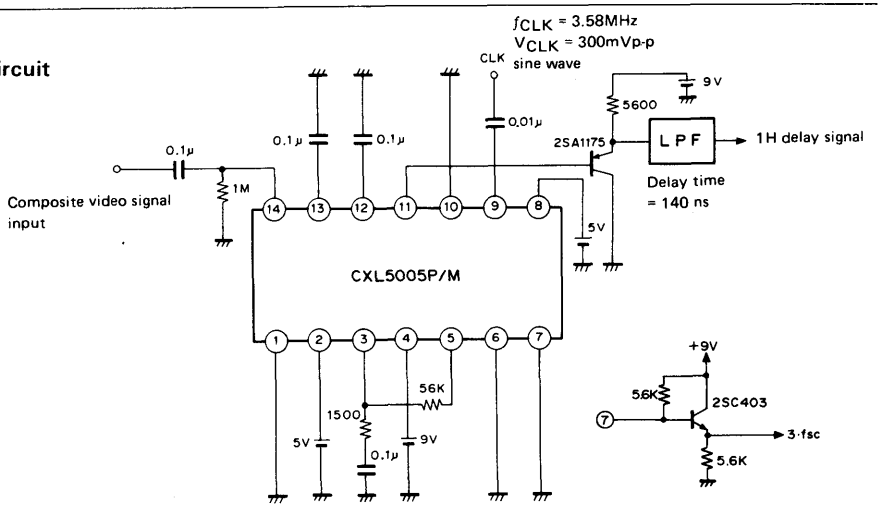
(Delay time ≃ 140ns)



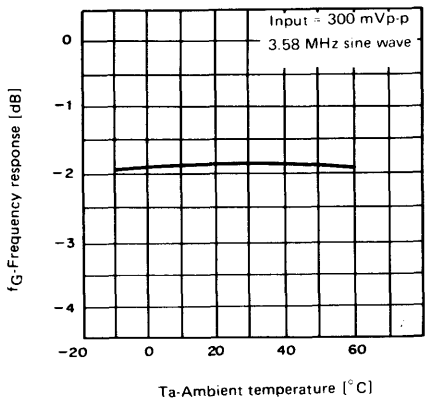
4) BPF frequency characteristics



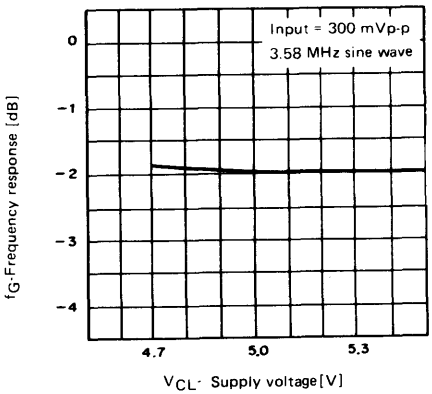
Application Circuit



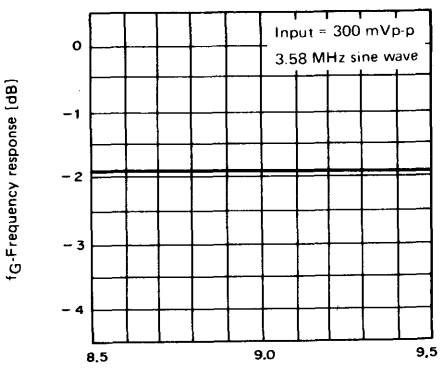
Frequency response vs. Ambient temperature



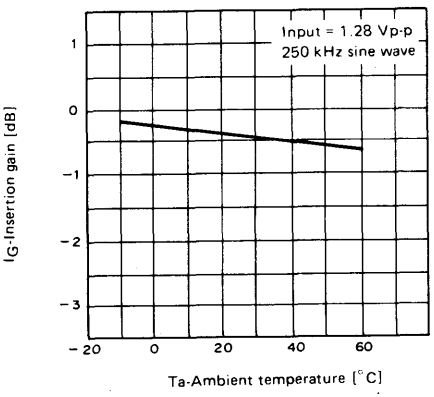
Frequency response vs. Supply voltage



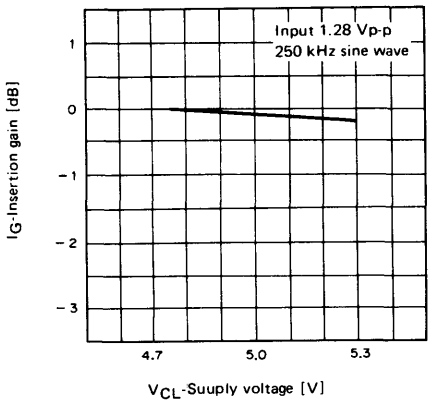
Frequency response vs. Supply voltage



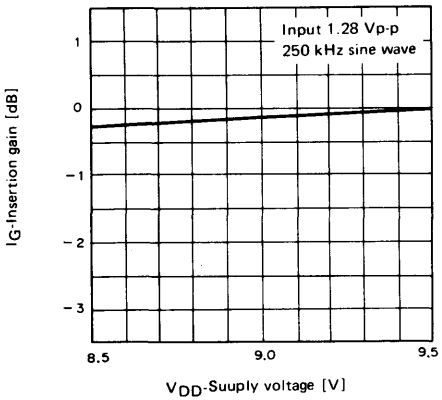
Insertion gain vs. Ambient temperature



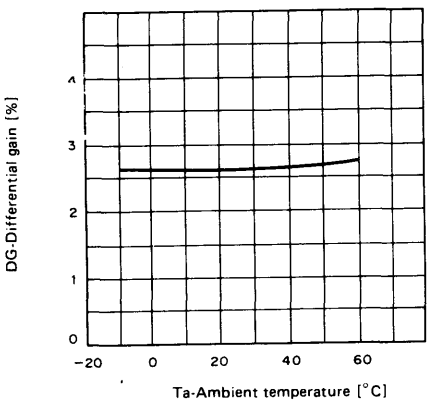
Insertion gain vs. Supply voltage



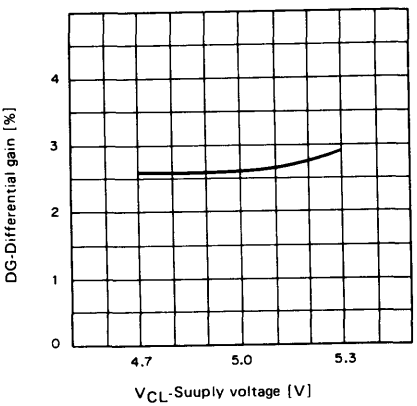
Insertion gain vs. Supply voltage



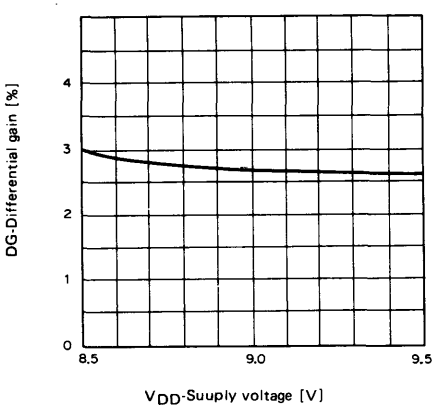
Differential gain vs. Ambient temperature



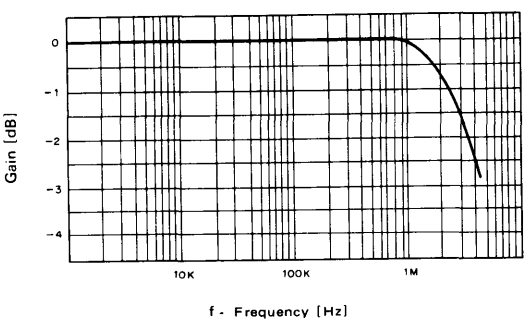
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage



Frequency response



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